Voltage Regulators

LM105/LM205/LM305 voltage regulator

general description

The LM105, LM205 and LM305 are positive voltage regulators similar to the LM100, except that an extra gain stage has been added for improved regulation. A redesign of the biasing circuitry removes any minimum load current requirement and at the same time reduces standby current drain, permitting higher voltage operation. They are direct, plug-in replacements for the LM100 in both linear and switching regulator circuits with output voltages greater than 4.5V. Important characteristics of the circuits are:

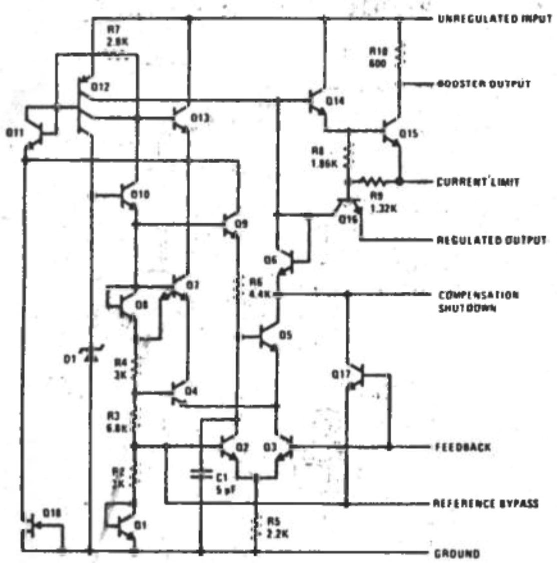
- Output voltage adjustable from 4.5V to 40V
- Output currents in excess of 10A possible by adding external transistors
- Load regulation better than 0.1%, full load with current limiting
- DC line regulation guaranteed at 0.03%/V
- Ripple rejection of 0.01%/V

Like the LM100, they also feature fast response to both load and line transients, freedom from oscillations with varying resistive and reactive loads and the ability to start reliably on any load within rating. The circuits are built on a single silicon chip and are supplied in either an 8-lead, TO-5 header or a 1/4" x 1/4" metal flat package.

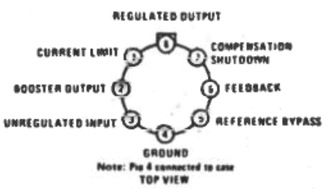
The LM205 is identical to the LM105 except that it is specified for operation from −25°C to 85°C.

The LM305 is specified for operation from 0°C to 70°C and for output voltages to 30V.

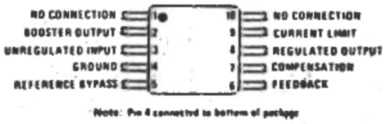
schematic and connection diagrams



Metal Can

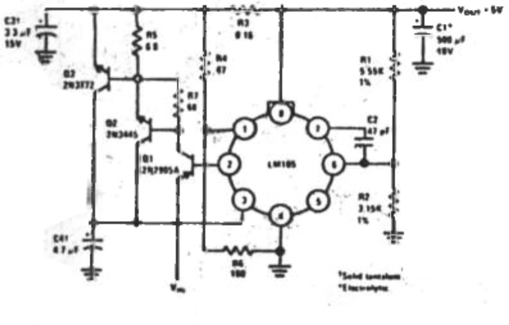


Flat Package

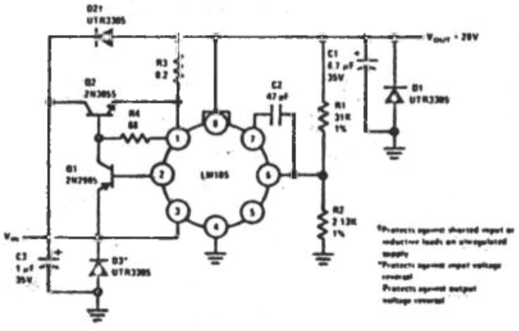


typical applications

10A Regulator with Foldback Current Limiting



1.0A Regulator with Protective Diodes


D2† UTR3305
VOUT = 20V
R3 0.2
Q2 2N3055
R4 68
Q1 2N2905
C2 47 pF
C1 4.7 µF 35V
R1 31K 1%
R2 2.13K 1%
D1 UTR3305
C3 1 µF 35V
D3* UTR3305
VIN
LM105
*Protects against shorted input or inductive loads on unregulated supply
**Protects against input voltage reversal
†Protects against output voltage reversal

absolute maximum ratings

Input Voltage	
LM105, LM205	50V
LM305	40V
Input-Output Voltage Differential	40V
Power Dissipation (Note 1)	
LM105, LM205	800 mW
LM305	500 mW
Operating Temperature Range	0°C to 70°C
LM105	-55°C to +85°C
LM205	-25°C to +150°C
LM305	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range					
LM105, LM205		8.5		50	V
LM305		8.5		40	V
Output Voltage Range					
LM105, LM205		4.5		40	V
LM305		4.5		30	V
Output-Input Voltage Differential		3.0		30	V
Load Regulation (Note 3)					
LM105	$0 \leq I_O \leq 12$ mA				
	R_{SC} = 18Ω, T_A = 25°C		0.02	0.05	%
	R_{SC} = 10Ω, T_A = 125°C		0.03	0.1	%
	R_{SC} = 18Ω, T_A = -55°C		0.03	0.1	%
LM205	$0 \leq I_o \leq 12\,\mu$A				
	R_{SC} = 18Ω, T_A = 25°C		0.02	0.05	%
	R_{SC} = 10Ω, T_A = 85°C		0.03	0.1	%
	R_{SC} = 18Ω, T_A = -25°C		0.03	0.1	%
LM305	$0 \leq I_O \leq 12$ mA				
	R_{SC} = 18Ω, T_A = 25°C		0.02	0.05	%
	R_{SC} = 15Ω, T_A = 70°C		0.03	0.1	%
	R_{SC} = 18Ω, T_A = 0°C		0.03	0.0	%
Line Regulation	$V_{IN} - V_{OUT} \leq 5V$		0.025	0.06	%/V
	$V_{IN} - V_{OUT} > 5V$		0.015	0.03	%/V
Ripple Rejection	C_{REF} = 10 μF, f = 120 Hz		0.003	0.01	%/V
Temperature Stability					
LM105	$-55°C \leq T_A \leq 125°C$		0.3	1.0	%
LM205	$-25°C \leq T_A \leq 85°C$		0.3	1.0	%
LM305	$0°C \leq T_A \leq 70°C$		0.3	1.0	%
Feedback Sense Voltage		1.63	1.7	1.81	V
Output Noise Voltage	$10 \text{ Hz} \leq f \leq 10 \text{ kHz}$				
	C_{REF} = 0		0.005		%
	$C_{REF} > 0.1\,\mu$F		0.002		%
Standby Current Drain					
LM105, LM205	V_{IN} = 40V		0.8	2.0	mA
LM305	V_{IN} = 50V		0.8	2.0	mA
Long Term Stability			0.1	1.0	%

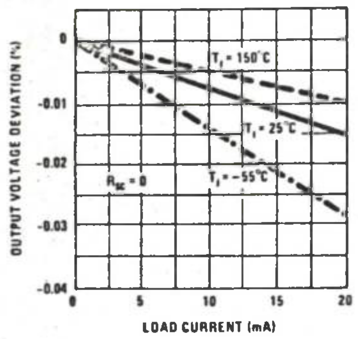
Note 1: The maximum junction temperature of the LM105 is 150°C, while that for the LM205 is 100°C, and that for the LM305 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. Peak dissipations to 1W are allowable providing the dissipation rating is not exceeded with the power averaged over a five second interval for the LM105 and LM205, and averaged over a two second interval for the LM305.

Note 2: These specifications apply for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2 kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation. With the LM205, however, all temperature specifications are limited to –25°C to 85°C.

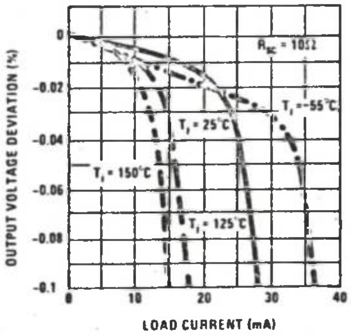
Note 3: The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

typical performance characteristics

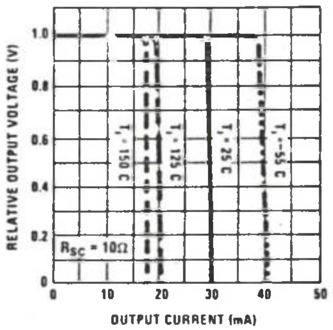
Load Regulation



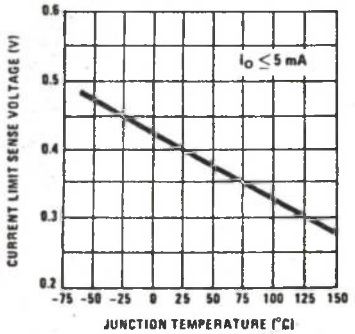
Load Regulation



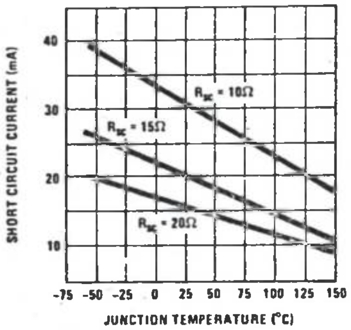
Current Limiting Characteristics



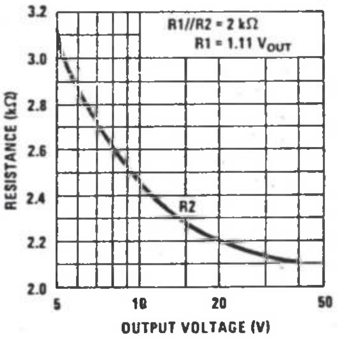
Current Limit Sense Voltage



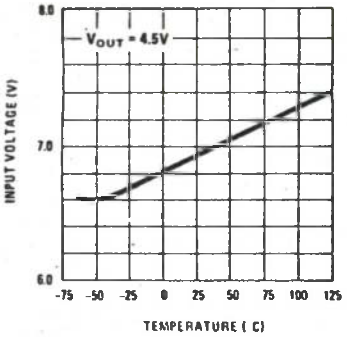
Short Circuit Current



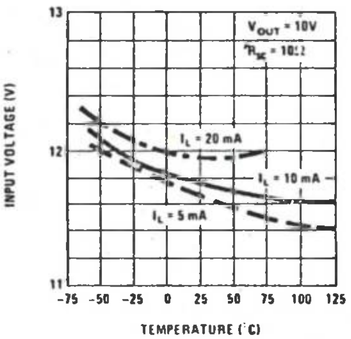
Optimum Divider Resistance Values



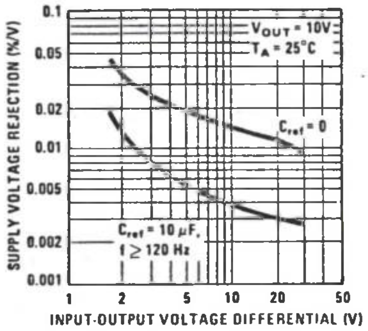
Minimum Input Voltage



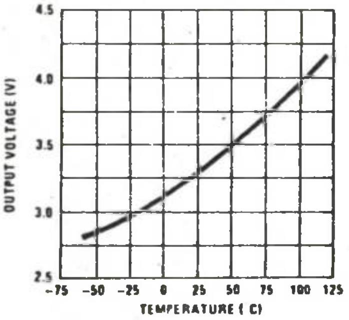
Regulator Dropout Voltage



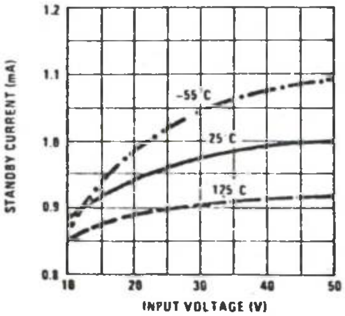
Supply Voltage Rejection



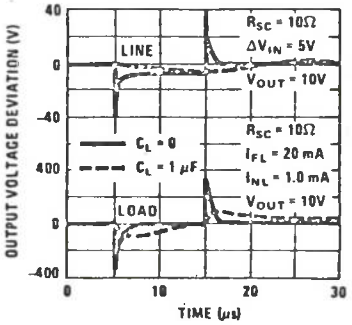
Minimum Output Voltage



Standby Current Drain

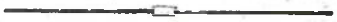


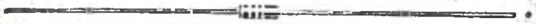
Transient Response

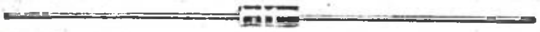


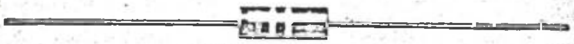
Pertinent Information for the Design Engineers Concerning Allen-Bradley Resistors

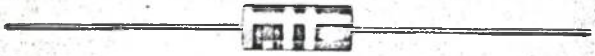
General Purpose Resistors


TYPE TR—1/10 Watt


TYPE CB—¼ Watt

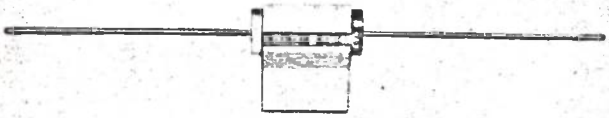

TYPE EB—½ Watt


TYPE GB—1 Watt

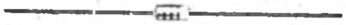

TYPE HB—2 Watt

Metal Clad Resistors

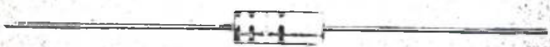
TYPE GM—3 Watt


TYPE HM—4 Watt

Hermetically Sealed— Ceramic Encased Resistors


TYPE TS—⅛ Watt

TYPE CS—⅓ Watt


TYPE ES—1 Watt

1. Resistance changes due to humidity are temporary, and in the case of Allen-Bradley resistors are reversible.
2. Resistance changes due to increase in moisture content are always positive.
3. Resistance change due to humidity in low-value resistors is less than in high-value resistors.
4. Change of resistance which has occurred due to humidity may be essentially eliminated by conditioning the resistor at 100°C for 48 hours.
5. Resistors operating with as little as 1/10th rated wattage load are essentially not affected by humidity.
6. Hermetically-sealed resistors do not exhibit resistance change because of humidity.
7. Resistance change due to load life is permanent and ultimately negative.
8. Resistance change due to load life can be minimized —1% to 2% in many thousands of hours by 50% derating.
9. This same result can be attained by limiting the maximum operating surface temperature of the resistor under load to 100°C.
10. Resistance change due to soldering is positive and may be permanent if the resistor has moisture present in its body. It can be greatly minimized if resistors are dry at the time of soldering.
11. The temperature characteristic of the Allen-Bradley resistor is positive above and below room temperature —room temperature is considered to be between 10°C and 30°C.
12. The temperature characteristic of the Allen-Bradley resistor is negligible from −10°C to +80°C.
13. The voltage characteristic of the Allen-Bradley resistor is negative and is less at elevated operated temperatures than at room ambient.
14. The voltage characteristic is less in low-value resistors than in high-value units.
15. The voltage characteristic and the temperature characteristic tend to cancel one another in an Allen-Bradley resistor under average operating conditions, where both voltage and temperature are present.
16. The heat sink to which a resistor is connected affects its rating. Resistors operated in parallel should be derated unless an adequate heat sink is provided.
17. The quality and reliability of Allen-Bradley resistors is the same for, and independent of, any resistance tolerances shown on the resistor.

Publication 6301 (November 3, 1958)

HIGH SPEED ANALOG COMPARATOR

SIGNETICS MONOLITHIC LINEAR CIRCUITS

SE526A
NE526A
SE526G
NE526G
SE526K
NE526K

JULY 1969

SE526A, NE526A, SE526G, NE526G, SE526K, NE526K

DESCRIPTION

The 526 is a high speed analog comparator intended for use in systems where low propagation delay and fast recovery from common mode or differential input overdrive is required. The device is specifically designed to provide a wide input common mode range while operating from power supplies commonly found in digital logic systems.

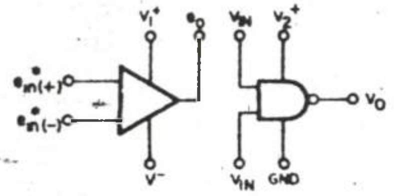
The 526 consists of a medium gain, high frequency differential amplifier and a high speed TTL gate fabricated within a single substrate by planer and epitaxial techniques. The output gate of the 526 has voltage and current capabilities compatible with DCL, DTL and TTL. The 526 output gate has a full fan-out of 10 to standard TTL loads.

The amplifier and gate may be used independently or cascaded for applications as a voltage comparator, digital line receiver or sense amplifier. The second gate input is used to provide strobe capability when operating the amplifier and gate in cascade. Additional applications information can be found under "Usage Information" in this data sheet.

FEATURES

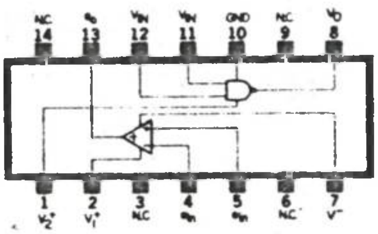
PROPAGATION DELAY -	30ns
INPUT COMMON MODE RANGE -	+4.5V -3.5V
DIFFERENTIAL OVERDRIVE RECOVERY -	20ns
OUTPUT COMPATIBLE WITH STANDARD LOGIC FORMS	
OPERATES FROM STANDARD ±5V SUPPLIES	

PIN CONFIGURATIONS

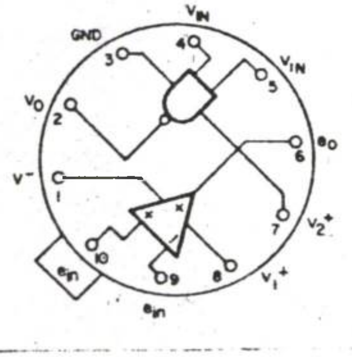


* INVERTING AND NON-INVERTING INPUTS ARE DEFINED RELATIVE TO AMPLIFIER OUTPUT, e_o

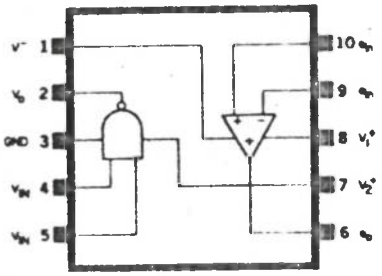
A PACKAGE



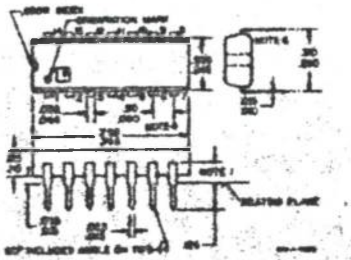
K PACKAGE



G PACKAGE



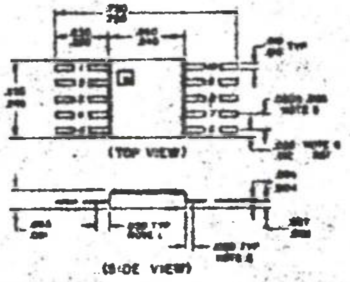
A PACKAGE (TO-116)



NOTES: (1) Lead spacing shall be measured within this zone.
(2) Molded Plastic Body.
(3) Kovar Leads.
(4) Lead spacing tolerances are non-cumulative.
(5) Thermal resistance from junction to still air, Θ_{J-A} = 0.16°C/mW.
(6) Leads shown as positioned by Signetics dual in-line package carrier.
(7) All dimensions of plastic package exclude molding-caused flash.

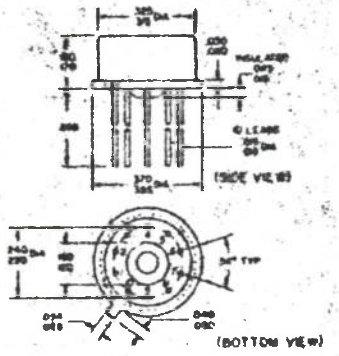
G PACKAGE (TO-91)

(MODULAR GLASS-KOVAR)



NOTES:
(1) Recommended minimum offset before lead bend.
(2) All leads weldable and solderable.
(3) Pin 1 internally connected to case.
(4) All dimensions in inches.
(5) Tolerances are non-cumulative.
(6) Lead spacing dimensions apply to this area only.
(7) Signetics symbol on flat package denotes lead No. 1.
(8) Thermal resistance (both G and K packages) from junction to case, Θ_{J-C} = 0.2°C/mW.

K PACKAGE (TO-100)



RECOMMENDED OPERATING SUPPLY VOLTAGES: $V_1^+ = V_2^+ = 5.0V$, $V^- = -5.0V$

ABSOLUTE MAXIMUM RATINGS*

SUPPLY VOLTAGE	±7.0V	STORAGE TEMPERATURE	-65°C to +150°C
GATE INPUT VOLTAGE	+6.0V	OPERATING TEMPERATURE	
DIFFERENTIAL INPUT VOLTAGE	+5.0V	SE526	-55°C to +125°C
COMMON MODE INPUT VOLTAGE	±5.0V	NE526	0°C to +75°C
GATE OUTPUT CURRENT	±100mA		

* Absolute Maximum Ratings are limiting values above which serviceability may be impaired.

ELECTRICAL CHARACTERISTICS (NOTES 1, 2, 3, 4, 13, 14) -- STANDARD CONDITIONS $V_1^+ = V_2^+ = 5.0V$, $V^- = -5.0V$

ACCEPTANCE TEST SUBGROUP	CHARACTERISTIC	SYMBOL	LIMITS				TEST CONDITIONS			NOTES
							TEMPERATURE		TEST CIRCUIT	
			MIN.	TYP.	MAX.	UNIT	SE526	NE526		
A-5	Input Offset Voltage	V_{io}		2.0	5.0	mV	-55°C	+ 0°C	Figure 1	5
A-7		V_{io}		2.0	5.0	mV	+25°C	+25°C	Figure 1	5
A-4		V_{io}		2.0	5.0	mV	+125°C	+75°C	Figure 1	5
A-4	Input Bias Current	I_{in}		30.0	35.0	µA	-55°C	0°C	Figure 2	6
A-7		I_{in}		25.0	35.0	µA	+25°C	+25°C	Figure 2	6
A-6		I_{in}		22.0	35.0	µA	+125°C	+75°C	Figure 2	6
A-4	Input Offset Current	I_{io}		0.6	5.0	µA	-55°C	0°C	Figure 2	
A-7		I_{io}		0.5	5.0	µA	+25°C	+25°C	Figure 2	
A-5		I_{io}		0.4	5.0	µA	+125°C	+75°C	Figure 2	
A-4	Input Common Mode Range	V_{cm}	+4.2	+4.7		V	-55°C	0°C	Figure 1	
A-2		V_{cm}	+4.2	+4.5		V	+25°C	+25°C	Figure 1	
A-6		V_{cm}	+4.2	+4.4		V	+125°C	+75°C	Figure 1	
A-4		V_{cm}	-3.2	-3.5		V	-55°C	0°C	Figure 1	
A-2		V_{cm}	-3.2	-3.5		V	+25°C	+25°C	Figure 1	
A-5		V_{cm}	-3.2	-3.5		V	+125°C	+75°C	Figure 1	
A-6	Amplifier Output Voltage	V_{ohi}	3.5			V	-55°C	0°C	Figure 3	
A-3		V_{ohi}	3.5			V	+25°C	+25°C	Figure 3	
[illegible]		V_{ohi}	3.5			V	+125°C	+75°C	Figure 3	
A-5		V_{olo}			0.6	V	-55°C	0°C	Figure 3	
A-2		V_{olo}			0.5	V	+25°C	+25°C	Figure 3	
A-4		V_{olo}			0.4	V	+125°C	+75°C	Figure 3	
Q1	Amplifier Power Consumption	P_d		90	120	mW	-55°C	0°C	Figure 4	
A-2		P_d		100	120	mW	+25°C	+25°C	Figure 4	
A-4		P_d		110	120	mW	+125°C	+75°C	Figure 4	
A-5	Gate Output Voltage	$V1_o$	2.8	3.5		V	-55°C	0°C	Figure 5	7, 8
A-3		$V1_o$	2.8	3.2		V	+25°C	+25°C	Figure 5	7, 8
A-4		$V1_o$	2.8	3.0		V	+125°C	+75°C	Figure 5	7, 8
A-6		$V0_o$		0.3	0.4	V	-55°C	0°C	Figure 5	7, 8
A-3		$V0_o$		0.2	0.4	V	+25°C	+25°C	Figure 5	7, 8
A-6		$V0_o$		0.3	0.4	V	+125°C	+75°C	Figure 5	7, 8
	Gate Output Sink Current	$I0_o$	16.0			mA	+25°C	+25°C	Figure 5	8
	Gate Output Source Current	$I1_o$	1.0			mA	+25°C	+25°C	Figure 5	7
	Gate Input Threshold Voltage	$V1_i$	2.0			V	-55°C	0°C	Figure 5	9
		$V1_i$	2.0			V	+25°C	+25°C	Figure 5	9
		$V1_i$	2.0			V	+125°C	+75°C	Figure 5	9
		$V0_i$			1.0	V	-55°C	0°C	Figure 5	10
		$V0_i$			0.9	V	+25°C	+25°C	Figure 5	10
		$V0_i$			0.8	V	+125°C	+75°C	Figure 5	10

ELECTRICAL CHARACTERISTICS (NOTES 1, 2, 3, 4, 13, 14) STANDARD CONDITIONS: $V_1^+ = V_2^+ = 5.0V$, $V^- = -5.0V$

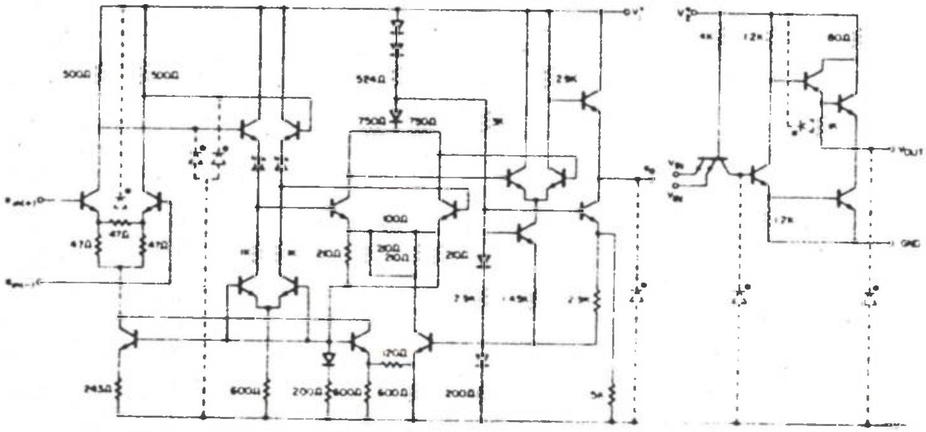
(Continued)

ACCEPTANCE TEST SUBGROUP	CHARACTERISTIC	SYMBOL	LIMITS				TEST CONDITIONS			NOTES
							TEMPERATURE		TEST CIRCUIT	
			MIN.	TYP.	MAX.	UNIT	SE526	NE526		
C-1	Gate Input Current (Input "0")	$I0_i$	-0.1	-1.2	-1.6	mA	-55°C	0°C	Figure 6	
A-3		$I0_i$	-0.1	-1.4	-1.6	mA	+25°C	+25°C	Figure 6	
C-1		$I0_i$	-0.1	-1.2	-1.6	mA	+125°C	+75°C	Figure 6	
C-1	(Input "1")	$I1_i$		5	25	µA	-55°C	0°C	Figure 7	
A-3		$I1_i$		10	25	µA	+25°C	+25°C	Figure 7	
A-4		$I1_i$		15	25	µA	+125°C	+75°C	Figure 7	
C-1	Gate Current Consumption (Output "1")	$I_{cc}1$			2.00	mA	-55°C	0°C	Figure 8	
A-2		$I_{cc}1$			2.00	mA	+25°C	+25°C	Figure 8	
A-4		$I_{cc}1$			2.00	mA	+125°C	+75°C	Figure 8	
C-1	(Output "0")	$I_{cc}0$			5.00	mA	-55°C	0°C	Figure 8	
A-2		$I_{cc}0$			5.00	mA	+25°C	+25°C	Figure 8	
A-4		$I_{cc}0$			5.00	mA	+125°C	+75°C	Figure 8	
A-2	Gate Input Latch Voltage Rating	BV_i			6.0	V	+25°C	+25°C	Figure 9	
A-2	Gate Output Short Circuit Current	I_{so}	-10.0		-70.0	mA	+25°C	+25°C	Figure 10	
	Switching Times									
A-6	Gate Turn-On Delay	T_{on}		15	17	ns	+25°C	+25°C	Figure 11	11
A-6	Gate Turn-Off Delay	T_{off}		15	17	ns	+25°C	+25°C	Figure 11	11
A-6	Propagation Delay	$T_{pd}0$		30	42	ns	+25°C	+25°C	Figure 12	11
A-6	Propagation Delay	$T_{pd}1$		40	48	ns	+25°C	+25°C	Figure 12	11
C-2	Differential Overload Recovery Time	t_{dm}		30	40	ns	+25°C	+25°C	Figure 13	11, 12

Notes

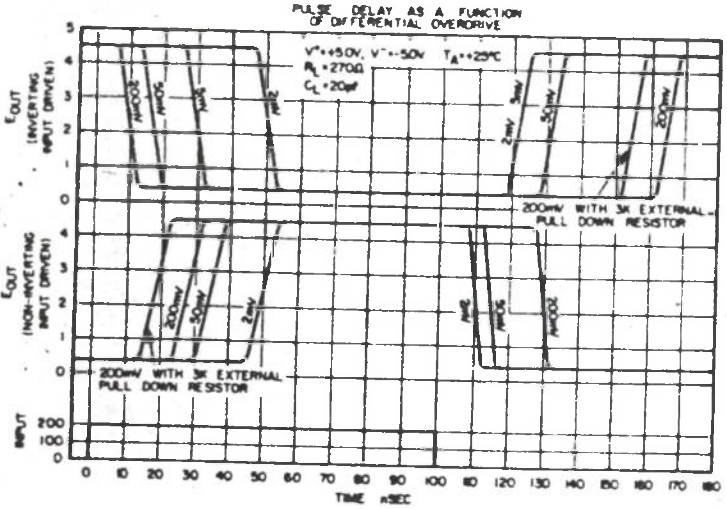
1. All measurements are referenced to the ground terminal.
2. Positive current is defined as into the pin referenced.
3. Pins not specifically referenced are left electrically open.
4. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
5. Input Offset Voltage is tested at guaranteed Input Common Mode Range voltage limits and includes the worst-case variations of voltage gain and input impedance. These are the maximum values required to drive the output down to "0" or up to "1".
6. Input Bias Current is defined as the maximum current required to bias either input.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_2^+.
9. These limits are guaranteed by Gate Output Voltage ($V0_o$) test.
10. These limits are guaranteed by Gate Output Voltage ($V1_o$) tests.
11. Load capacitance includes test fixture and probe capacitance.
12. Differential Input Voltage = 500mV for this test.
13. Acceptance Test Subgroup A-7 provides end point parameters for linear devices processed to Signetics SURE Program. See Signetics SURE Bulletin 5001.
14. Manufacturer reserves the right to make design and process changes and improvements.

BASIC CIRCUIT SCHEMATIC

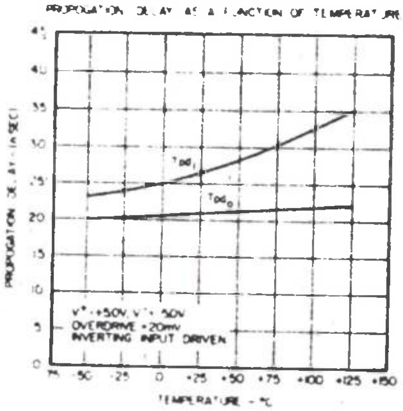


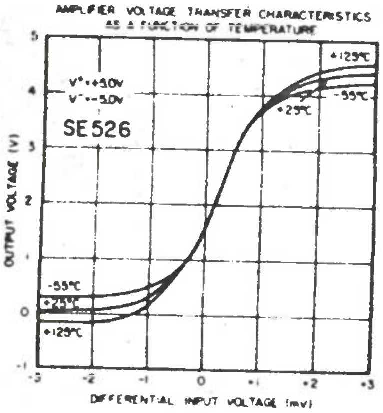
NOTES COMPONENT VALUES ARE TYPICAL
* ISOLATION DIODES

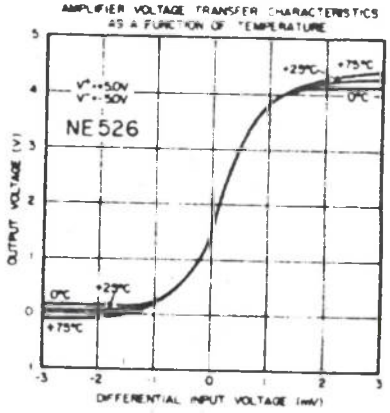
TYPICAL OPERATING CURVES

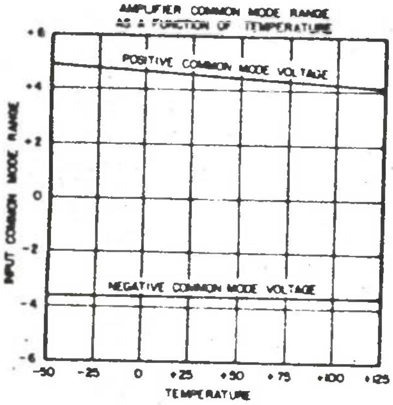


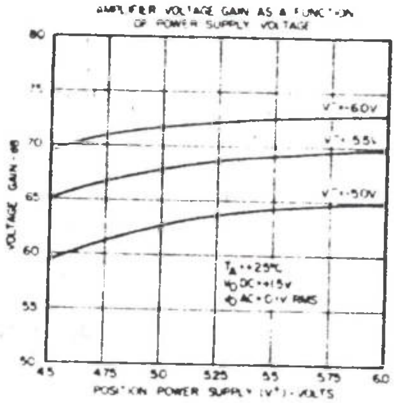
Pulse delay curves illustrate propagation delay at the leading edge and differential overload recovery at the trailing edge











SE526A
NE526A
SE526G
NE526G
SE526K
NE526K

USAGE INFORMATION

The 526 is designed for use in voltage comparator and sense amplifier applications. Because of its high voltage gain and high speed, care must be taken in its circuit application to ensure stable operation. The power supplies must be bypassed for frequencies as high as 50MHz. The source impedances should be kept as small as feasible and the inputs should be kept well isolated from the output to avoid generating a positive feedback loop. To optimize the effective input offset voltage external resistance used in the bases of the input transistors should be kept equal (Figure 1).

The amplifier and gate circuits are completely independent, making their external connection very versatile and capable of performing a multitude of functions. For most applications, the amplifier will be connected directly to the gate. The parasitic capacitance at the interconnecting point must be minimized if the propagation delay of the circuit is to be optimized. It is permissible to connect an external discrete resistor from the amplifier output to the negative supply (Figure 2). The increased sink capability resulting from this connection tends to reduce the propagation delay. The external pull-down resistor should be no less than 5000 ohms. The remaining gate input may be used to strobe the output of the amplifier output.

An external NAND gate may be cross-coupled with the gate output of the 526 to provide a bi-stable latch or storage element. In this application, the differential inputs of the amplifier should be biased such that the amplifier output will be positive when no input signal is present, i.e. the non-inverting input should be biased with respect to the inverting input (Figure 3).

Amplifier outputs may be tied together to provide the logical OR of the amplifier outputs (Figure 4). This technique will tend to increase propagation delay because of the parasitic capacitances associated with the connection.

The amplifier of one 526 may be used to drive the second gate input (strobe) of another 526, performing the logical NAND of the amplifier outputs. This configuration removes the strobe capability of the output (Figure 5). In either of these configurations, the unused 526 gate may be used to implement other system logic requirements.

The power supply inputs for the gate and amplifier are independent. Where power consumption is critical, the amplifier may be disabled while maintaining a logical 1 output at the gate. Total power consumption is reduced to about 20% of the power required for normal operation.

FIGURE 1

MINIMIZING EFFECTIVE INPUT OFFSET VOLTAGE

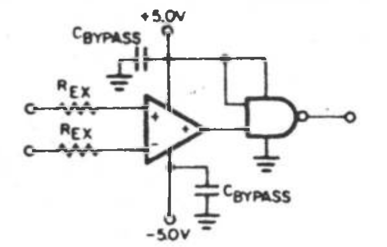


FIGURE 2

DECREASING PROPOGATION DELAY BY ADDITION OF EXTERNAL PULL DOWN RESISTOR

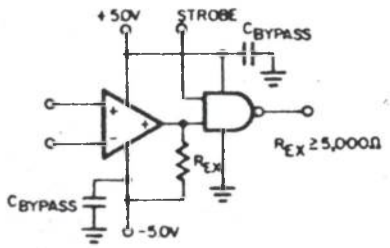


FIGURE 3

INCORPORATING EXTERNAL NAND GATE TO PROVIDE OUTPUT STORAGE

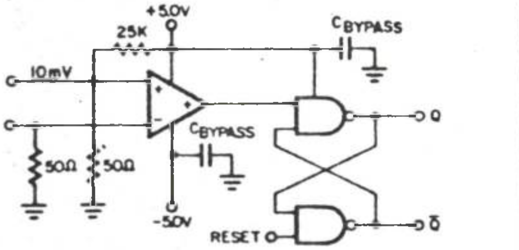
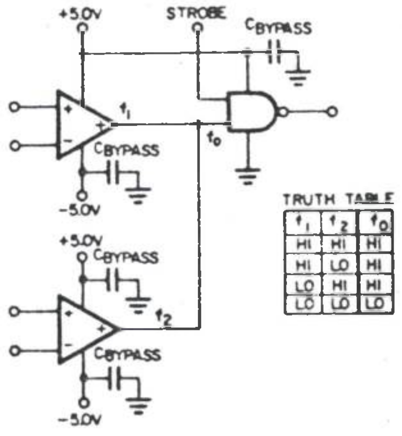


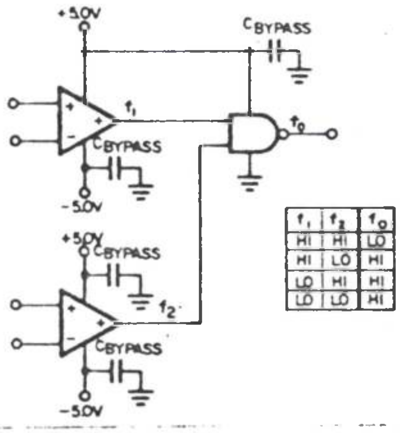
FIGURE 4 PARALLELING AMPLIFIER OUTPUTS PROVIDE THE LOGICAL OR OF THE AMPLIFIER OUTPUTS.



f1	f2	f0
HI	HI	HI
HI	LO	HI
LO	HI	HI
LO	LO	LO

FIGURE 5

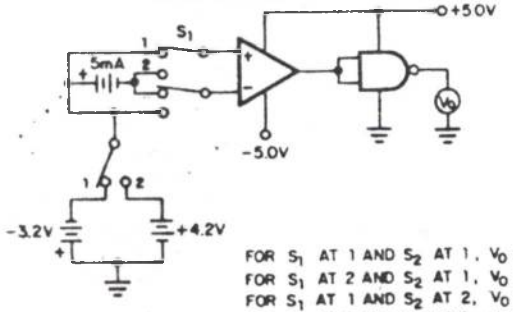
LOGICAL NAND OF THE AMPLIFIER OUTPUTS



f1	f2	f0
HI	HI	LO
HI	LO	HI
LO	HI	HI
LO	LO	HI

TEST FIGURE 1

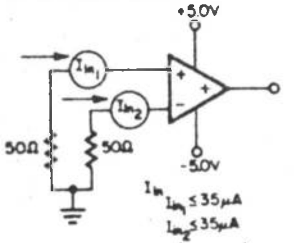
INPUT OFFSET VOLTAGE
INPUT COMMON MODE RANGE



FOR S_1 AT 1 AND S_2 AT 1, V_0 = "0"
FOR S_1 AT 2 AND S_2 AT 1, V_0 = "1"
FOR S_1 AT 1 AND S_2 AT 2, V_0 = "0"
FOR S_1 AT 2 AND S_2 AT 2, V_0 = "1"

TEST FIGURE 2

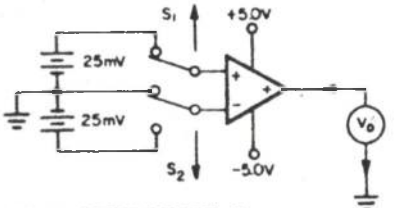
INPUT BIAS CURRENT
INPUT OFFSET CURRENT



I_{in} $I_{in_1} \le 35\mu A$
$I_{in_2} \le 35\mu A$
$I_{io} = |I_{in_1} - I_{in_2}| \le 5\mu A$

TEST FIGURE 3

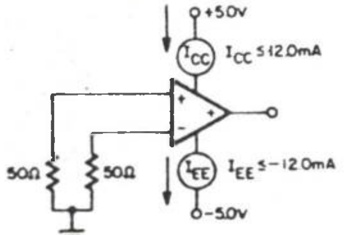
AMPLIFIER OUTPUT VOLTAGE



FOR V_{OH} SWITCH POSITION = S_1
FOR V_{OL} SWITCH POSITION = S_2

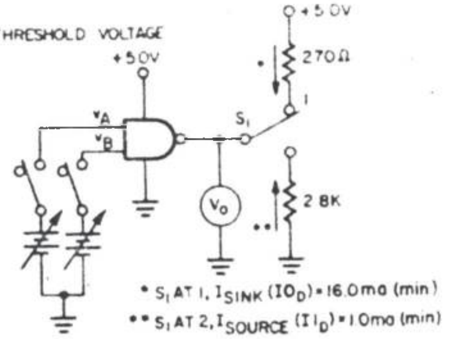
TEST FIGURE 4

AMPLIFIER POWER CONSUMPTION



TEST FIGURE 5

GATE INPUT THRESHOLD VOLTAGE

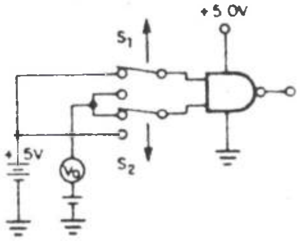


* S_1 AT 1, I_{SINK} (IO_D) = 16.0ma (min)
** S_1 AT 2, I_{SOURCE} (II_D) = 1.0ma (min)

TEST NO	INPUT CONDITION	-55°C/0°C	+25°C	+125°C/75°C	OUTPUT
1	V_A V_B	2.0V 2.0V	2.0V 2.0V	2.0V 2.0V	VO_0
2	V_A V_B	1.0V OPEN	0.9V OPEN	0.8V OPEN	VI_0
3	V_A V_B	OPEN 1.0V	OPEN 0.9V	OPEN 0.8V	VI_0

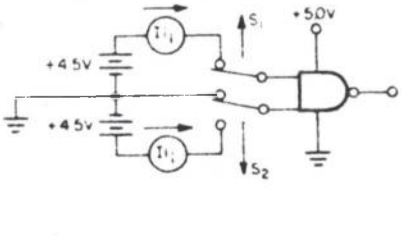
TEST FIGURE 6

GATE INPUT CURRENT (INPUT "0")



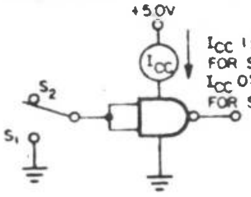
TEST FIGURE 7

GATE INPUT CURRENT (INPUT "1")



TEST FIGURE 8

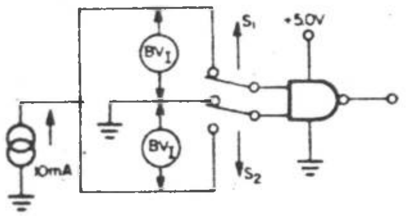
GATE POWER CONSUMPTION



I_{CC} 1 ≤ 2.0mA
FOR SWITCH POSITION 1
I_{CC} 0 ≤ 5.0mA
FOR SWITCH POSITION 2

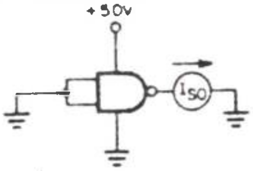
TEST FIGURE 9

GATE INPUT LATCH VOLTAGE RATING



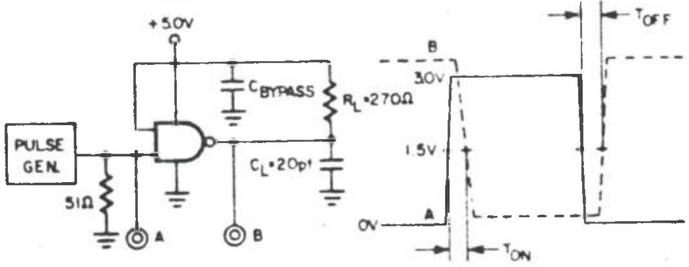
TEST FIGURE 10

GATE OUTPUT SHORT CIRCUIT CURRENT



TEST FIGURE 11

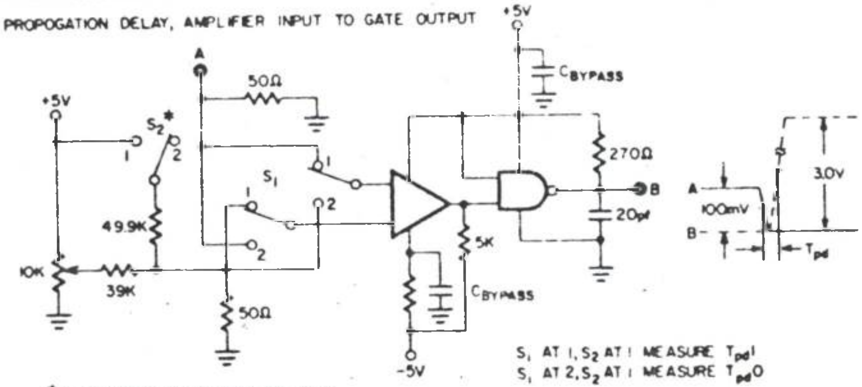
PROPOGATION DELAY, GATE INPUT TO GATE OUTPUT



INPUT PULSE A
AMPLITUDE = 3.0V
PULSE WIDTH = 100ns
$t_r = t_f \leq 10ns$

TEST FIGURE 12

PROPOGATION DELAY, AMPLIFIER INPUT TO GATE OUTPUT

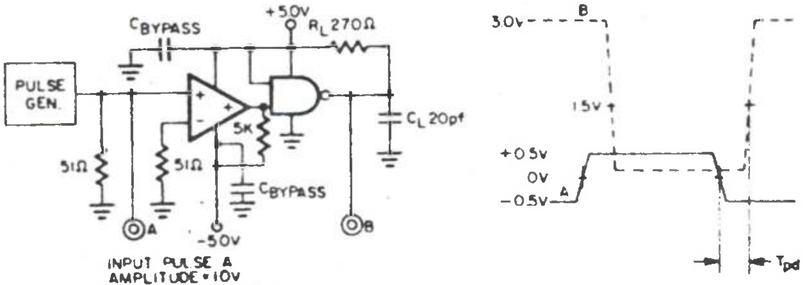


S1 AT 1, S2 AT 1 MEASURE $T_{pd}1$
S1 AT 2, S2 AT 1 MEASURE $T_{pd}0$

*S2 CHANGES DC OFFSET BY 5mV

TEST FIGURE 13

DIFFERENTIAL OVERLOAD RECOVERY TIME, AMPLIFIER INPUT TO GATE OUTPUT



INPUT PULSE A
AMPLITUDE = 1.0V
PULSE WIDTH = 100ns
$t_r = t_f \leq 10ns$

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC1595L
MC1495L

Specifications and Applications Information

WIDEBAND MONOLITHIC FOUR-QUADRANT MULTIPLIER

. . . designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

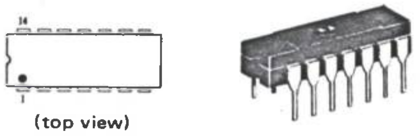
*When used with an operational amplifier.

- Wide Bandwidth
- Excellent Linearity – 1% max Error on X-Input, 2% max Error on Y-Input – MC1595L
- Excellent Linearity – 2% max Error on X-Input, 4% max Error on Y-Input – MC1495L
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ± 10 Volts
- ± 15 Volt Operation

LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON
EPITAXIAL PASSIVATED

DS 9124 R1



CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 – FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC

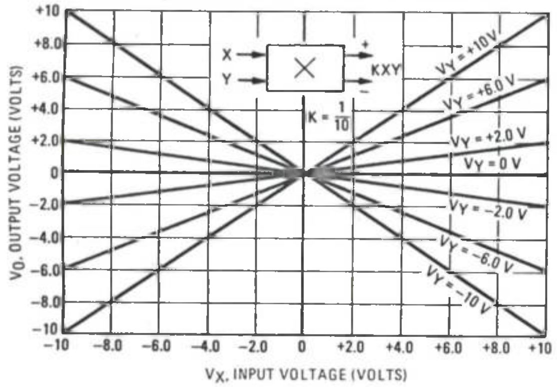


FIGURE 2 – TRANSCONDUCTANCE BANDWIDTH

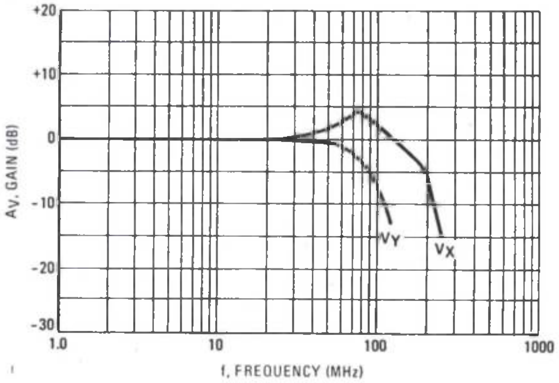
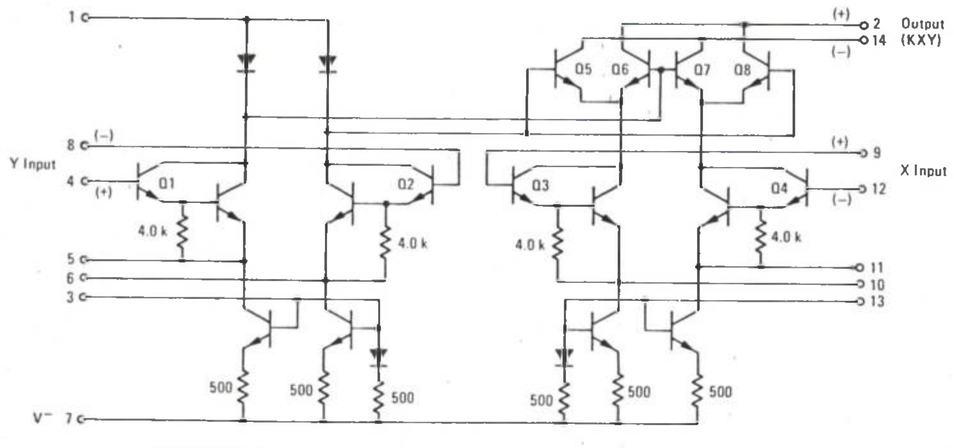


FIGURE 3 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (V^+ = +32V, V^- = −15 V, T_A = +25°C, $I_3 = I_{13}$ = 1 mA, $R_X = R_Y$ = 15 kΩ, R_L = 11 kΩ unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Linearity: Output Error in Percent of Full Scale:		5					%
T_A = +25°C							
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)	MC1495		E_{RX}	–	±1.0	±2.0	
	MC1595			–	±0.5	±1.0	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)	MC1495		E_{RY}	–	±2.0	±4.0	
	MC1595			–	±1.0	±2.0	
T_A = 0 to +70°C	MC1495						
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)			E_{RX}	–	±1.5	–	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)			E_{RY}	–	±3.0	–	
T_A = −55°C to +125°C	MC1595						
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)			E_{RX}	–	±0.75	–	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)			E_{RY}	–	±1.50	–	
Squaring Mode Error: Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment		5	E_{SQ}				%
T_A = +25°C	MC1495			–	±0.75	–	
	MC1595			–	±0.5	–	
T_A = 0 to +70°C	MC1495			–	±1.0	–	
T_A = −55°C to +125°C	MC1595			–	±0.75	–	
Scale Factor (Adjustable) $\left(K = \frac{2R_L}{I_3 R_X R_Y}\right)$		–	K	–	0.1	–	–
Input Resistance (f = 20 Hz)	MC1495	7	R_{INX}	–	20	–	MegOhms
	MC1595			–	35	–	
	MC1495		R_{INY}	–	20	–	
	MC1595			–	35	–	
Differential Output Resistance (f = 20 Hz)		8	R_o	–	300	–	k Ohms
Input Bias Current $I_{bx} = \frac{(I_9 + I_{12})}{2}, I_{by} = \frac{(I_4 + I_8)}{2}$	MC1495	6	I_{bx}	–	2.0	12	μA
	MC1595			–	2.0	8.0	
	MC1495		I_{by}	–	2.0	12	
	MC1595			–	2.0	8.0	
Input Offset Current $\lvert I_9 - I_{12} \rvert$	MC1495	6	$\lvert I_{iox} \rvert$	–	0.4	2.0	μA
	MC1595			–	0.2	1.0	
$\lvert I_4 - I_8 \rvert$	MC1495		$\lvert I_{ioy} \rvert$	–	0.4	2.0	
	MC1595			–	0.2	1.0	
Average Temperature Coefficient of Input Offset Current		6	$\lvert TC_{Iio} \rvert$				nA/°C
(T_A = 0 to +70°C)	MC1495			–	2.0	–	
(T_A = −55°C to +125°C)	MC1595			–	2.0	–	
Output Offset Current $\lvert I_{14} - I_2 \rvert$		6	$\lvert I_{oo} \rvert$				μA
	MC1495			–	20	100	
	MC1595			–	10	50	
Average Temperature Coefficient of Output Offset Current		6	$\lvert TC_{Ioo} \rvert$				nA/°C
(T_A = 0 to +70°C)	MC1495			–	20	–	
(T_A = −55°C to +125°C)	MC1595			–	20	–	
Frequency Response 3.0 dB Bandwidth, R_L = 11 kΩ		9,10	BW_{3dB}	–	3.0	–	MHz
3.0 dB Bandwidth, R_L = 50 Ω (Transconductance Bandwidth)			T_{BW3dB}	–	80	–	MHz
3° Relative Phase Shift Between V_X and V_Y			f_ϕ	–	750	–	kHz
1% Absolute Error Due to Input-Output Phase Shift			f_θ	–	30	–	kHz
Common Mode Input Swing (Either Input)		11	CMV				Vdc
	MC1495			±10.5	±12	–	
	MC1595			±11.5	±13	–	
Common Mode Gain (Either Input)		11	A_{CM}				dB
	MC1495			-40	-50	–	
	MC1595			-50	-60	–	
Common Mode Quiescent Output Voltage		12	V_{o1}	–	21	–	Vdc
			V_{o2}	–	21	–	
Differential Output Voltage Swing Capability		9	V_o	–	±14	–	V_{peak}
Power Supply Sensitivity		12	S^+	–	5.0	–	mV/V
			S^-	–	10	–	
Power Supply Current		12	I_7	–	6.0	7.0	mA
DC Power Dissipation		12	P_D	–	135	170	mW

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MC1545 MC1445

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

. . . designed for use as a general-purpose gated wideband-amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier. See Application Notes AN475 and AN491 for design details.

- Large Bandwidth; 75 MHz typical
- Channel-Select Time of 20 ns typical
- Differential Inputs and Differential Output

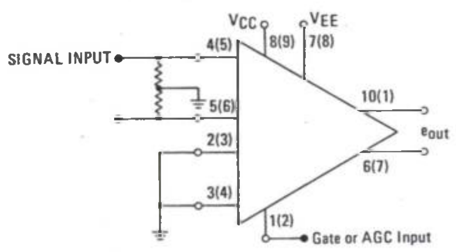
GATE CONTROLLED
TWO-CHANNEL-INPUT
WIDEBAND AMPLIFIER

MONOLITHIC SILICON
EPITAXIAL PASSIVATED

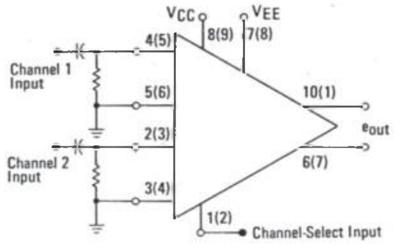
OCTOBER 1971 – DS 9125 R1

TYPICAL APPLICATIONS

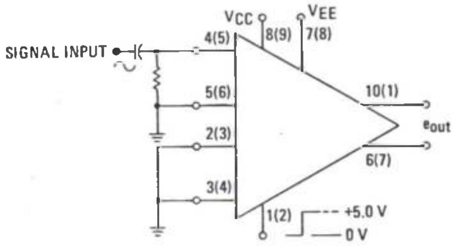
VIDEO SWITCH OR DIFFERENTIAL AMPLIFIER WITH AGC



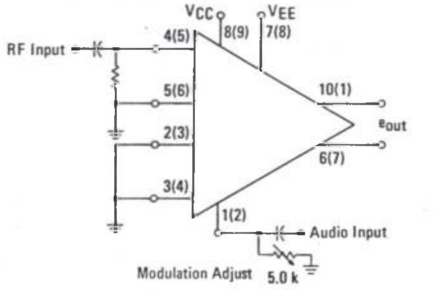
MULTIPLEX OR FSK



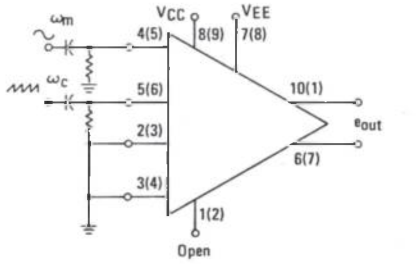
ANALOG SWITCH



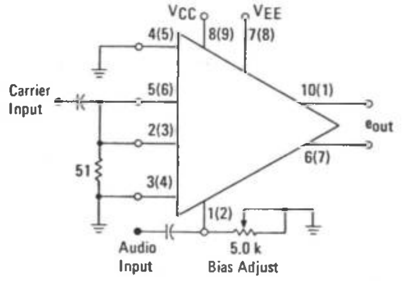
AMPLITUDE MODULATOR



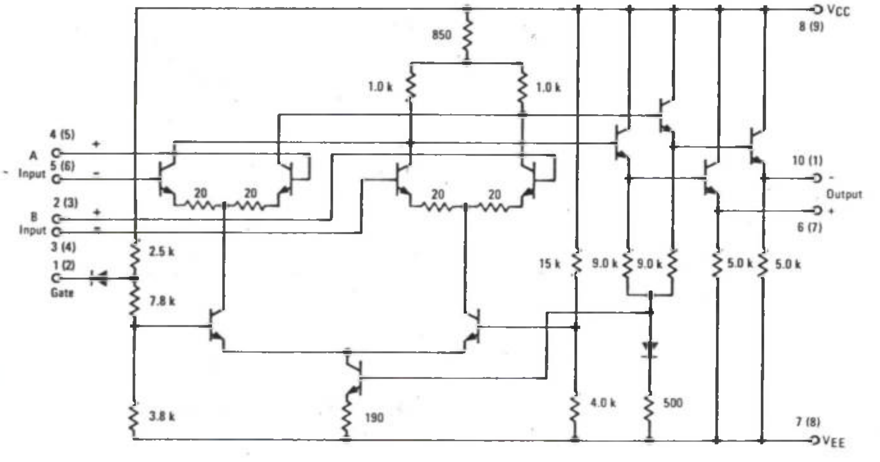
PULSE-WIDTH MODULATOR



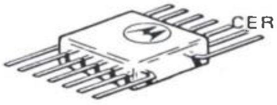
BALANCED MODULATOR



CIRCUIT SCHEMATIC

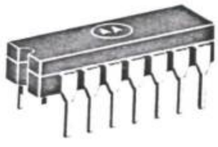


Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.



F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86

G SUFFIX
METAL PACKAGE
CASE 602A



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+12 −12	Vdc Vdc
Differential Input Signal	V_{ID}	±5.0	Volts
Load Current	I_L	25	mA
Power Dissipation (Package Limitation)	P_D		
Flat Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Ceramic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Operating Temperature Range MC1445 MC1545	T_A	0 to +75 −55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = 5.0 Vdc, at T_A = +25°C, specifications apply to both input channels unless otherwise noted)

Characteristic		Fig. No.	Symbol*	Min	Typ	Max	Unit
Single-Ended Voltage Gain	MC1445 MC1545	1, 12	A_{vs}	16 16	19 18	22 20	dB
Bandwidth	MC1445 MC1545	1, 12	BW	— 50	75 75	— —	MHz
Input Impedance (f = 50 kHz)	MC1445 MC1545	5, 14	z_{is}	3.0 4.0	10 10	— —	k ohms
Output Impedance (f = 50 kHz)		6, 15	z_{os}	—	25	—	Ohms
Output Voltage Swing (R_L = 1.0 k ohm, f = 50 kHz)		4, 13	V_{OD}	1.5	2.5	—	V_{p-p}
Input Bias Current ($I_{IB} = (I_1 + I_2)/2$)	MC1445 MC1545	16	I_{IB}	— —	15 15	30 25	µAdc
Input Offset Current		16	$\lvert I_{IO}\rvert$	—	2.0	—	µAdc
Input Offset Voltage	MC1445 MC1545	17	$\lvert V_{IO}\rvert$	— —	— 1.0	7.5 5.0	mVdc
Quiescent Output dc Level		17	V_O	—	0.2	—	Vdc
Output dc Level Change (Gate Voltage Change: +5.0 V to 0 V)		17	$\lvert \Delta V_O \rvert$	—	15	—	mV
Common-Mode Rejection Ratio (f = 50 kHz)		9, 18	CMRR	—	85	—	dB
Input Common-Mode Voltage Swing		18	V_{ICR}	—	±2.5	—	V_p
Gate Characteristics		8					Vdc
Gate Voltage Low (See Note 1)	MC1445 MC1545		V_{GOL}	0.20 0.45	0.40 0.70	— —	
Gate Voltage High (See Note 2)	MC1445 MC1545		V_{GOH}	— —	1.3 1.5	3.0 2.2	
Gate Current Low (Gate Voltage = 0 V)	MC1445 MC1545	18	I_{GOL}	— —	— —	4.0 2.5	mA
Gate Current High (Gate Voltage = +5.0 V)	MC1445 MC1545	18	I_{GOH}	— —	— —	4.0 2.0	µA
Step Response (e_{in} = 20 mV)	MC1445 MC1545	19	t_{PLH}	— —	6.5 6.5	— 10	ns
	MC1445 MC1545		t_{PHL}	— —	6.3 6.3	— 10	
	MC1445 MC1545		t_r	— —	6.5 6.5	— 10	
	MC1445 MC1545		t_f	— —	7.0 7.0	— 10	
Wideband Input Noise (5.0 Hz – 10 MHz, R_S = 50 ohms)		10, 20	$V_{N(in)}$	—	25	—	µV(rms)
DC Power Dissipation	MC1445 MC1545	11, 20	P_D	— —	70 70	150 110	mW

Note 1 V_{GOL} is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.
Note 2 V_{GOH} is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.
*Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

FIGURE 13 – OUTPUT VOLTAGE SWING TEST CIRCUIT

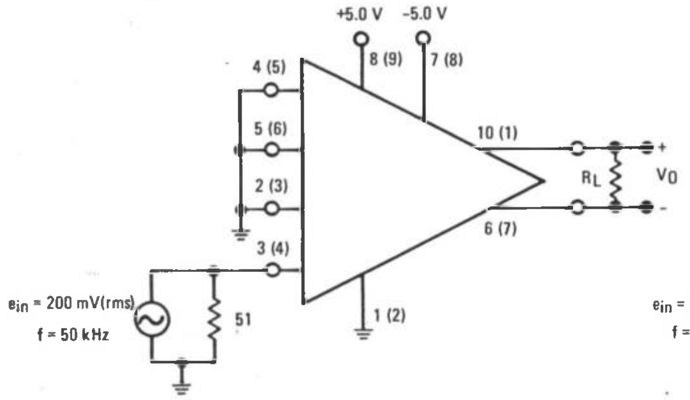


FIGURE 14 – INPUT IMPEDANCE TEST CIRCUIT

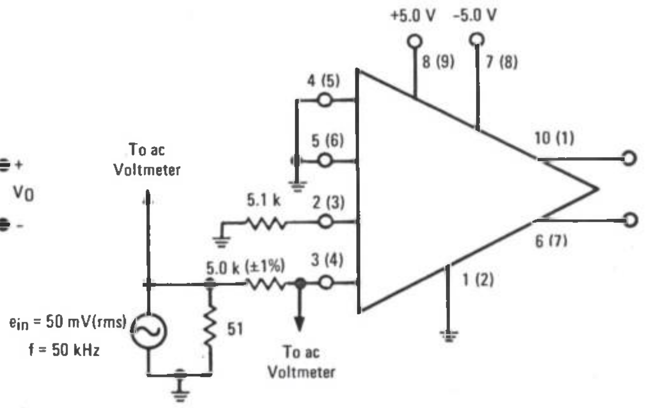


FIGURE 15 – OUTPUT IMPEDANCE TEST CIRCUIT

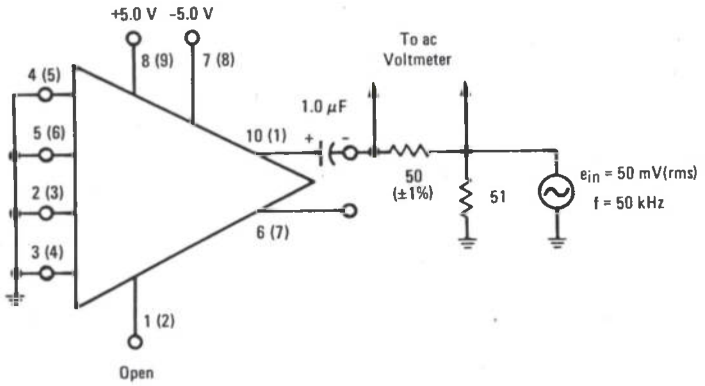
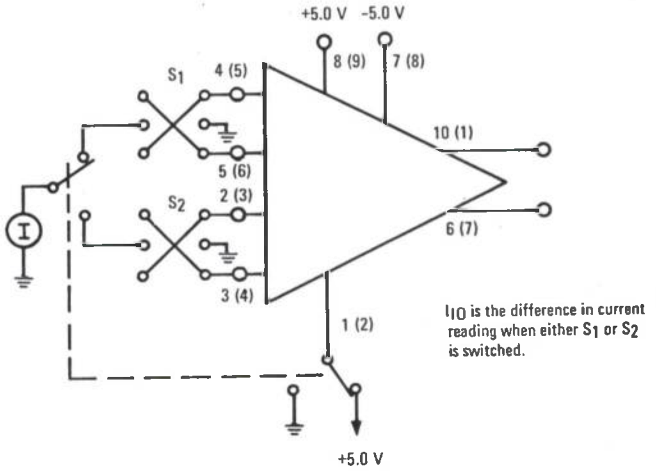
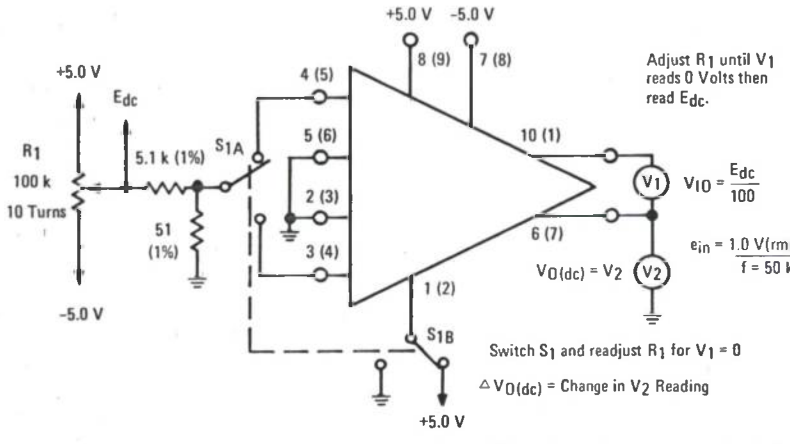


FIGURE 16 – INPUT BIAS CURRENT AND INPUT OFFSET CURRENT TEST CIRCUIT



I_{IO} is the difference in current reading when either S_1 or S_2 is switched.

FIGURE 17 – INPUT OFFSET VOLTAGE AND QUIESCENT OUTPUT LEVEL TEST CIRCUIT



Adjust R_1 until V_1 reads 0 Volts then read E_{dc}.

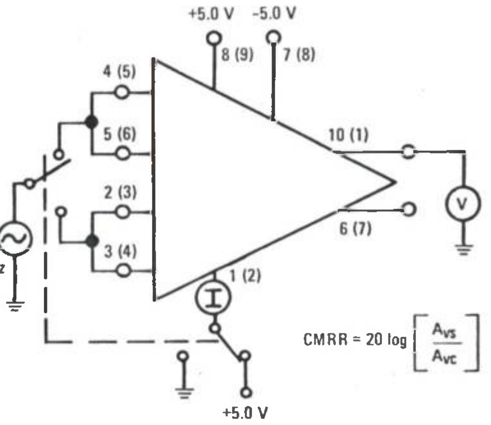
$V_{IO} = \frac{E_{dc}}{100}$

$V_{O(dc)} = V_2$

Switch S_1 and readjust R_1 for $V_1 = 0$

$\Delta V_{O(dc)}$ = Change in V_2 Reading

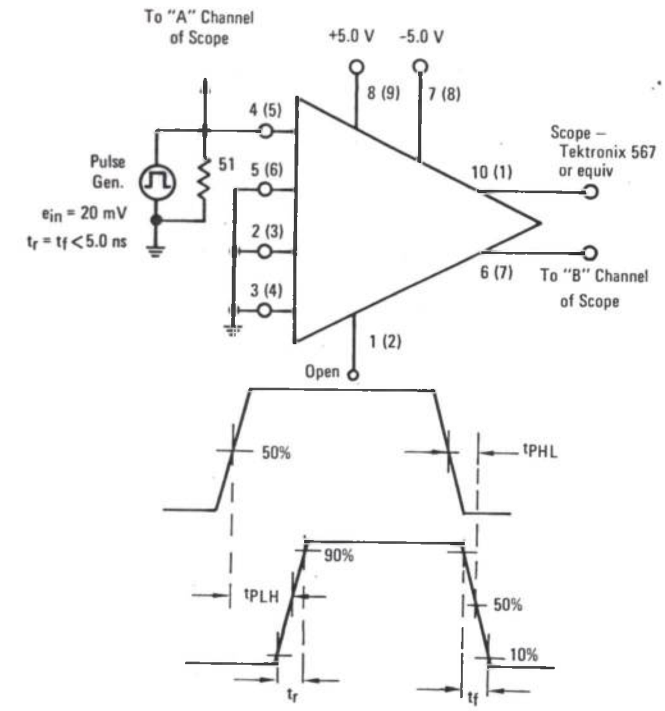
FIGURE 18 – GATE CURRENT (HIGH AND LOW), COMMON-MODE REJECTION AND COMMON-MODE INPUT RANGE TEST CIRCUIT



$\text{CMRR} = 20 \log \left[\frac{A_{vs}}{A_{vc}}\right]$

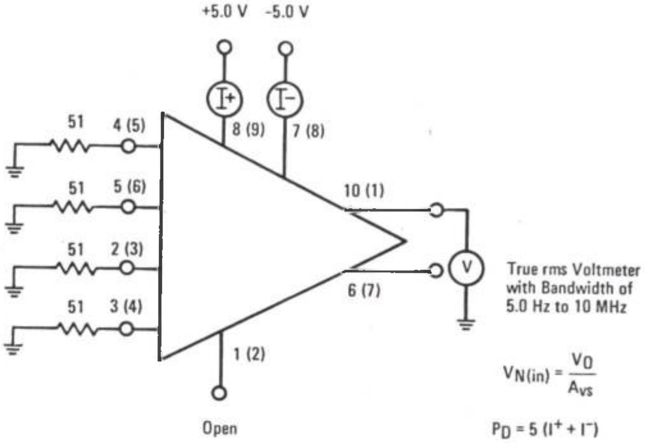
Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.

FIGURE 19 – PROPAGATION DELAY AND RISE AND FALL TIMES TEST CIRCUIT



Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.

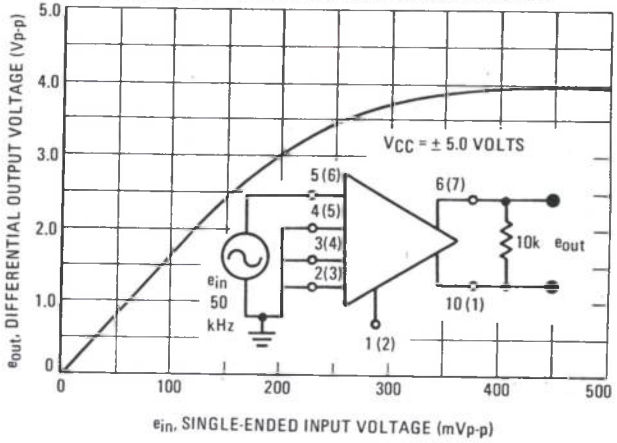
FIGURE 20 – POWER DISSIPATION AND WIDEBAND INPUT NOISE TEST CIRCUIT



$V_{N(in)} = \frac{V_O}{A_{vs}}$

$P_D = 5\,(I^+ + I^-)$

FIGURE 21 – LIMITING CHARACTERISTIC

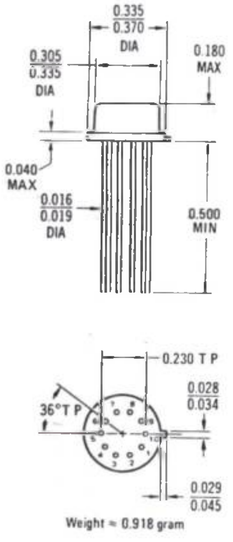


CASE OUTLINES

G SUFFIX

METAL PACKAGE

CASE 602A



Weight ≈ 0.918 gram

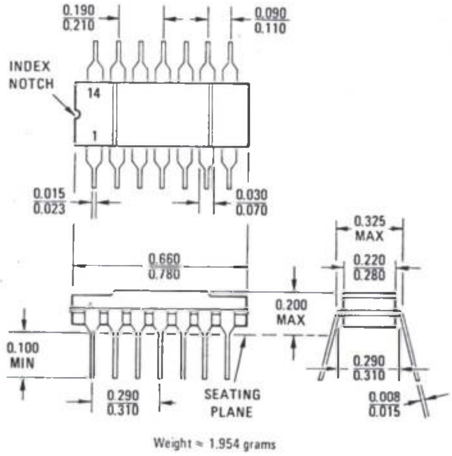
Pin 7 connected to case

L SUFFIX

CERAMIC PACKAGE

CASE 632

TO-116



Weight ≈ 1.954 grams

All JEDEC TO-116 dimensions and notes apply.

① This dimension is measured from the lead centers at the seating plane.

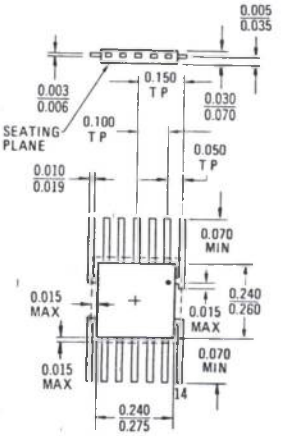
② Orientation will be indicated either by mechanical index point or notch in pin 1 as shown.

F SUFFIX

CERAMIC PACKAGE

CASE 607

TO-86



Lead 1 identified by color dot or by elbow on lead.

All JEDEC dimensions and notes apply

Weight ≈ 0.218 Gram

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

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4583-1 PRINTED IN USA 10-71 IMPERIAL LITHO B25251 10M

TYPES TIP29, TIP29A, TIP29B, TIP29C
N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

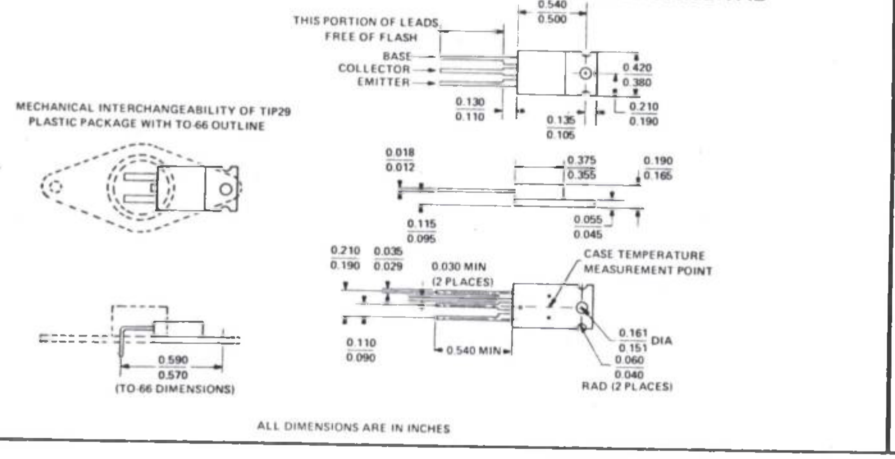
TYPES TIP29, TIP29A, TIP29B, TIP29C
BULLETIN NO. DL-S 7011371, OCTOBER 1970
REPLACES BULLETIN NO. DL-S 6810954, JULY 1968

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS DESIGNED FOR COMPLEMENTARY USE WITH TIP30, TIP30A, TIP30B, TIP30C

- 30 W at 25°C Case Temperature
- 1 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 200 mA

mechanical data

THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE MOUNTING TAB



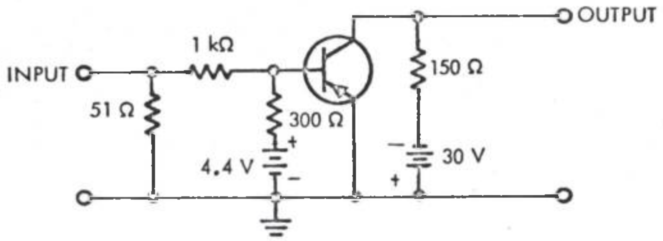
ALL DIMENSIONS ARE IN INCHES

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

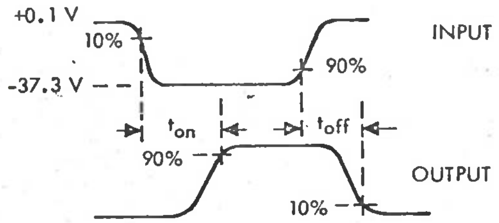
	TIP29	TIP29A	TIP29B	TIP29C
Collector-Base Voltage	40 V	60 V	80 V	100 V
Collector-Emitter Voltage (See Note 1)	40 V	60 V	80 V	100 V
Emitter-Base Voltage	← 5 V →			
Continuous Collector Current	← 1 A →			
Peak Collector Current (See Note 2)	← 3 A →			
Continuous Base Current	← 0.4 A →			
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 5 →			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 30 W →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 2 W →			
Unclamped Inductive Load Energy (See Note 5)	← 32 mJ →			
Operating Collector Junction Temperature Range	← −65°C to 150°C →			
Storage Temperature Range	← −65°C to 150°C →			
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →			

NOTES:
1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
3. Derate linearly to 150°C case temperature at the rate of 0.24 W/°C.
4. Derate linearly to 150°C free-air temperature at the rate of 16 mW/°C.
5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB1} = 100\ \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1\ \Omega$, $V_{CC} = 10$ V. Energy $\approx I_C{}^2L/2$.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

NOTES: a. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50\ \Omega$, $t_p = 10\ \mu s$, duty cycle $\leq 2\%$.

b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10\ M\Omega$, $C_{in} \leq 11.5$ pF.

c. Resistors must be noninductive types.

d. The d-c power supplies may require additional bypassing in order to minimize ringing.

MAXIMUM SAFE OPERATING REGION

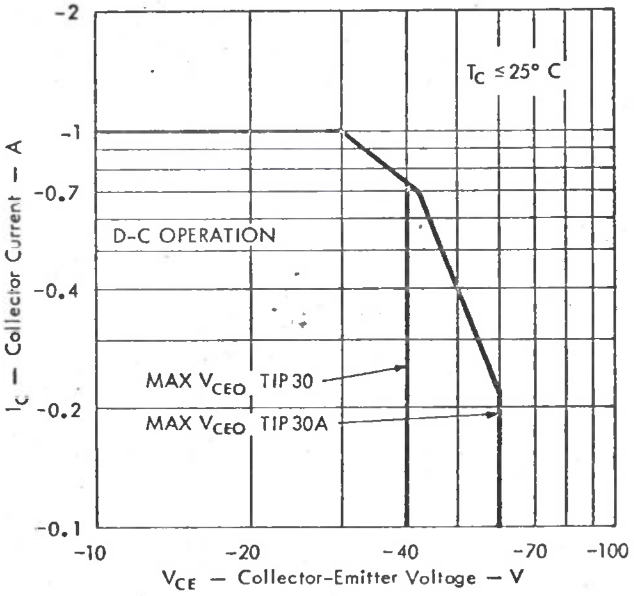
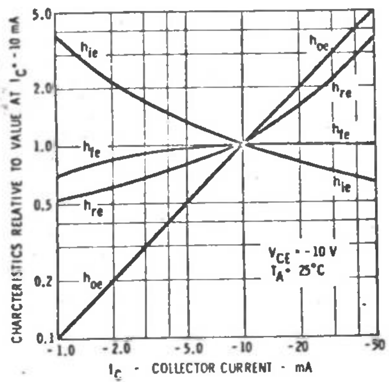
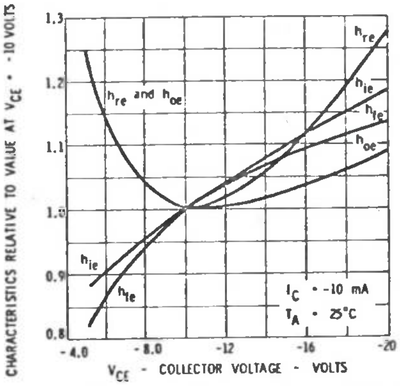
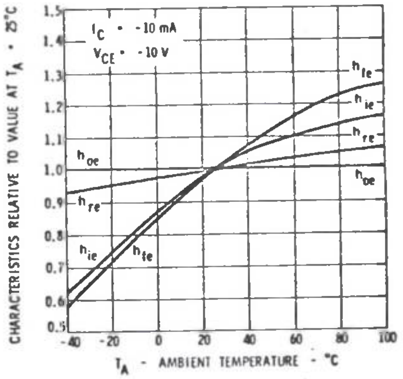


FIGURE 2

SMALL SIGNAL CHARACTERISTICS





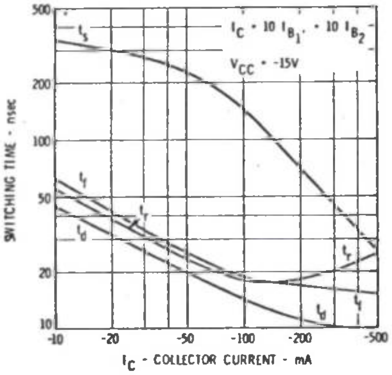


h PARAMETERS (f = 1 kc)

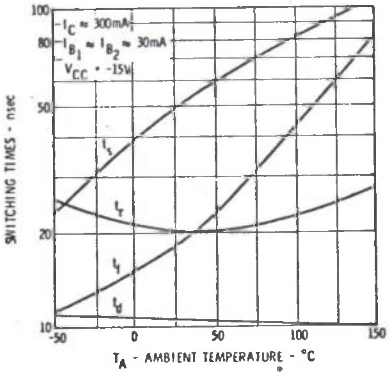
Symbol		Min.	Typ.	Max.	Units	Test Conditions
h_{ie}	Input Resistance		480	2000	ohms	I_C = 10 mA V_{CE} = -10 V
h_{oe}	Output Conductance		80	1200	µmhos	I_C = 10 mA V_{CE} = -10 V
h_{re}	Voltage Feedback Ratio		162	1500	$x10^{-6}$	I_C = 10 mA V_{CE} = -10 V
h_{fe}	Small Signal Current Gain	100				I_C = 10 mA V_{CE} = -10 V

TYPICAL ELECTRICAL CHARACTERISTICS

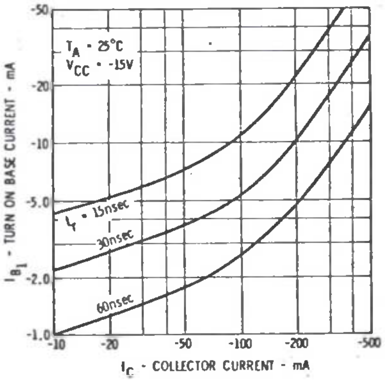
SWITCHING TIMES VERSUS COLLECTOR CURRENT



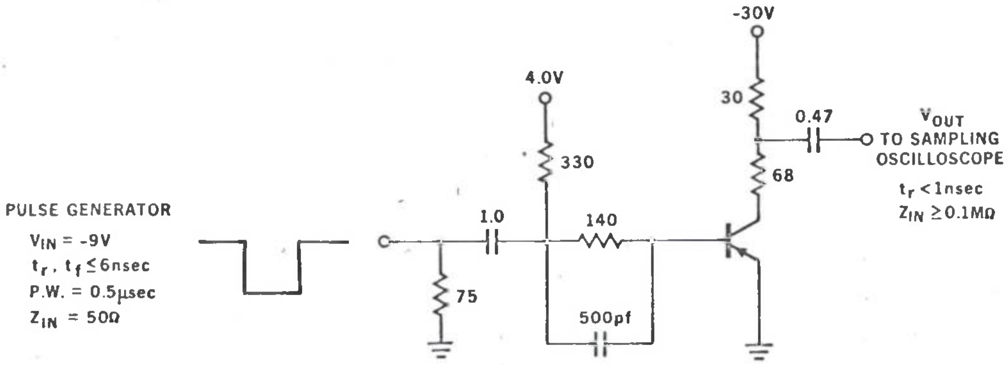
SWITCHING TIMES VERSUS AMBIENT TEMPERATURE



RISE TIME VERSUS COLLECTOR AND TURN ON BASE CURRENTS



T_{ON} AND T_{OFF} TEST CIRCUIT



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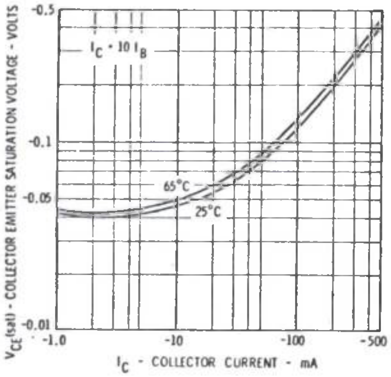
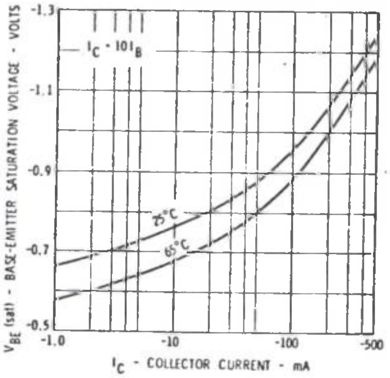
TYPICAL ELECTRICAL CHARACTERISTICS

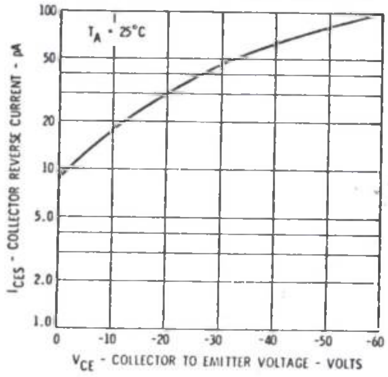
PULSED COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



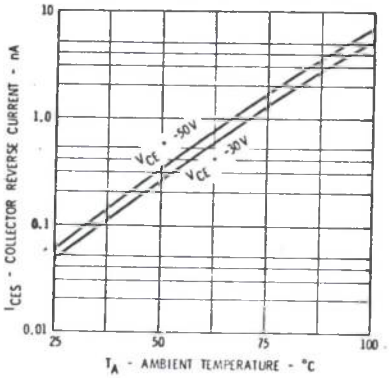
PULSED BASE SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



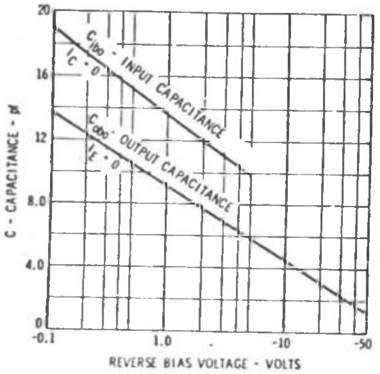
COLLECTOR REVERSE CURRENT VERSUS REVERSE BIAS VOLTAGE



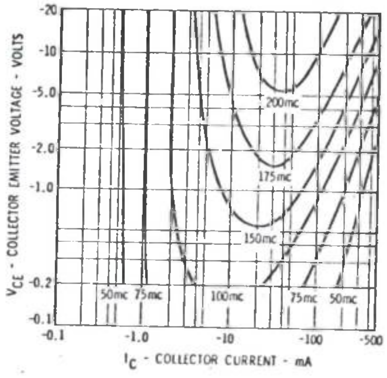
COLLECTOR REVERSE CURRENT VERSUS AMBIENT TEMPERATURE



INPUT AND OUTPUT CAPACITANCES VERSUS REVERSE BIAS VOLTAGE



CONTOURS OF CONSTANT GAIN BANDWIDTH PRODUCT (f_T)

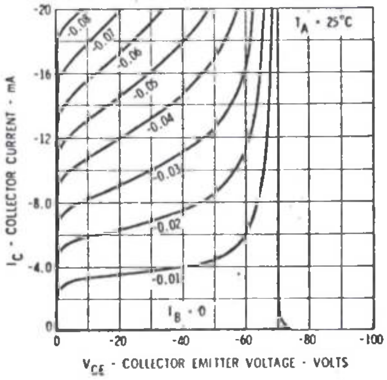


ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

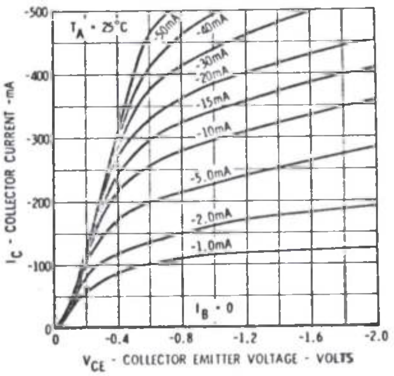
SYMBOL	CHARACTERISTIC		MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{CE}(sat)	Collector Saturation Voltage (Pulsed, see Note 5)			-0.08	-0.25	Volts	I_C = 50 mA I_B = 2.5 mA
V_{CE}(sat)	Collector Saturation Voltage (Pulsed, see Note 5)			-0.18	-0.4	Volts	I_C = 150 mA I_B = 15 mA
V_{CE}(sat)	Collector Saturation Voltage (Pulsed, see Note 5)			-0.5	-1.0	Volts	I_C = 300 mA I_B = 30 mA
V_{CEO}(sust)	Collector to Emitter Sustaining Voltage (Notes 4 & 5)	2N3645 2N3644	-60 -45			Volts Volts	I_C = 10 mA I_B = 0 (pulsed)
V_{BE}(sat)	Base Saturation Voltage (Pulsed, see Note 5)			-0.9	-1.0	Volts	I_C = 50 mA I_B = 2.5 mA
V_{BE}(sat)	Base Saturation Voltage (Pulsed, see Note 5)			-1.0	-1.3	Volts	I_C = 150 mA I_B = 15 mA
V_{BE}(sat)	Base Saturation Voltage (Pulsed, see Note 5)		-0.8		-2.0	Volts	I_C = 300 mA I_B = 30 mA
BV_{EBO}	Emitter to Base Breakdown Voltage		-5.0			Volts	I_C = 0 I_E = 10 μA
BV_{CBO}	Collector to Base Breakdown Voltage	2N3645 2N3644	-60 -45			Volts Volts	I_C = 100 μA I_E = 0
t_{on}	Turn On Time (Note 6)			30	40	nsec	$I_C \approx$ 300 mA $I_{B1} \approx$ 30 mA
t_{off}	Turn Off Time (Note 6)			65	100	nsec	$I_C \approx$ 300 mA, $I_{B1} \approx$ 30 mA, $I_{B2} \approx$ -30 mA
I_{CES}	Collector Reverse Current	2N3645			35	nA	V_{CE} = -50 V V_{BE} = 0
		2N3644			35	nA	V_{CE} = -30 V V_{BE} = 0
I_{CES}	Collector Reverse Current (+65°C)	2N3645			2.0	μA	V_{CE} = -50 V V_{BE} = 0
		2N3644			2.0	μA	V_{CE} = -30 V V_{BE} = 0

TYPICAL ELECTRICAL CHARACTERISTICS

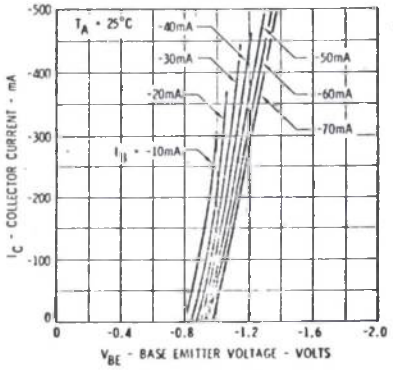
COLLECTOR CHARACTERISTICS *



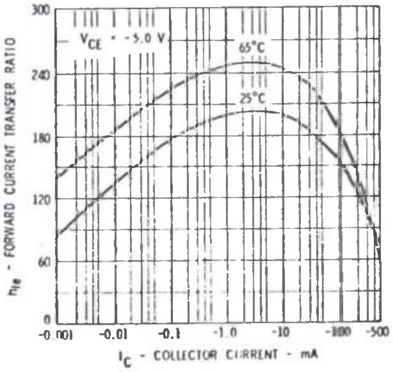
COLLECTOR CHARACTERISTICS*



BASE CHARACTERISTICS *



DC PULSED CURRENT GAIN VERSUS COLLECTOR CURRENT



* Single family characteristics on Transistor Curve Tracer.

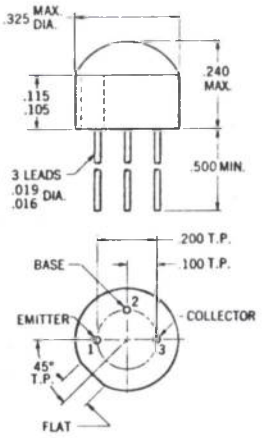
2N3644 · 2N3645

PNP HIGH CURRENT SWITCHES

DIFFUSED SILICON PLANAR EPITAXIAL TRANSISTORS

These PNP silicon PLANAR epitaxial transistors are designed for digital and analog applications at current levels up to 500 milliamperes. Their high beta, high f_T at high current and high LV_{CEO}, make them ideal for use as line drivers and memory applications.

PHYSICAL DIMENSIONS
Epoxy package
TO-105



NOTES: All dimensions in inches
Leads are gold plated kovar
Package is electrically Non conductive material
Package weight is 0.66 gram

ABSOLUTE MAXIMUM RATINGS [Note 1]

Maximum Temperatures

Storage Temperature	-55°C to +125°C
Operating Junction Temperature	+125°C Maximum
Lead Temperature (soldering, 10 sec time limit)	+260°C Maximum

Maximum Power Dissipation		2N3645	2N3644
Total Dissipation	at 25°C Case Temperature (Notes 2 & 3)	0.7 Watt	0.7 Watt
	at 25°C Free Air Temperature (Notes 2 & 3)	0.3 Watt	0.3 Watt

Maximum Voltages

V_{CBO}	Collector to base Voltage	-60 Volts	-45 Volts
V_{CEO}	Collector to Emitter Voltage (Note 4)	-60 Volts	-45 Volts
V_{EBO}	Emitter to Base Voltage	-5.0 Volts	-5.0 Volts

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
h_{FE}	DC Current Gain	40	170			I_C = 100 µA V_{CE} = -10 V
h_{FE}	DC Current Gain	80	200			I_C = 1.0 mA V_{CE} = -10 V
h_{FE}	DC Pulse Current Gain (Note 5)	100	270			I_C = 10 mA V_{CE} = -10 V
h_{FE}	DC Pulse Current Gain (Note 5)	115	160	300		I_C = 50 mA V_{CE} = -1.0 V
h_{FE}	DC Pulse Current Gain (Note 5)	100	150	300		I_C = 150 mA V_{CE} = -10 V
h_{FE}	DC Pulse Current Gain (Note 5)	20	50			I_C = 300 mA V_{CE} = -2.0 V
h_{fe}	High Frequency Current Gain (f = 100 Mc)	2.0	2.50			I_C = 20 mA V_{CE} = -20 V
C_{obo}	Common Base Output Capacitance		4.5	8.0	pf	I_E = 0 V_{CB} = -10 V
C_{ibo}	Common Base Input Capacitance		15	25	pf	I_C = 0 V_{EB} = -0.5 V

Additional Electrical Characteristics on page 2

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 125°C and junction-to-case thermal resistance of 143°C/Watt (derating factor of 7.0 mW/°C); junction-to-ambient thermal resistance of 333°C/Watt (derating factor of 3.0 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300 µsec; duty cycle = 1%.

(6) See switching circuit for exact values of I_C, I_{B1}, and I_{B2}.

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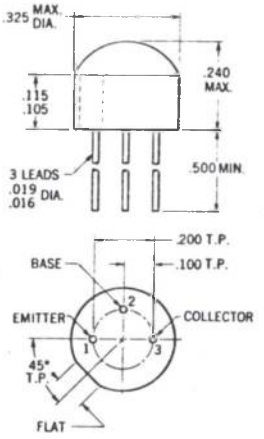
2N3567 · 2N3568

NPN GENERAL PURPOSE TYPES

DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

The 2N3567 and 2N3568 are NPN silicon PLANAR*epitaxial transistors designed primarily for amplifier and switching applications over a wide range of voltage and current. These devices feature a useful beta range to 500 mA and low saturation voltage. High collector-to-emitter voltage allows operation to 60 volts for the 2N3568 and 40 volts for the 2N3567.

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-105) outline



NOTES: All dimensions in inches
Leads are gold plated kovar
Package is electrically Non-conductive material
Package weight is 0.66 gram

ABSOLUTE MAXIMUM RATINGS [Note 1]

Maximum Temperatures

Storage Temperature	-55°C to +125°C
Operating Junction Temperature	+125°C Maximum
Lead Temperature (Soldering, 10 sec. time limit)	+260°C Maximum

Maximum Power Dissipation

Total Dissipation at 25°C Case Temperature (Notes 2 & 3)	0.8 Watt
at 25°C Ambient Temperature (Notes 2 & 3)	0.3 Watt

Maximum Voltages

		2N3567	2N3568
V_{CBO}	Collector to Base Voltage	80 Volts	80 Volts
V_{CEO}	Collector to Emitter Voltage (Note 4)	40 Volts	60 Volts
V_{EBO}	Emitter to Base Voltage	5.0 Volts	5.0 Volts

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Characteristic		2N3567 Min.	2N3567 Typ.	2N3567 Max.	2N3568 Min.	2N3568 Typ.	2N3568 Max.	Units	Test Conditions	
h_{FE}	DC Pulse Current Gain	(Note 5)	40	80	120	40	80	120		I_C = 150 mA	V_{CE} = 1.0 V
h_{FE}	DC Pulse Current Gain	(Note 5)	40			40				I_C = 30 mA	V_{CE} = 1.0 V
$V_{CE}(sat)$	Collector Saturation Voltage (pulsed, see note 5)			0.15	0.25		0.15	0.25	Volts	I_C = 150 mA	I_B = 15 mA
$V_{BE}(sat)$	Base Saturation Voltage (pulsed, see note 5)			0.9	1.1		0.9	1.1	Volts	I_C = 150 mA	I_B = 15 mA
h_{fe}	High Frequency Current Gain (f = 20 MHz)		3.0			3.0				I_C = 50 mA	V_{CE} = 10 V
C_{obo}	Open Circuit Output Capacitance			13	20		13	20	pF	I_E = 0	V_{CB} = 10 V
C_{ibo}	Open Circuit Input Capacitance			63	80		63	80	pF	I_C = 0	V_{EB} = 0.5 V
I_{CBO}	Collector Cutoff Current				50			50	nA	I_E = 0	V_{CB} = 40 V
$I_{CBO}(75°C)$	Collector Cutoff Current				5.0			5.0	µA	I_E = 0	V_{CB} = 40 V
I_{EBO}	Emitter Cutoff Current				25			25	nA	I_C = 0	V_{EB} = 4.0 V
BV_{CBO}	Collector to Base Breakdown Voltage		80			80			Volts	I_E = 0	I_C = 100 µA
$V_{CEO}(sust)$	Collector to Emitter Sustaining Voltage (Notes 4 and 5)		40			60			Volts	I_C = 30 mA (pulsed)	I_B = 0
BV_{EBO}	Emitter to Base Breakdown Voltage		5.0			5.0			Volts	I_C = 0	I_E = 10 µA

* Planar is a patented Fairchild process.

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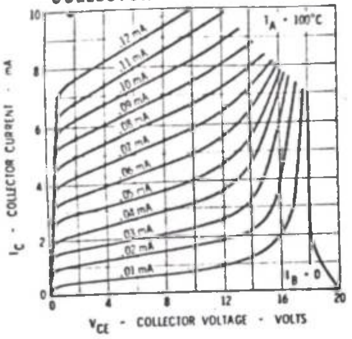
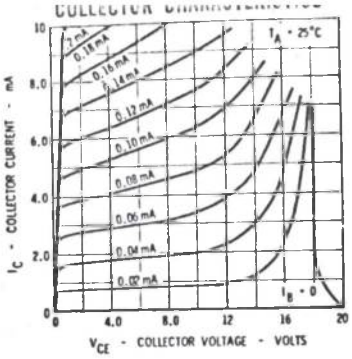
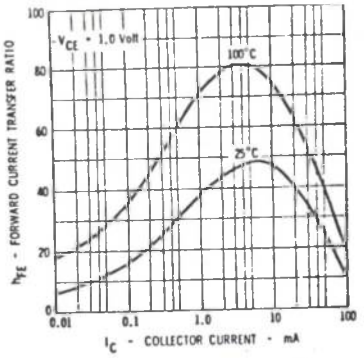
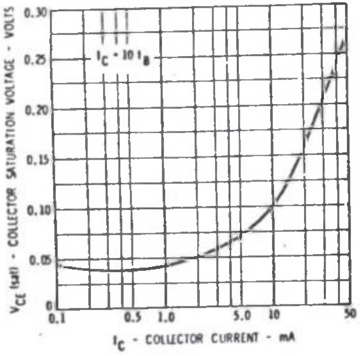
COLLECTOR CHARACTERISTICS*



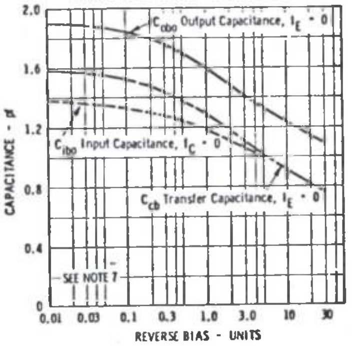




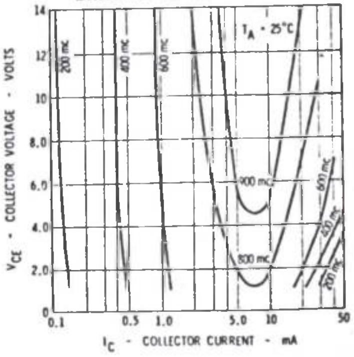
COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



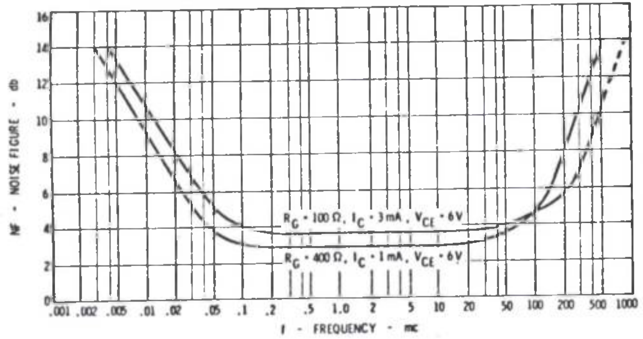
CAPACITANCE VERSUS REVERSE BIAS VOLTAGE



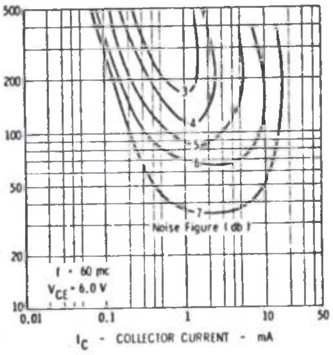
CONTOURS OF CONSTANT BANDWIDTH PRODUCT (f_T)



NOISE FIGURE VERSUS FREQUENCY

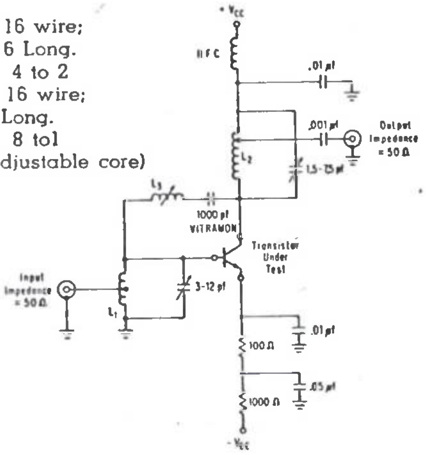


CONTOURS OF CONSTANT NOISE FIGURE

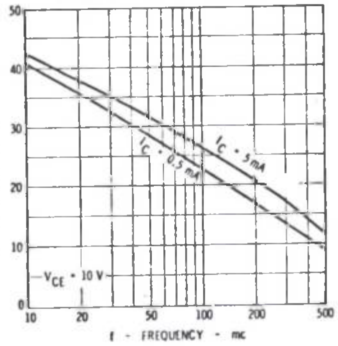


NEUTRALIZED 200 MC POWER GAIN AMPLIFIER TEST CIRCUIT

L_1 — 3.5 Turns No. 16 wire;
5/16 Dia; 7/16 Long.
Turns Ratio 4 to 2
L_2 — 8.0 Turns No. 16 wire;
1/8 Dia; 7/8 Long.
Turns Ratio 8 tol
L_3 — 0.4-0.65 μh (adjustable core)



MAXIMUM AVAILABLE GAIN VERSUS FREQUENCY



* Single family characteristics on Transistor Curve Tracer.

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These ratings give a maximum junction temperature of 125°C and junction-to-case thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C); junction-to-ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).

(3) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(4) Pulse Conditions: length = 300 μsec; duty cycle ≤ 1%.

(5) Forward gain (db) + reverse gain (db) < (-20 db). See test circuit.

(6) f = 60 mc; R_S = 400 Ω.

(7) C_{cb} is measured using a three-terminal measurement technique with case and emitter guarded. C_{cb} is equivalent to C_{re}.

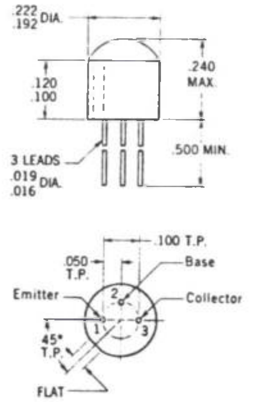
2N3563

NPN LOW LEVEL RF AMPLIFIER

DIFFUSED SILICON PLANAR EPITAXIAL TRANSISTOR

The 2N3563 is an NPN silicon PLANAR epitaxial transistor designed for low-level RF applications. It features high power gain, low noise and low leakage in a new solid package designed to give maximum mechanical support to the transistor chip.

PHYSICAL DIMENSIONS
Epoxy package
TO-106



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram. Package is electrically non-conductive material

ABSOLUTE MAXIMUM RATINGS [Note 1]

Maximum Temperatures

Operating Junction Temperature	+125°C Maximum
Storage Temperature	-55°C to +125°C
Soldering Temperature (10 sec. time limit)	+260°C Maximum

Maximum Power Dissipation

Total Dissipation at 25°C Case Temperature	(Note 2)	0.5 Watt
at 65°C Case Temperature	(Note 2)	0.3 Watt
at 25°C Ambient Temperature	(Note 2)	0.2 Watt

Maximum Voltages

V_{CBO}	Collector to Base Voltage		30 Volts
V_{CEO}	Collector to Emitter Voltage	(Note 3)	12 Volts
V_{EBO}	Emitter to Base Voltage		2.0 Volts

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Characteristics		Min.	Typ.	Max.	Units	Test Conditions	
h_{FE}	DC Pulse Current Gain	(Note 4)	20	50	200		I_C = 8.0 mA	V_{CE} = 10 V
V_{CE}(sat)	Collector Saturation Voltage			0.1		Volts	I_C = 10 mA	I_B = 1.0 mA
C_{obo}	Open Circuit Output Capacitance			1.3	1.7	pf	I_E = 0	V_{CB} = 10 V
C_{cb}	Collector-base Transfer	(Note 7)		0.8		pf	I_E = 0	V_{CB} = 10 V
I_{CBO}	Collector Cutoff Current				50	nA	I_E = 0	V_{CB} = 15 V
I_{CBO}(65°C)	Collector Cutoff Current				5.0	μA	I_E = 0	V_{CB} = 15 V
h_{fe}	High Frequency Current Gain (f = 100 mc)		6.0	9.0			I_C = 8.0 mA	V_{CE} = 10 V
G_{pe}	Available Power Gain (neutralized) (f = 200 mc)	(Note 5)	14	17		db	I_C = 8.0 mA	V_{CE} = 10 V
NF	Noise Figure	(Note 6)		4.0		db	I_C = 1.0 mA	V_{CE} = 6.0 V
$r_b'C_c$	Collector-Base Time Constant (f = 79.8 mc)		8.0	15	25	psec	I_C = 8.0 mA	V_{CB} = 10 V
h_{fe}	Small Signal Current Gain (f = 1.0 Kc)		20		250		I_C = 8.0 mA	V_{CE} = 10 V
BV_{CBO}	Collector to Base Breakdown Voltage		30			Volts	I_E = 0	I_C = 100 μA
V_{CEO}(sust)	Collector to Emitter Sustaining Voltage (Notes 3 and 4)		12			Volts	I_C = 3.0 mA (pulsed)	I_B = 0
BV_{EBO}	Emitter to Base Breakdown Voltage		2.0			Volts	I_C = 0	I_E = 10 μA

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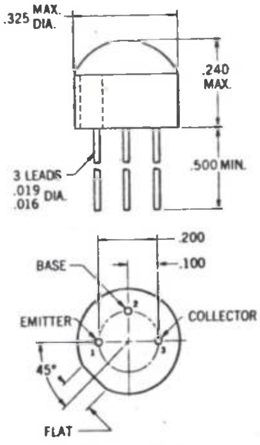
2N4354 • 2N4355 • 2N4356
PNP LOW LEVEL, LOW NOISE AMPLIFIERS AND HIGH CURRENT SWITCHES
DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

- HIGH BREAKDOWN . . . . −60 AND −80 VOLT (MIN) LV_{CEO}
- EXCELLENT BETA LINEARITY . . . FROM 100 μA TO 500 mA
- LOW NOISE FIGURE . . . . 3 dB (MAX) AT 1.0 kHz
- LOW $V_{CE(sat)}$ . . . . 1.0 VOLT (MAX) AT $I_C = 1.0$ A
- COMPLEMENTARY WITH 2N3567, 2N3568, 2N3569

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-105) outline



NOTES All dimensions in inches
Leads are gold-plated kovar
Package is electrically Non-conductive material
Package weight is 0.66 gram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures			
Storage Temperature			−55°C to +125°C
Operating Junction Temperature			125°C
Lead Temperature (Soldering, 10 second time limit)			260°C
Maximum Power Dissipation (Notes 2 and 3)			
Total Dissipation at 25°C Case Temperature			0.8 Watt
at 25°C Ambient Temperature			0.35 Watt
Maximum Voltages		2N4354 2N4355	2N4356
V_{CBO}	Collector to Base Voltage	−60 Volts	−80 Volts
V_{CEO}	Collector to Emitter Voltage (Note 4)	−60 Volts	−80 Volts
V_{EBO}	Emitter to Base Voltage	−5.0 Volts	−5.0 Volts

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N4354 MIN.	2N4354 TYP.	2N4354 MAX.	2N4355 MIN.	2N4355 TYP.	2N4355 MAX.	2N4356 MIN.	2N4356 TYP.	2N4356 MAX.	UNITS	TEST CONDITIONS
h_{FE}	DC Pulse Current Gain (Note 5)	25	110		60	180		25	160			$I_C = 100\ \mu A$ $V_{CE} = -10$ V
h_{FE}	DC Pulse Current Gain (Note 5)	40	120		75	200		40	180			$I_C = 1$ mA $V_{CE} = -10$ V
h_{FE}	DC Pulse Current Gain (Note 5)	50	120	500	100	200	400	50	180	250		$I_C = 10$ mA $V_{CE} = -10$ V
h_{FE}	DC Pulse Current Gain (Note 5)	40	115		75	190		40	170			$I_C = 100$ mA $V_{CE} = -10$ V
h_{FE}	DC Pulse Current Gain (Note 5)	30	110		75	170		30	160			$I_C = 500$ mA $V_{CE} = -10$ V
h_{fe}	High Frequency Current Gain (f = 100 MHz)	1.0	2.0	5.0	1.0	2.0	5.0	1.0	2.0	5.0		$I_C = 50$ mA $V_{CE} = -10$ V
BV_{CBO}	Collector to Base Breakdown Voltage	−60			−60			−80			Volts	$I_C = 10\ \mu A$ $I_E = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0			−5.0			−5.0			Volts	$I_C = 0$ $I_E = 10\ \mu A$
$V_{CEO(sus)}$	Collector to Emitter Sustaining Voltage (Notes 4 and 5)	−60			−60			−80			Volts	$I_C = 10$ mA $I_B = 0$ (pulsed)
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 5)					−0.5	−1.0				Volts	$I_C = 1.0$ A $I_B = 100$ mA
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 5)						−1.2				Volts	$I_C = 1.0$ A $I_B = 100$ mA
$V_{BE(ON)}$	Pulsed Base Emitter "ON" Voltage (Note 5)					−1.05	−1.20				Volts	$I_C = 1.0$ A $V_{CE} = -1.0$ V

*Planar is a patented Fairchild process.

NOTES:
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
(3) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 125°C/Watt (derating factor of 8.0 mW/°C); junction to ambient thermal resistance of 286°C/Watt (derating factor of 3.5 mW/°C).
(4) Rating refers to a high current point where collector to emitter voltage is lowest.
(5) Pulse Conditions: length = 300 μs; duty cycle = 1%.
(6) See switching circuit for exact values of I_C, I_{B1}, and I_{B2}.

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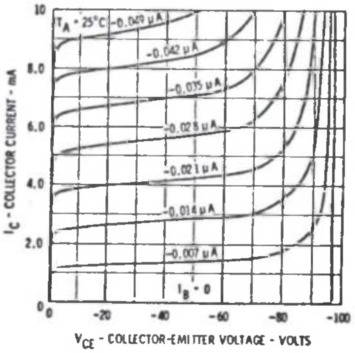
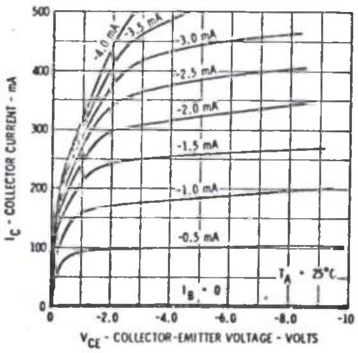
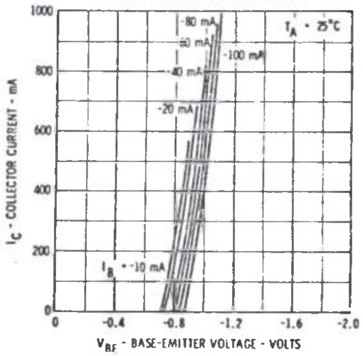
ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

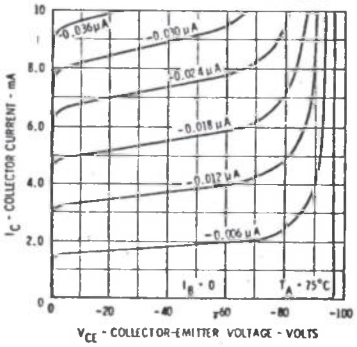
SYMBOL	CHARACTERISTIC	TYP.	MAX.	UNITS	TEST CONDITIONS	
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 5)	−0.10	−0.15	Volts	$I_C = 150$ mA	$I_B = 15$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 5)	−0.25	−0.5	Volts	$I_C = 500$ mA	$I_B = 50$ mA
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 5)	−0.8	−0.9	Volts	$I_C = 150$ mA	$I_B = 15$ mA
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 5)		−1.1	Volts	$I_C = 500$ mA	$I_B = 50$ mA
$V_{BE(ON)}$	Pulsed Base Emitter "ON" Voltage (Note 5)	−0.95	−1.1	Volts	$I_C = 500$ mA	$V_{CE} = -0.5$ V
I_{CBO}	Collector Cutoff Current	0.2	50	nA	$I_E = 0$	$V_{CB} = -50$ V
I_{CBO}(+75°C)	Collector Cutoff Current	0.02	5.0	μA	$I_E = 0$	$V_{CB} = -50$ V
I_{EBO}	Emitter to Base Current	1.0	100	nA	$I_C = 0$	$V_{EB} = -4.0$ V
C_{cb}	Collector to Base Capacitance (f = 1.0 MHz)	15	30	pF	$I_C = 0$	$V_{CB} = -10$ V
C_{eb}	Emitter to Base Capacitance (f = 1.0 MHz)	75	110	pF	$I_C = 0$	$V_{EB} = -0.5$ V
t_{on}	Turn-on Time (Note 6)	23	100	ns	$I_C \simeq 500$ mA	$I_{B1} \simeq 50$ mA
t_{off}	Turn-off Time (Note 6)	200	400	ns	$I_C \simeq 500$ mA $I_{B2} \simeq -50$ mA	$I_{B1} \simeq 50$ mA
NF	Noise Figure (f = 1.0 kHz)	1.0	3.0	dB	$I_C = 100$ μA $R_S = 1.0$ kΩ	$V_{CE} = -10$ V

TYPICAL ELECTRICAL CHARACTERISTICS


COLLECTOR CHARACTERISTICS•


COLLECTOR CHARACTERISTICS•


BASE CHARACTERISTICS•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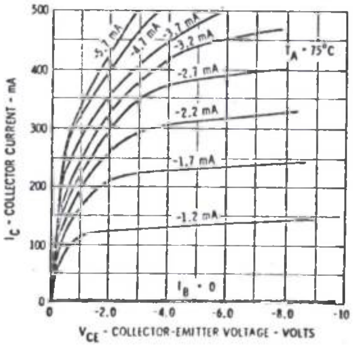
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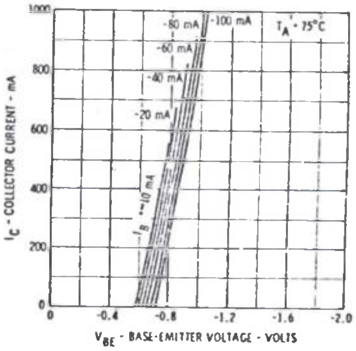
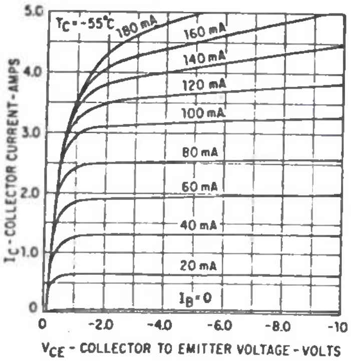

BASE CHARACTERISTICS•

•Single family characteristic on Transistor Curve Tracer.

TYPICAL ELECTRICAL CHARACTERISTICS

2N5003

COLLECTOR CHARACTERISTICS



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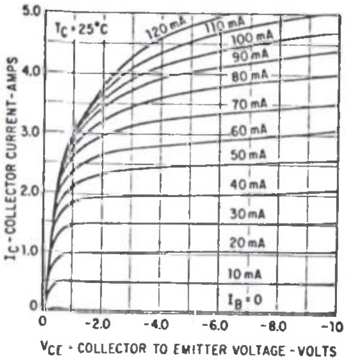

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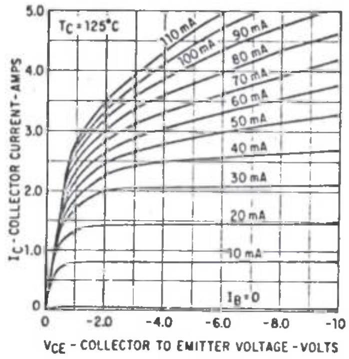
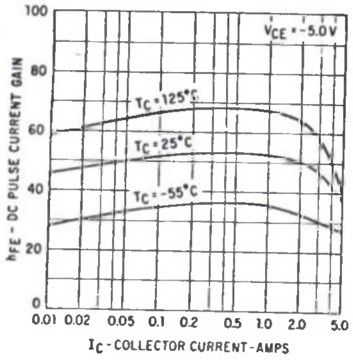
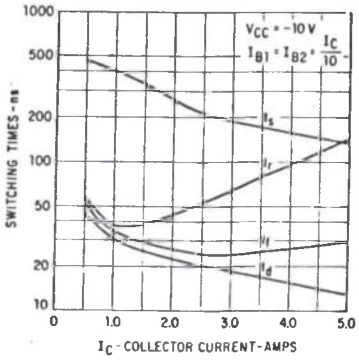


DC PULSE CURRENT GAIN VERSUS COLLECTOR CURRENT

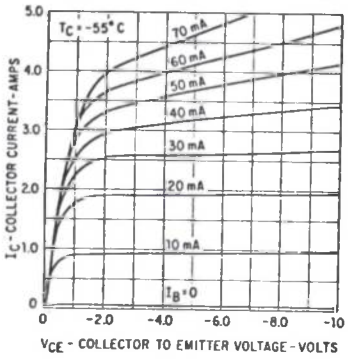


SWITCHING TIMES VERSUS COLLECTOR CURRENT

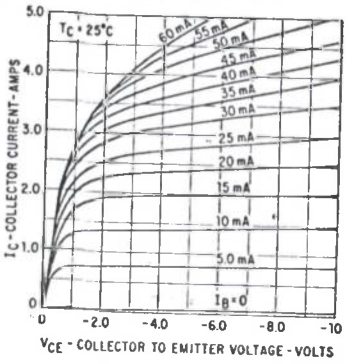


2N5005

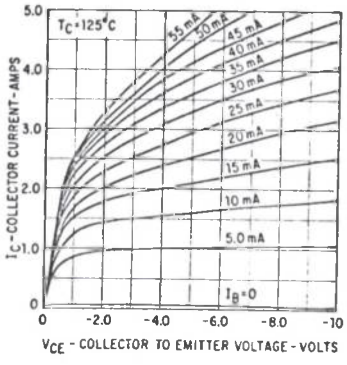
COLLECTOR CHARACTERISTICS



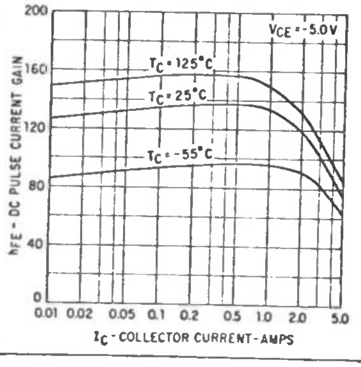
COLLECTOR CHARACTERISTICS



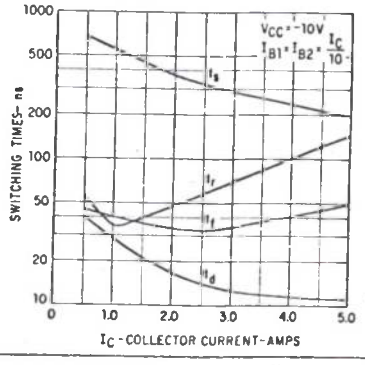
COLLECTOR CHARACTERISTICS



DC PULSE CURRENT GAIN VERSUS COLLECTOR CURRENT



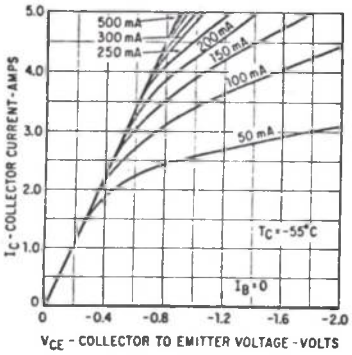
SWITCHING TIMES VERSUS COLLECTOR CURRENT



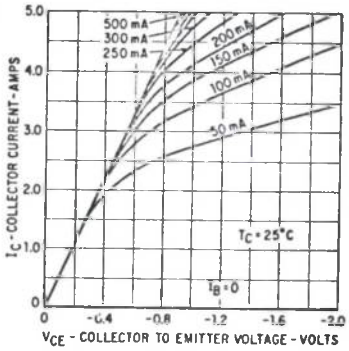
Fairchild cannot assume responsibility for use of [illegible]

TYPICAL ELECTRICAL CHARACTERISTICS

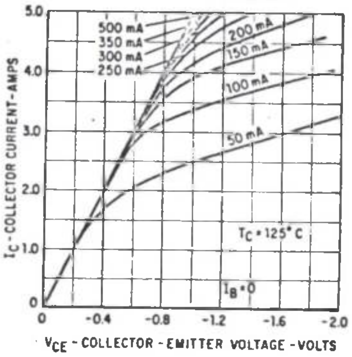
COLLECTOR CHARACTERISTICS SATURATION REGION



COLLECTOR CHARACTERISTICS SATURATION REGION



COLLECTOR CHARACTERISTICS SATURATION REGION



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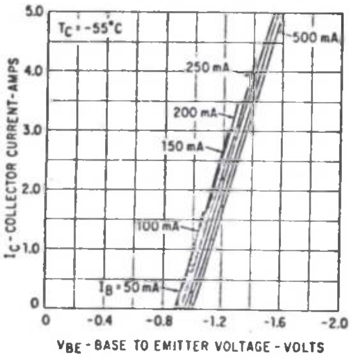

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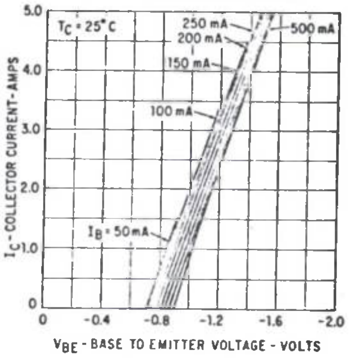
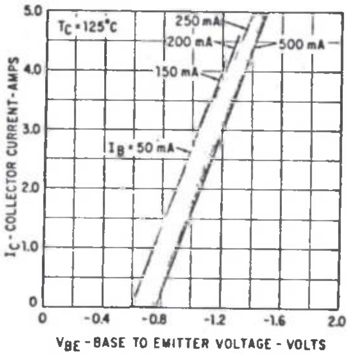
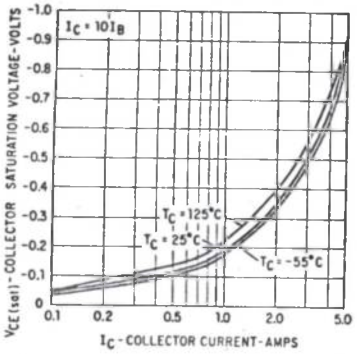


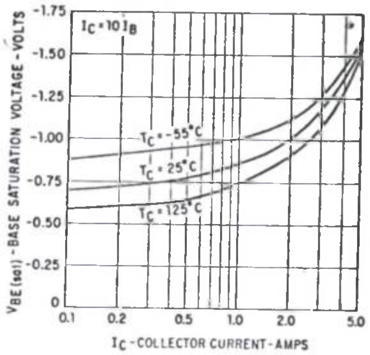
BASE CHARACTERISTICS



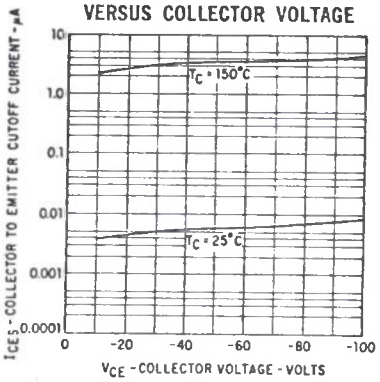
COLLECTOR SATURATION VOLTAGE VS. COLLECTOR CURRENT



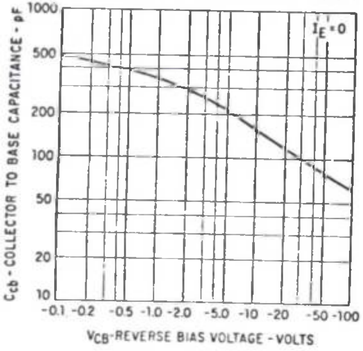
BASE SATURATION VOLTAGE VS. COLLECTOR CURRENT



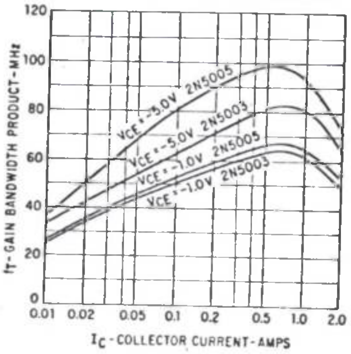
COLLECTOR CUTOFF CURRENT VERSUS COLLECTOR VOLTAGE



COLLECTOR TO BASE CAPACITANCE VERSUS REVERSE BIAS VOLTAGE



GAIN BANDWIDTH PRODUCT VERSUS COLLECTOR CURRENT



ELECTRICAL CHARACTERISTICS (25°C Case Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N5003 MIN.	2N5003 TYP.	2N5003 MAX.	2N5005 MIN.	2N5005 TYP.	2N5005 MAX.	UNITS	TEST CONDITIONS	
V_{BE}(sat)	Pulsed Base Saturation Voltage (Note 3)		−1.1	−1.45		−1.1	−1.45	Volts	$I_C = 2.5$ A	$I_B = 0.25$ A
V_{BE}(sat)	Pulsed Base Saturation Voltage (Note 3)		−1.55	−2.2		−1.55	−2.2	Volts	$I_C = 5.0$ A	$I_B = 0.5$ A
V_{BE}(on)	Pulsed Base Emitter "ON" Voltage (Note 3)			−1.45			−1.45	Volts	$I_C = 2.5$ A	$V_{CE} = -5.0$ V
I_{CES}	Collector Cutoff Current		0.006	1.0		0.006	1.0	μA	$V_{CE} = -60$ V	$V_{BE} = 0$
I_{EBO}	Emitter Cutoff Current			1.0			1.0	μA	$I_C = 0$	$V_{BE} = 4.0$ V
I_{CEX}(150°C)	Collector Reverse Current			500			500	μA	$V_{CE} = -60$ V	$V_{BE} = 2.0$ V
C_{cb}	Collector to Base Capacitance		170	250		170	250	pF	$I_E = 0$	$V_{CB} = -10$ V

NOTES:

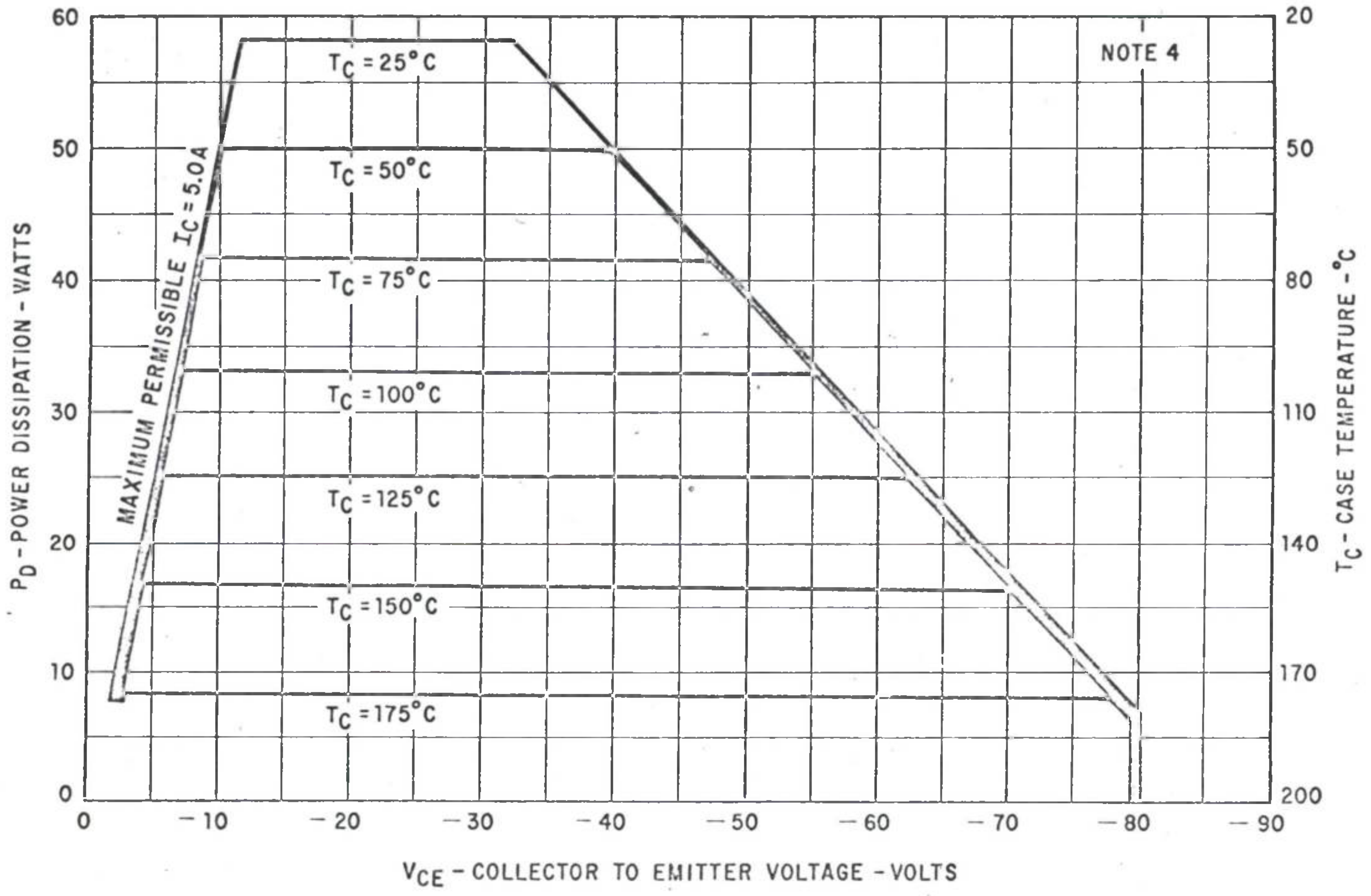
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) This rating refers to a high current point where collector to emitter voltage is lowest. For more information send for Fairchild Publication APP-4/2.

(3) Pulse Conditions: length = 300μs; duty cycle = 1%.

(4) Contact factory for maximum permissible power under pulsed or reverse biased operating conditions.

MAXIMUM PERMISSIBLE DC FORWARD BIASED POWER DISSIPATION



MARCH 1967

2N5003 · 2N5005

50 WATT PNP POWER TRANSISTORS

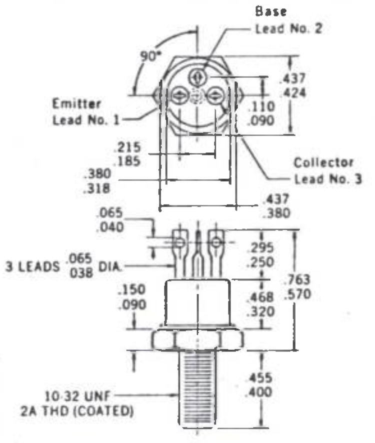
DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

SEE 2N5002 · 2N5004 FOR NPN COMPLEMENT

FEATURES

- HIGH POWER - - 50 WATTS @ $T_C = 50°C$, $V_{CE} = -40$ V
- HIGH VOLTAGE - - -80 V (MIN) LV_{CEO}
- HIGH CURRENT SAT. VOLTAGE - - -1.5 V (MAX) $V_{CE}(sat)$ @ 5.0 A
- HIGH FREQUENCY - - 60 AND 70 MHz (MIN) f_T
- BETA GUARANTEED @ 3 POINTS - - 50 mA, 2.5 A AND 5.0 A
- ISOLATED COLLECTOR PACKAGE - - NO ISOLATING HARDWARE REQUIRED
- DISCRETE EMITTER GEOMETRY WITH INTEGRATED FEEDBACK RESISTORS

PHYSICAL DIMENSIONS
(in accordance with JEDEC TO-59 outline)



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 6.44 grams

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures		
Storage Temperature		$-65°C$ to $+200°C$
Operating Junction Temperature		$-65°C$ to $+200°C$
Lead Temperature (Soldering, 60 seconds time limit)		$+300°C$
Maximum Power Dissipation		
Total Dissipation at 50°C Case Temperature, $V_{CE} = -40$ V (See Maximum Permissible Power Curve and Note 4)		50 Watts
Maximum Voltages and Current		
V_{CES}	Collector to Emitter Voltage	-100 Volts
V_{CEO}	Collector to Emitter Voltage (Note 2)	-80 Volts
V_{EBO}	Emitter to Base Voltage	-5.5 Volts
I_C	Collector Current	5.0 Amps

ELECTRICAL CHARACTERISTICS (25°C Case Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N5003 MIN.	2N5003 TYP.	2N5003 MAX.	2N5005 MIN.	2N5005 TYP.	2N5005 MAX.	UNITS	TEST CONDITIONS	
$V_{CEO}(sust)$	Collector to Emitter Sustaining Voltage (Notes 2 and 3)	-80			-80			Volts	$I_C = 100$ mA	$I_B = 0$
BV_{CES}	Collector to Emitter Breakdown Voltage	-100			-100			Volts	$I_C = 1.0$ mA	$V_{BE} = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	-5.5			-5.5			Volts	$I_C = 0$	$I_E = 1.0$ mA
h_{FE}	DC Pulse Current Gain (Note 3)	20	52		50	133			$I_C = 50$ mA	$V_{CE} = -5.0$ V
h_{FE}	DC Pulse Current Gain (Note 3)	30	50	90	70	114	200		$I_C = 2.5$ A	$V_{CE} = -5.0$ V
$h_{FE}(-55°C)$	DC Pulse Current Gain (Note 3)	15	32		35	90			$I_C = 2.5$ A	$V_{CE} = -5.0$ V
h_{FE}	DC Pulse Current Gain (Note 3)	20	38		40	77			$I_C = 5.0$ A	$V_{CE} = -5.0$ V
h_{fe}	High Frequency Current Gain (f = 20 MHz)	3.0	4.05		3.5	4.85			$I_C = 0.5$ A	$V_{CE} = -5.0$ V
$V_{CE}(sat)$	Pulsed Collector Saturation Voltage (Note 3)		-0.45	-0.75		-0.45	-0.75	Volts	$I_C = 2.5$ A	$I_B = 0.25$ A
$V_{CE}(sat)$	Pulsed Collector Saturation Voltage (Note 3)		-0.9	-1.5		-0.9	-1.5	Volts	$I_C = 5.0$ A	$I_B = 0.5$ A

Additional Electrical Characteristics on page 2

*Planar is a patented Fairchild process.

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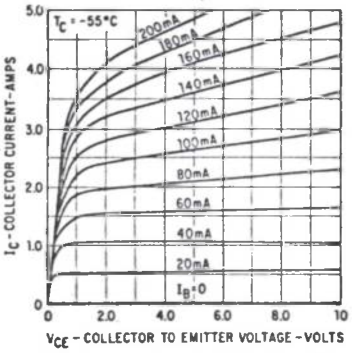
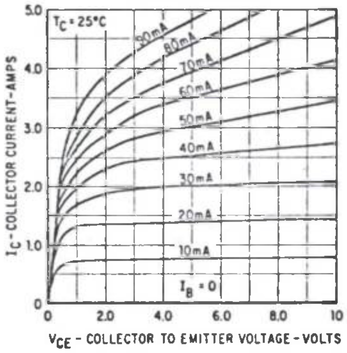
TYPICAL ELECTRICAL CHARACTERISTICS

2N5002

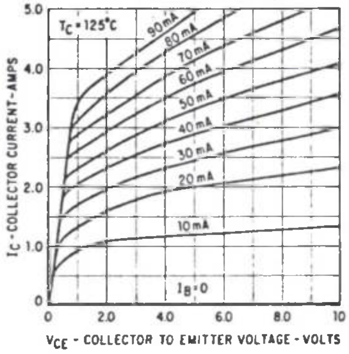
COLLECTOR CHARACTERISTICS*
ACTIVE REGION



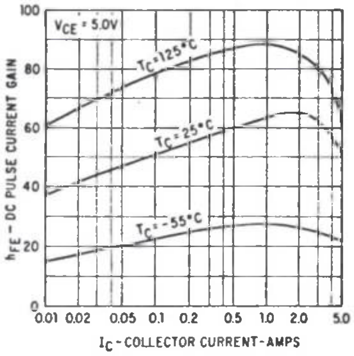
COLLECTOR CHARACTERISTICS*
ACTIVE REGION



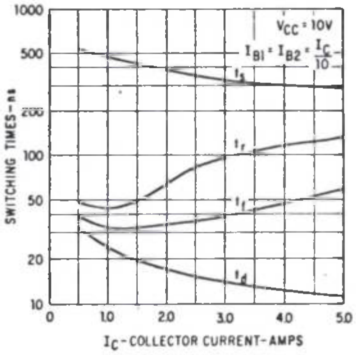
COLLECTOR CHARACTERISTICS*
ACTIVE REGION



DC PULSE CURRENT GAIN
VERSUS COLLECTOR CURRENT

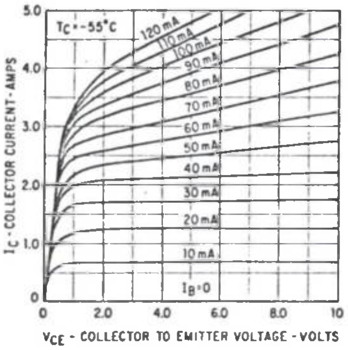


SWITCHING TIMES VERSUS
COLLECTOR CURRENT

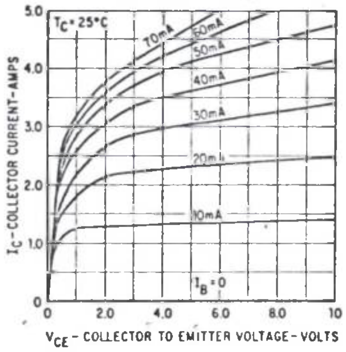


2N5004

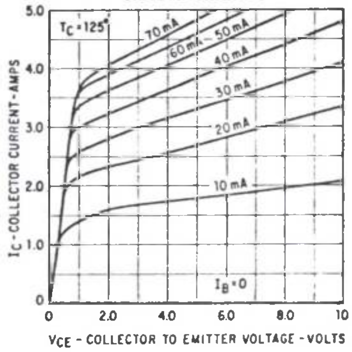
COLLECTOR CHARACTERISTICS*
ACTIVE REGION



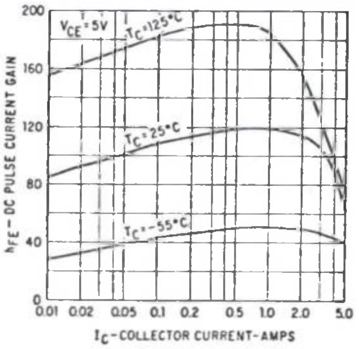
COLLECTOR CHARACTERISTICS*
ACTIVE REGION



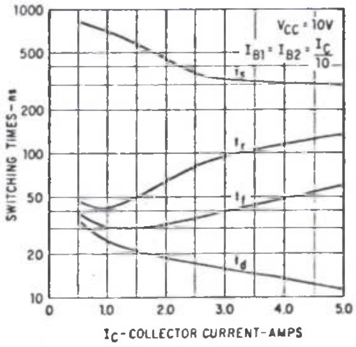
COLLECTOR CHARACTERISTICS*
ACTIVE REGION



DC PULSE CURRENT GAIN
VERSUS COLLECTOR CURRENT



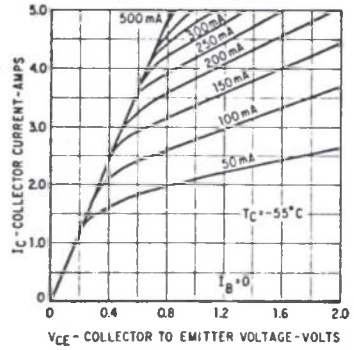
SWITCHING TIMES VERSUS
COLLECTOR CURRENT



*Single Family Characteristics on Transistor Curve Tracer.

TYPICAL ELECTRICAL CHARACTERISTICS

COLLECTOR CHARACTERISTICS*
SATURATION REGION



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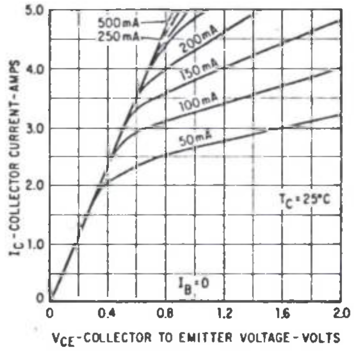
SATURATION REGION



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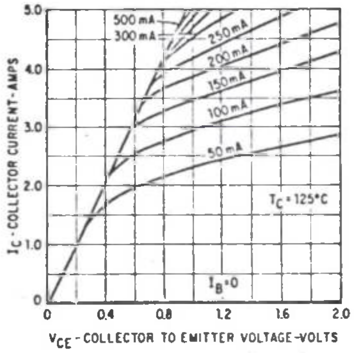
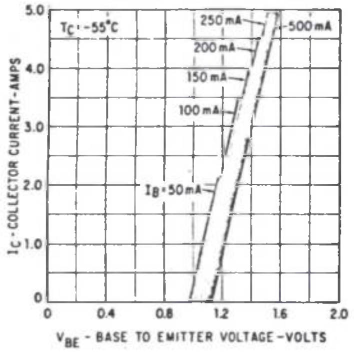
SATURATION REGION



BASE CHARACTERISTICS*



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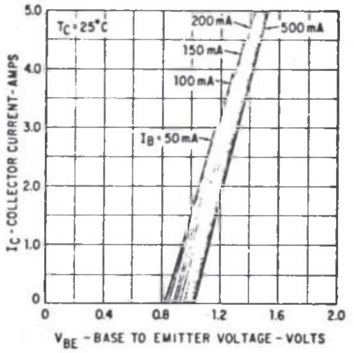

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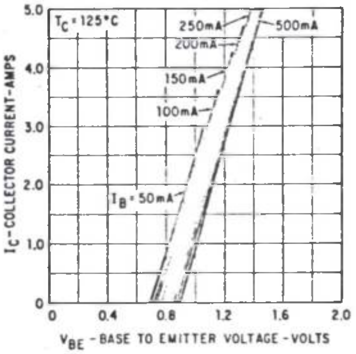
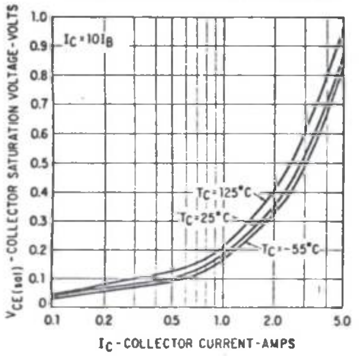
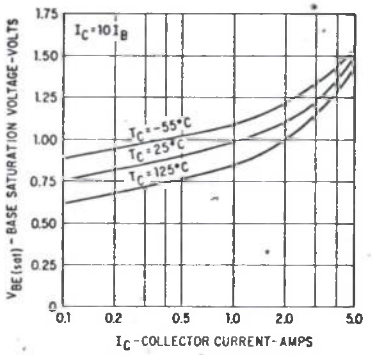


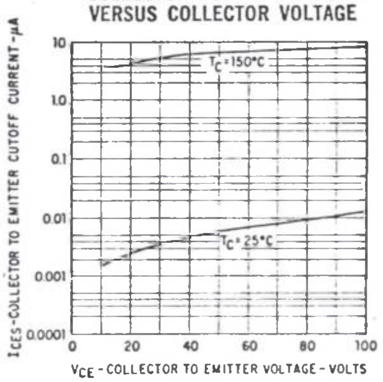
COLLECTOR SATURATION VOLTAGE
VERSUS COLLECTOR CURRENT



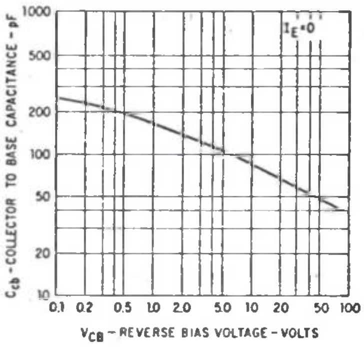
BASE SATURATION VOLTAGE
VERSUS COLLECTOR CURRENT



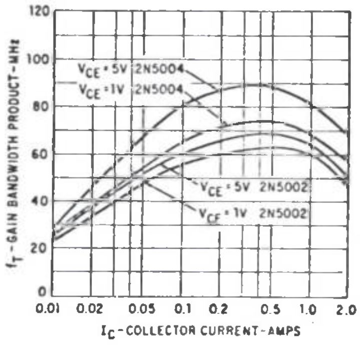
COLLECTOR CUTOFF CURRENT
VERSUS COLLECTOR VOLTAGE



COLLECTOR TO BASE CAPACITANCE
VERSUS REVERSE BIAS VOLTAGE



GAIN BANDWIDTH PRODUCT
VERSUS COLLECTOR CURRENT



*Single Family Characteristics on Transistor Curve Tracer.

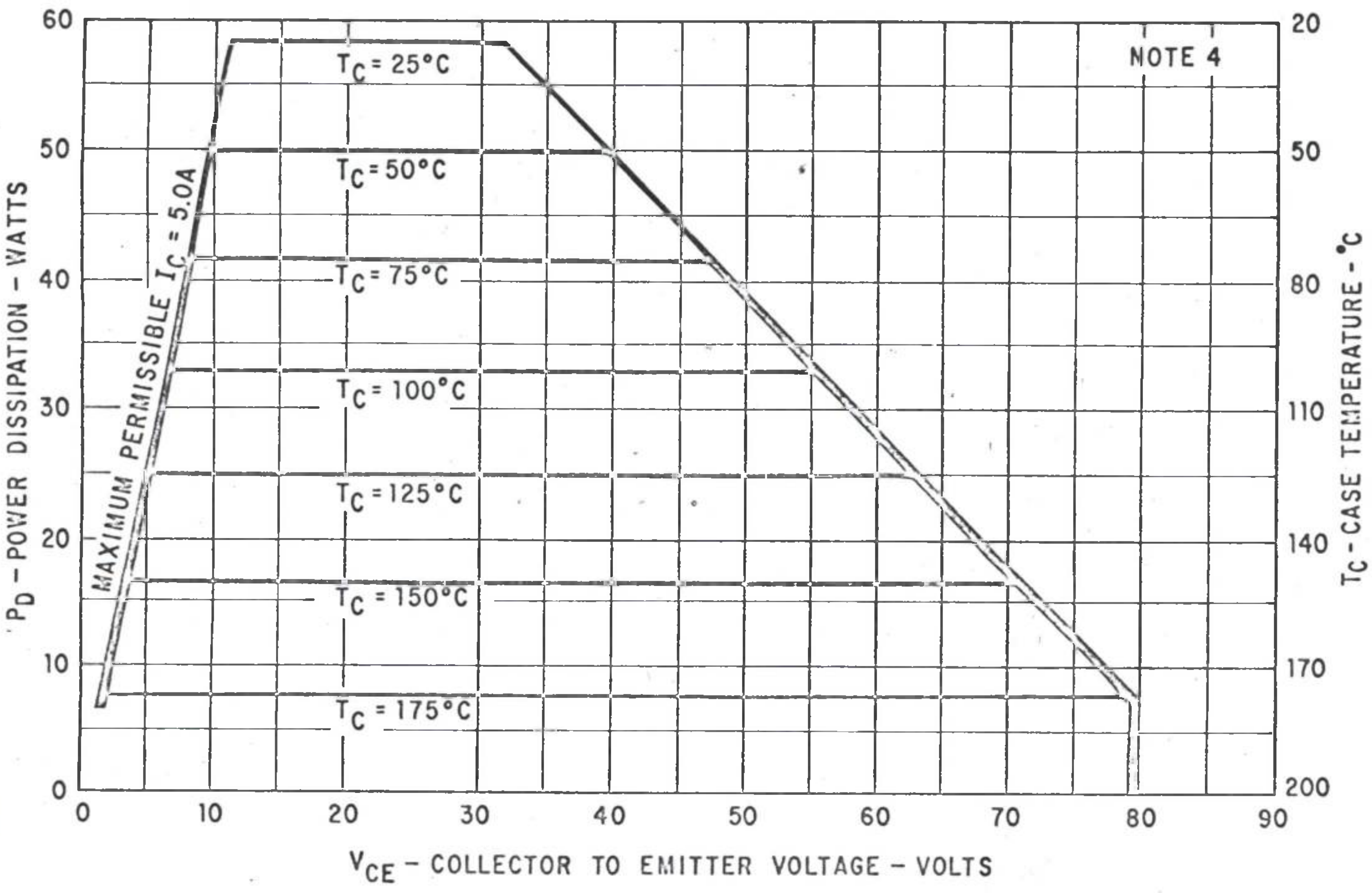
ELECTRICAL CHARACTERISTICS (25°C Case Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N5002			2N5004			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
V_{BE}(sat)	Pulsed Base Saturation Voltage (Note 3)		1.16	1.45		1.16	1.45	Volts	$I_C = 2.5$ A	$I_B = 0.25$ A
V_{BE}(sat)	Pulsed Base Saturation Voltage (Note 3)		1.50	2.2		1.50	2.2	Volts	$I_C = 5.0$ A	$I_B = 0.5$ A
V_{BE}(on)	Pulsed Base Emitter "ON" Voltage (Note 3)			1.45			1.45	Volts	$I_C = 2.5$ A	$V_{CE} = 5.0$ V
I_{CES}	Collector Cutoff Current		0.007	1.0		0.007	1.0	μA	$V_{CE} = 60$ V	$V_{BE} = 0$
I_{EBO}	Emitter Cutoff Current			1.0			1.0	μA	$I_C = 0$	$V_{EB} = 5.0$ V
I_{CEX}(150°C)	Collector Reverse Current			500			500	μA	$V_{CE} = 60$ V	$V_{EB} = 2.0$ V
C_{cb}	Collector to Base Capacitance		90	250		90	250	pF	$I_E = 0$	$V_{CB} = 10$ V

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) This rating refers to a high current point where collector to emitter voltage is lowest. For more information send for Fairchild Publication APP-4/2.
(3) Pulse Conditions: length = 300μs; duty cycle = 1%.
(4) Contact factory for maximum permissible power under pulsed or reverse biased operating conditions.

MAXIMUM PERMISSIBLE DC FORWARD BIASED POWER DISSIPATION



MAY 1967

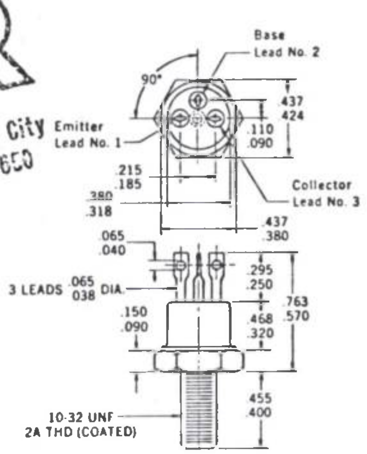
2N5002 • 2N5004
50 WATT NPN POWER TRANSISTORS
DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

SEE 2N5003 • 2N5005 FOR PNP COMPLEMENT

- HIGH POWER .... 50 WATTS @ $T_C = 50°C$, $V_{CE} = 40$ V
- HIGH VOLTAGE .... 80 V (MIN) LV_{CEO}
- HIGH CURRENT SATURATION VOLTAGE .... 1.5 V (MAX) $V_{CE}(sat)$ @ 5.0 A
- HIGH FREQUENCY .... 60 AND 70 MHz (MIN) f_T
- BETA GUARANTEED @ 3 POINTS .... 50 mA, 2.5 A AND 5.0 A
- ISOLATED COLLECTOR PACKAGE .... NO ISOLATING HARDWARE REQUIRED
- DISCRETE EMITTER GEOMETRY WITH INTEGRATED FEEDBACK RESISTORS

HYER
Denver 771-5285
Albuquerque 265-5767
Phoenix 264-9291
Salt Lake City ZEnith-650

PHYSICAL DIMENSIONS
(in accordance with JEDEC TO-59 outline)



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 6.44 grams

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	−65°C to +200°C
Lead Temperature (Soldering, 60 second time limit)	+300°C

Maximum Power Dissipation

Total Dissipation at 50°C Case Temperature, $V_{CE} = 40$ V (See Maximum Permissible Power Curve and Note 4)	50 Watts

Maximum Voltages and Current

V_{CES}	Collector to Emitter Voltage	100 Volts
V_{CEO}	Collector to Emitter Voltage (Note 2)	80 Volts
V_{EBO}	Emitter to Base Voltage	6.0 Volts
I_C	Collector Current	5.0 Amps

ELECTRICAL CHARACTERISTICS (25°C Case Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N5002 MIN.	2N5002 TYP.	2N5002 MAX.	2N5004 MIN.	2N5004 TYP.	2N5004 MAX.	UNITS	TEST CONDITIONS	
$V_{CEO}(sust)$	Collector to Emitter Sustaining Voltage (Notes 2 and 3)	80			80			Volts	$I_C = 100$ mA	$I_B = 0$
BV_{CES}	Collector to Emitter Breakdown Voltage	100			100			Volts	$I_C = 1.0$ mA	$V_{BE} = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	6.0			6.0			Volts	$I_C = 0$	$I_E = 1.0$ mA
h_{FE}	DC Pulse Current Gain (Note 3)	20	46		50	100			$I_C = 50$ mA	$V_{CE} = 5.0$ V
h_{FE}	DC Pulse Current Gain (Note 3)	30	64	90	70	114	200		$I_C = 2.5$ A	$V_{CE} = 5.0$ V
$h_{FE}(-55°C)$	DC Pulse Current Gain (Note 3)	15	26		35	50			$I_C = 2.5$ A	$V_{CE} = 5.0$ V
h_{FE}	DC Pulse Current Gain (Note 3)	20	53		40	65			$I_C = 5.0$ A	$V_{CE} = 5.0$ V
h_{fe}	High Frequency Current Gain (f = 20 MHz)	3.0	3.4		3.5	4.4			$I_C = 0.5$ A	$V_{CE} = 5.0$ V
$V_{CE}(sat)$	Pulsed Collector Saturation Voltage (Note 3)		0.43	0.75		0.43	0.75	Volts	$I_C = 2.5$ A	$I_B = 0.25$ A
$V_{CE}(sat)$	Pulsed Collector Saturation Voltage (Note 3)		0.85	1.5		0.85	1.5	Volts	$I_C = 5.0$ A	$I_B = 0.5$ A

Additional Electrical Characteristics on page 2
Notes on page 2

*Planar is a patented Fairchild process.

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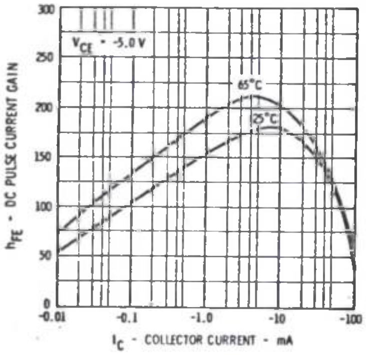
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

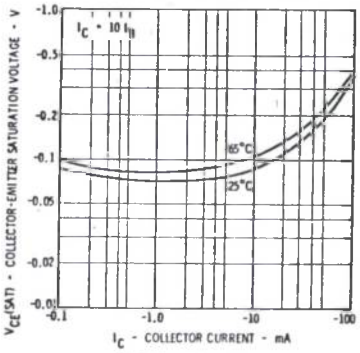
SYMBOL	CHARACTERISTIC	2N4916 MIN.	2N4916 TYP.	2N4916 MAX.	2N4917 MIN.	2N4917 TYP.	2N4917 MAX.	UNITS	TEST CONDITIONS
V_{CEO} (sust)	Collector to Emitter Sustaining Voltage [Notes 4 and 5]	−30			−30			Volts	$I_C = 10$ mA $I_B = 0$ (pulsed)
BV_{CBO}	Collector to Base Breakdown Voltage	−30			−30			Volts	$I_C = 10\ \mu A$ $I_E = 0$
BV_{CES}	Collector to Emitter Breakdown Voltage	−30			−30			Volts	$I_C = 10\ \mu A$ $V_{BE} = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0			−5.0			Volts	$I_C = 0$ $I_E = 10\ \mu A$
I_{CES}	Collector Reverse Current			25			25	nA	$V_{CE} = -15$ V $V_{BE} = 0$
I_{CES} (65°C)	Collector Reverse Current			25			25	μA	$V_{CE} = -15$ V $V_{BE} = 0$
C_{obo}	Open Circuit Output Capacitance		2.2	4.5		2.2	4.5	pF	$I_E = 0$ $V_{CB} = -10$V
C_{ibo}	Open Circuit Input Capacitance		4.0	8.0		4.0	8.0	pF	$I_C = 0$ $V_{EB} = -0.5$ V
$r_b' C_c$	Collector-Base Time Constant (f = 80 MHz)			50			50	ps	$I_C = 10$ mA $V_{CE} = -20$ V
NF	Noise Figure (f = 100 MHz)		3.5	6.0		3.5	6.0	dB	$I_C = 1.0$ mA $V_{CE} = -5.0$ V $R_S = 100\Omega$ BW = 15 MHz
NF	Noise Figure [Note 7]		2.5	4.0		2.5	4.0	dB	$I_C = 100\ \mu A$ $V_{CE} = -5.0$ V $R_S = 1.0\ k\Omega$

TYPICAL ELECTRICAL CHARACTERISTICS

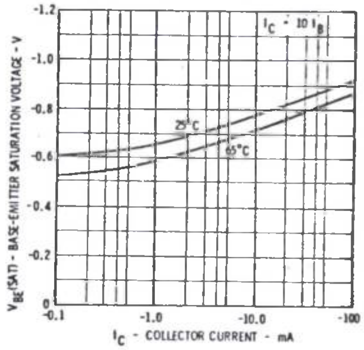
DC PULSED CURRENT GAIN VERSUS COLLECTOR CURRENT



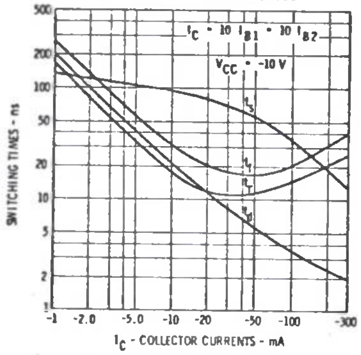
COLLECTOR-EMITTER SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



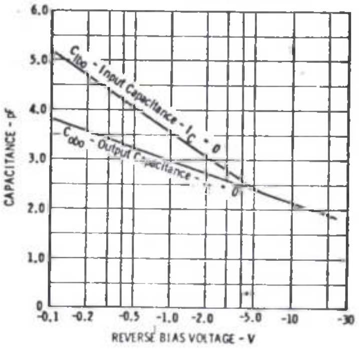
BASE SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



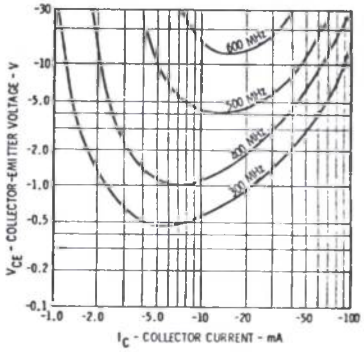
SWITCHING TIMES VERSUS COLLECTOR CURRENT



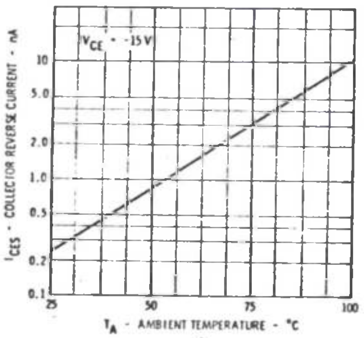
INPUT AND OUTPUT CAPACITANCES VERSUS REVERSE BIAS VOLTAGE



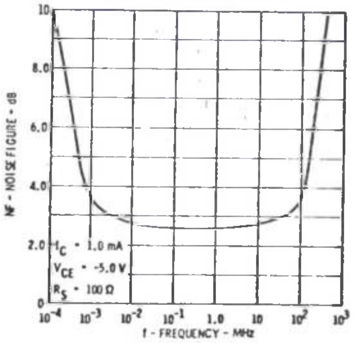
CONTOURS OF CONSTANT GAIN BANDWITH PRODUCT (f_T)



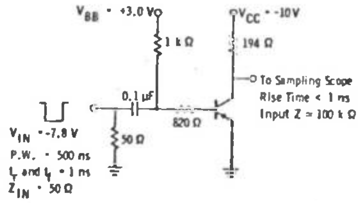
COLLECTOR REVERSE CURRENT VERSUS AMBIENT TEMPERATURE



NOISE FIGURE VERSUS FREQUENCY



SWITCHING TIME TEST CIRCUIT



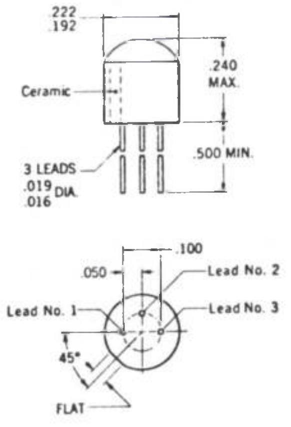
2N4916 • 2N4917

PNP HIGH-SPEED SWITCH AND RF AMPLIFIER

DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

- HIGH BETA (h_{FE}) -- 150 to 300 @ 10 mA
- HIGH FREQUENCY (f_T) -- 450 MHz Min. @ 10 mA
- EXCELLENT R.F. PERFORMANCE ($r_b'C_c$) -- 50 ps Max.
- LOW CAPACITANCE (C_{obo}) -- 4.5 pF Max.
- LOW NOISE (100 MHz N.F.) -- 6.0 dB Max.

PHYSICAL DIMENSIONS
Epoxy package
TO-106



NOTES. All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram

ABSOLUTE MAXIMUM RATINGS [Note 1]

Maximum Temperatures	
Storage Temperature	−55°C to +125°C
Operating Junction Temperature	+125°C Maximum
Lead Temperature (Soldering, 10 sec time limit)	+260°C Maximum
Maximum Power Dissipation	
Total Dissipation at 25°C Case Temperature [Notes 2 and 3]	0.5 Watt
at 25°C Ambient Temperature [Notes 2 and 3]	0.2 Watt
Maximum Voltages and Current	
V_{CBO} Collector to Base Voltage	−30 Volts
V_{CEO} Collector to Emitter Voltage [Note 4]	−30 Volts
V_{EBO} Emitter to Base Voltage	−5.0 Volts
I_C Collector Current	100 mA

[illegible]TRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N4916 MIN.	2N4916 TYP.	2N4916 MAX.	2N4917 MIN.	2N4917 TYP.	2N4917 MAX.	UNITS	TEST CONDITIONS
h_{FE}	DC Current Gain	40	70		100	150			$I_c = 100\ \mu A$ $V_{CE} = -1.0\ V$
h_{FE}	DC Current Gain	60	100		150	200			$I_C = 1.0\ mA$ $V_{CE} = -1.0\ V$
h_{FE}	DC Pulse Current Gain [Note 5]	70	150	200	150	200	300		$I_C = 10\ mA$ $V_{CE} = -1.0\ V$
h_{FE}	DC Pulse Current Gain [Note 5]	15	30		30	60			$I_C = 50\ mA$ $V_{CE} = -1.0\ V$
V_{CE} (sat)	Collector Saturation Voltage		−0.07	−0.13		−0.07	−0.13	Volts	$I_C = 1.0\ mA$ $I_B = 0.1\ mA$
V_{CE} (sat)	Pulsed Collector Saturation Voltage [Note 5]		−0.1	−0.14		−0.1	−0.14	Volts	$I_C = 10\ mA$ $I_B = 1.0\ mA$
V_{CE} (sat)	Pulsed Collector Saturation Voltage [Note 5]		−0.2	−0.3		−0.2	−0.3	Volts	$I_C = 50\ mA$ $I_B = 5.0\ mA$
V_{BE} (sat)	Base Saturation Voltage		−0.65	−0.75		−0.65	−0.75	Volts	$I_C = 1.0\ mA$ $I_B = 0.1\ mA$
V_{BE} (sat)	Pulsed Base Saturation Voltage [Note 5]	−0.7	−0.77	−0.9	−0.7	−0.77	−0.9	Volts	$I_C = 10\ mA$ $I_B = 1.0\ mA$
V_{BE} (sat)	Pulsed Base Saturation Voltage [Note 5]	−0.75	−0.88	−1.1	−0.75	−0.88	−1.1	Volts	$I_C = 50\ mA$ $I_B = 5.0\ mA$
t_{on}	Turn On Time [Note 6]		20	40		20	40	ns	$I_C \approx 50\ mA$ $I_{B1} \approx 5.0\ mA$
t_{off}	Turn Off Time [Note 6]		95	150		95	150	ns	$I_C \approx 50\ mA$ $I_{B1} \approx 5.0\ mA$ $I_{B2} \approx -5.0\ mA$
h_{fe}	High Frequency Current Gain (f = 100 MHz)	4.0	5.5		4.5	6.0			$I_C = 10\ mA$ $V_{CE} = -20\ V$

* Planar is a patented Fairchild process.

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
(3) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C); junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).
(4) This rating refers to a high current point where collector to emitter voltage is lowest.
(5) Pulse Conditions: length = 300 μs; duty cycle = 1%.
(6) See switching circuit for exact values of I_C, I_{B1} and I_{B2}.
(7) Power Bandwidth of 15.7 kHz with 3 dB points at 10 Hz and 10 kHz.

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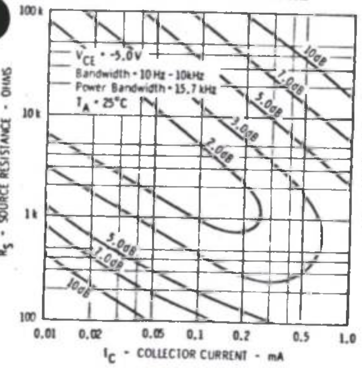
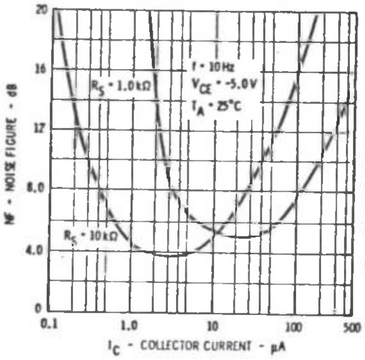
2N4889
TYPICAL ELECTRICAL CHARACTERISTICS

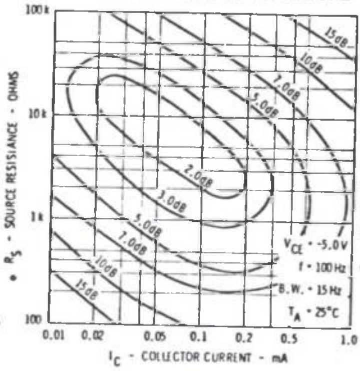
CONTOURS OF CONSTANT WIDE BAND NOISE FIGURE



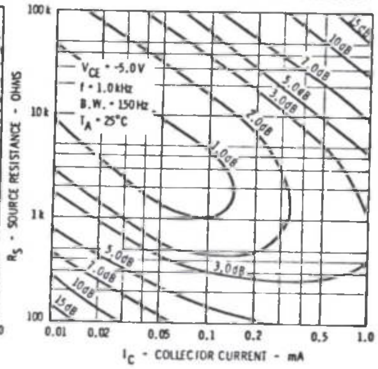
NOISE FIGURE VERSUS COLLECTOR CURRENT



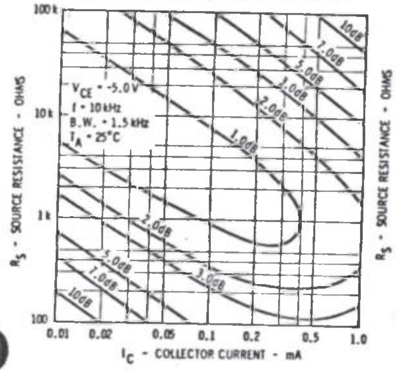
CONTOURS OF CONSTANT NARROW BAND NOISE FIGURE



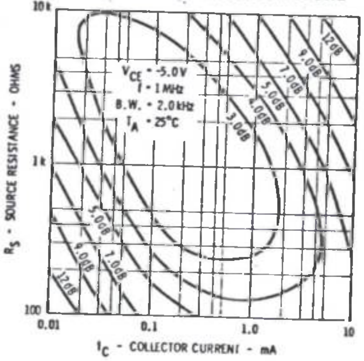
CONTOURS OF CONSTANT NARROW BAND NOISE FIGURE



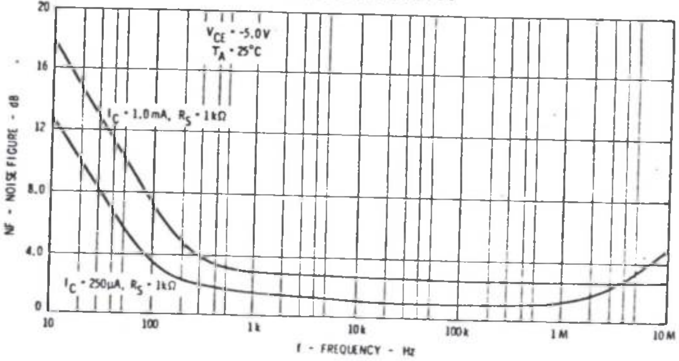
CONTOURS OF CONSTANT NARROW BAND NOISE FIGURE



CONTOURS OF CONSTANT NARROW BAND NOISE FIGURE



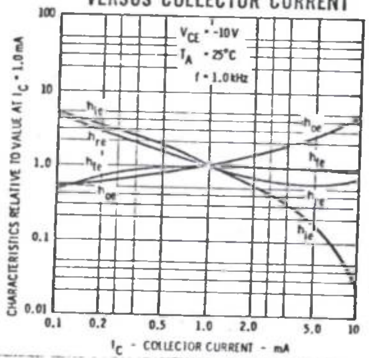
SPOT NOISE FIGURE VERSUS FREQUENCY



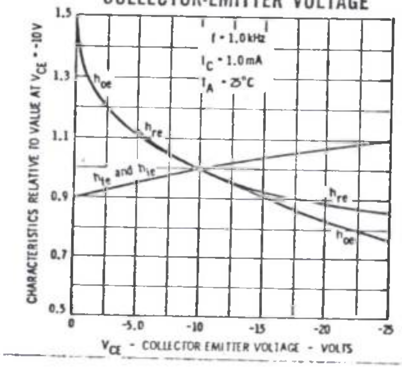
LL SIGNAL CHARACTERISTICS (f = 1.0 kHz)

SYMBOL	CHARACTERISTIC	2N4888 MIN.	2N4888 TYP.	2N4888 MAX.	2N4889 MIN.	2N4889 TYP.	2N4889 MAX.	UNITS	TEST CONDITIONS
h_{fe}	Small Signal Current Gain	30	40	500	65	150	400		$I_C = 1.0$ mA $V_{CE} = -10$ V
h_{ie}	Input Resistance	0.75	1.2	20	1.7	5.0	12	kΩ	$I_C = 1.0$ mA $V_{CE} = -10$ V
h_{oe}	Output Conductance	1.4	2.5	40	3.0	10	25	µmhos	$I_C = 1.0$ mA $V_{CE} = -10$ V
h_{re}	Voltage Feedback Ratio		1.0			2.5	5.0	$\times 10^{-4}$	$I_C = 1.0$ mA $V_{CE} = -10$ V

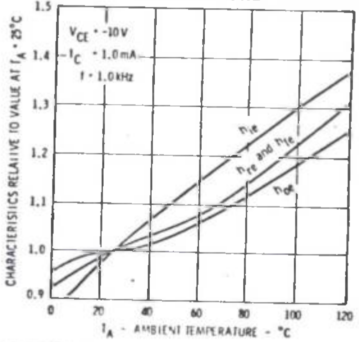
COMMON EMITTER CHARACTERISTICS VERSUS COLLECTOR CURRENT



COMMON EMITTER CHARACTERISTICS VERSUS COLLECTOR-EMITTER VOLTAGE



COMMON EMITTER CHARACTERISTICS VERSUS TEMPERATURE



SEMICONDUCTOR

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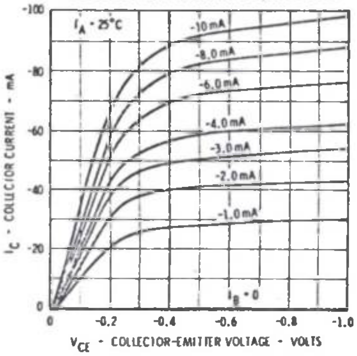
Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product. No other circuit patent licenses are implied

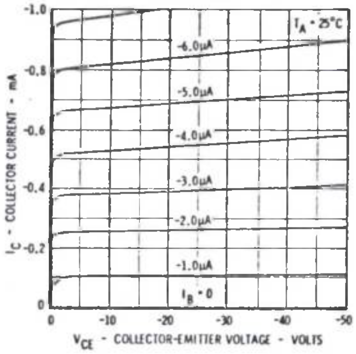
2N4889

TYPICAL ELECTRICAL CHARACTERISTICS

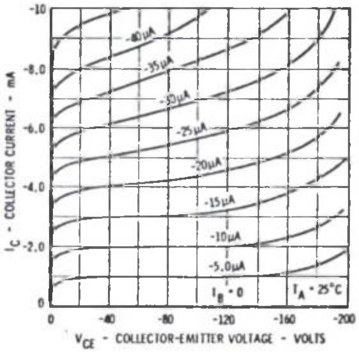
COLLECTOR CHARACTERISTICS*



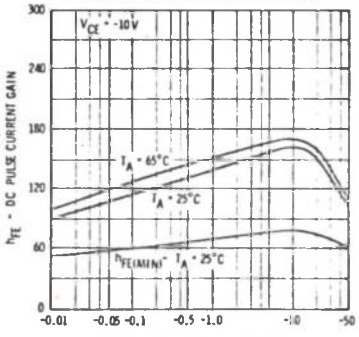
COLLECTOR CHARACTERISTICS*



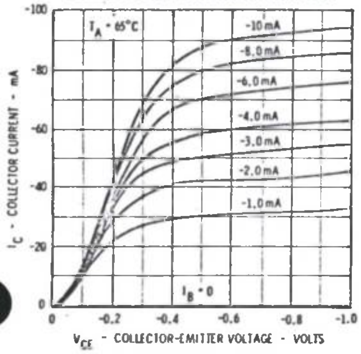
COLLECTOR CHARACTERISTICS*



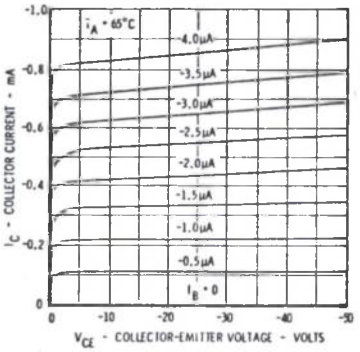
DC PULSE CURRENT GAIN VERSUS COLLECTOR CURRENT



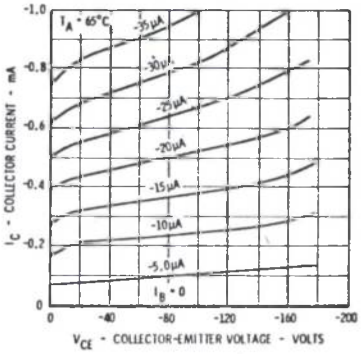
COLLECTOR CHARACTERISTICS*



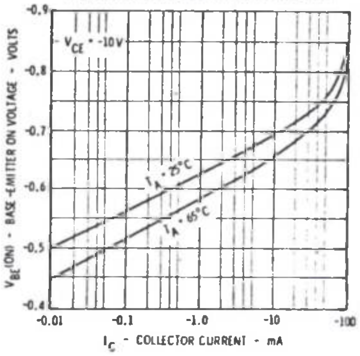
COLLECTOR CHARACTERISTICS*



COLLECTOR CHARACTERISTICS*

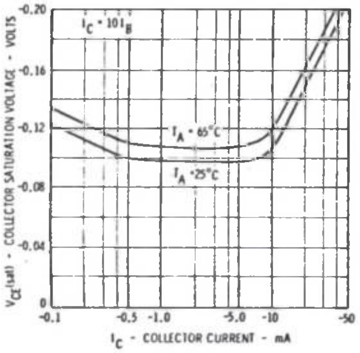


BASE-EMITTER ON VOLTAGE VERSUS COLLECTOR CURRENT

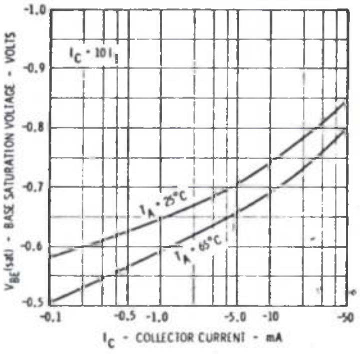


2N4888 ● 2N4889

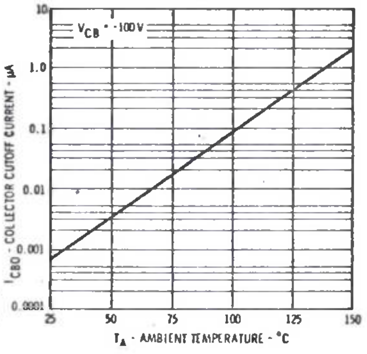
COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



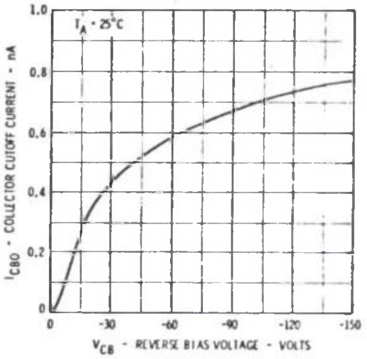
BASE SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



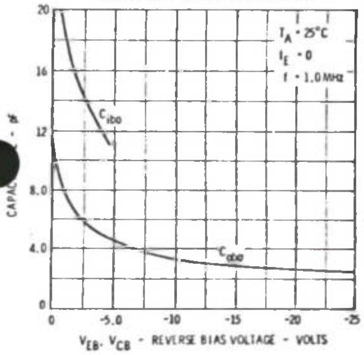
COLLECTOR CUTOFF CURRENT VERSUS AMBIENT TEMPERATURE



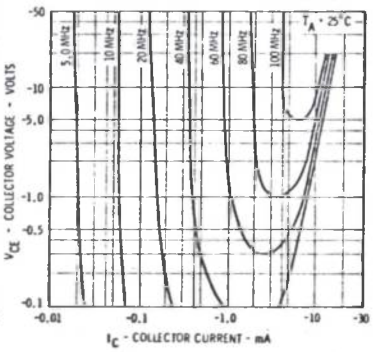
COLLECTOR CUTOFF CURRENT VERSUS REVERSE BIAS VOLTAGE



INPUT AND OUTPUT CAPACITANCES VERSUS REVERSE BIAS VOLTAGES

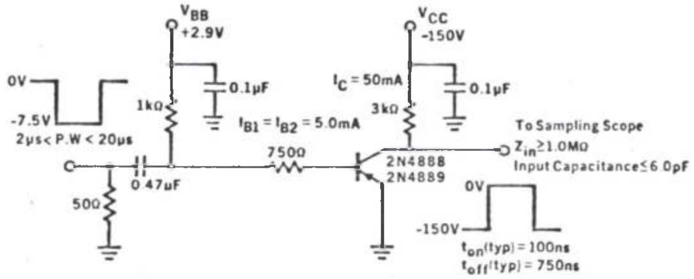


CONTOURS OF CONSTANT GAIN BANDWIDTH PRODUCT (f_T)



$T_{on} - T_{off}$

SWITCHING CIRCUIT



ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

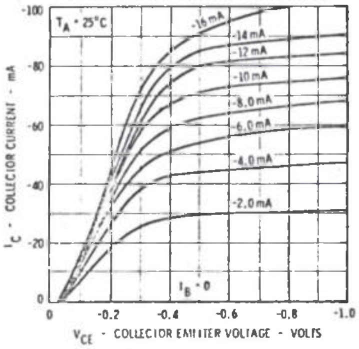
SYMBOL	CHARACTERISTIC	2N4888 MIN.	2N4888 TYP.	2N4888 MAX.	2N4889 MIN.	2N4889 TYP.	2N4889 MAX.	UNITS	TEST CONDITIONS
I_{CBO}	Collector Cutoff Current		0.7	50		0.7	10	nA	$V_{CB} = -100$ V $I_E = 0$
I_{CBO} (65°C)	Collector Cutoff Current		0.01	2.5		0.01	0.5	μA	$V_{CB} = -100$ V $I_E = 0$
V_{CE} (sat)	Pulsed Collector Saturation Voltage (Note 4)		−0.1	−0.5		−0.1	−0.5	Volts	$I_C = 10$ mA $I_B = 1.0$ mA
BV_{EBO}	Emitter to Base Breakdown Voltage	−6.0			−6.0			Volts	$I_E = 10\mu$A $I_C = 0$
I_{EBO}	Emitter Cutoff Current		0.4	50		0.4	10	nA	$V_{EB} = -4.0$ V $I_C = 0$
V_{BE} (on)	Pulsed Base Emitter On Voltage (Note 4)		−0.66	−0.8		−0.59	−0.7	Volts	$I_C = 1.0$ mA $V_{CE} = -10$ V
V_{BE} (sat)	Pulsed Base Saturation Voltage (Note 4)		−0.74	−0.9		−0.74	−0.9	Volts	$I_C = 10$ mA $I_B = 1.0$ mA
C_{ibo}	Common-Base, Open-Circuit Input Capacitance		11	30		11	25	pF	$V_{EB} = -0.5$ V $I_C = 0$
h_{fe}	High Frequency Current Gain (f = 20 MHz)	1.5	1.8	8.0	2.0	3.3	8.0		$I_C = 1.0$ mA $V_{CE} = -10$ V

NOTES:

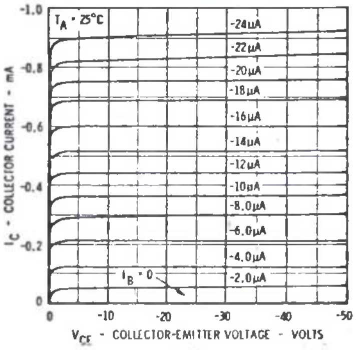
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 125°C/Watt (derating factor of 8.0 mW/°C); junction to ambient thermal resistance of 333°C/Watt (derating factor of 3.0 mW/°C).
(3) This rating refers to a high current point where collector to emitter voltage is lowest. For more information send for Fairchild Publication APP-4/2.
(4) Pulse Conditions: length = 300 μs; duty cycle = 1%.

2N4888
TYPICAL ELECTRICAL CHARACTERISTICS

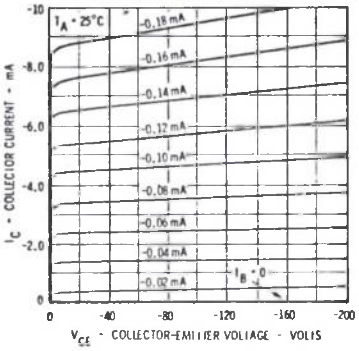
COLLECTOR CHARACTERISTICS*



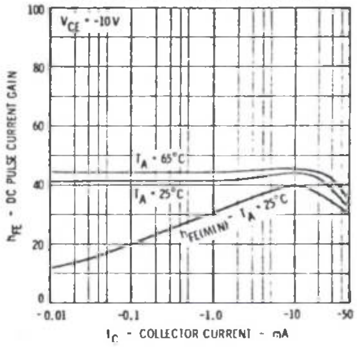
COLLECTOR CHARACTERISTICS*



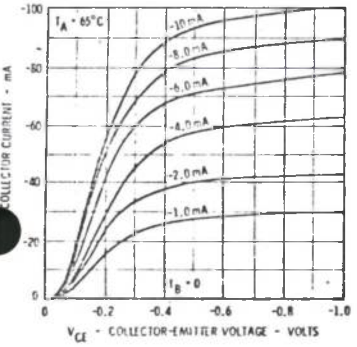
COLLECTOR CHARACTERISTICS*



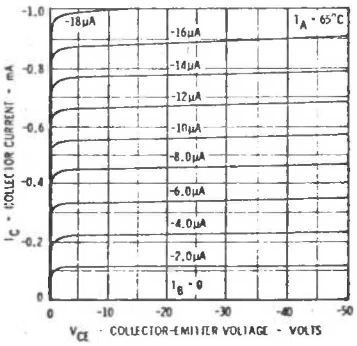
DC PULSE CURRENT GAIN
VERSUS COLLECTOR CURRENT



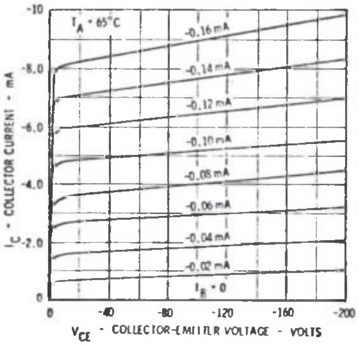
COLLECTOR CHARACTERISTICS*



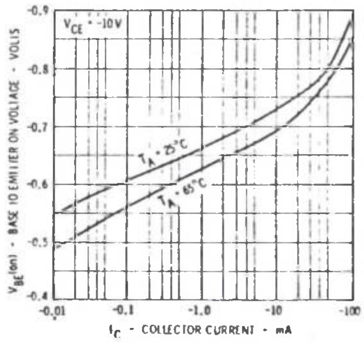
COLLECTOR CHARACTERISTICS*



COLLECTOR CHARACTERISTICS*



BASE-EMITTER ON VOLTAGE
VERSUS COLLECTOR CURRENT



* Single family characteristic on Transistor Curve Tracer.

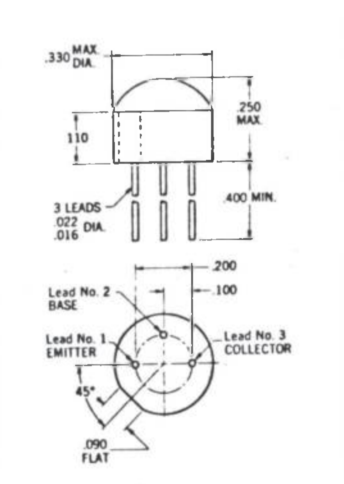
2N4888 • 2N4889

PNP LOW NOISE HIGH VOLTAGE AMPLIFIER

DIFFUSED SILICON PLANAR* II TRANSISTORS

- **VERY HIGH VOLTAGE (LV_{CEO}) -- 150 VOLTS (Min.)**
- **LOW NOISE FIGURE -- 3.0 dB (Max.) @ 1.0 kHz**
- **LOW OUTPUT CAPACITANCE (C_{obo}) -- 4.0 pF (Max.)**
- **HIGH BETA (h_{FE}) -- 80–300 @ 10 mA**
- **EXCELLENT BETA LINEARITY FROM 10 μA to 50 mA**

PHYSICAL DIMENSIONS



NOTES All dimensions in inches
Leads are gold plated kovar
Package weight is 0.68 gram

ABSOLUTE MAXIMUM RATINGS [Note 1]

Maximum Temperatures	
Storage Temperature	−55°C to +125°C
Operating Junction Temperature	+125°C
Soldering Temperature (10 second time limit)	+260°C
Maximum Power Dissipation	
Total Dissipation at 25°C Case Temperature [Note 2]	0.8 Watt
at 75°C Case Temperature [Note 2]	0.4 Watt
at 25°C Ambient Temperature [Note 2]	0.3 Watt
Maximum Voltages	
V_{CBO} Collector to Base Voltage	−150 Volts
V_{CEO} Collector to Emitter Voltage [Note 3]	−150 Volts
V_{EBO} Emitter to Base Voltage	−6.0 Volts

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N4888 MIN.	2N4888 TYP.	2N4888 MAX.	2N4889 MIN.	2N4889 TYP.	2N4889 MAX.	UNITS	TEST CONDITIONS
V_{CEO}	Collector to Emitter Sustaining Voltage	−150			−150			Volts	$I_C = 2.0$ mA $I_B = 0$
BV_{CBO}	Collector to Base Breakdown Voltage	−150			−150			Volts	$I_C = 100\ \mu$A $I_E = 0$
NF	Narrow Band Noise Figure (f = 100 Hz)					3.0	10	dB	$I_C = 250\ \mu$A $V_{CE} = -5.0$ V $R_S = 1.0$ kΩ B.W. = 15 Hz
NF	**Narrow Band Noise Figure (f = 1.0 kHz)**					**0.8**	**3.0**	**dB**	$I_C = 30\ \mu$A $V_{CE} = -5.0$ V $R_S = 10$ kΩ B.W. = 150 Hz
NF	Narrow Band Noise Figure (f = 10 kHz)					1.5	3.0	dB	$I_C = 250\ \mu$A $V_{CE} = -5.0$ V $R_S = 1.0$ kΩ B.W. = 1.5 kHz
NF	Wide Band Noise Figure (f = 10 Hz to 10 kHz)					2.0	4.0	dB	$I_C = 250\ \mu$A $V_{CE} = -5.0$ V $R_S = 1.0$ kΩ B.W. = 15.7 kHz
NF	Narrow Band Noise Figure (f = 1.0 MHz)					2.0	4.0	dB	$I_C = 1.0$ mA $V_{CE} = -10$ V $R_S = 1.0$ kΩ B.W. = 2.0 kHz
h_{FE}	DC Pulse Current Gain [Note 4]		30		60	135			$I_C = 100\ \mu$A $V_{CE} = -10$ V
h_{FE}	DC Pulse Current Gain [Note 4]	30	40		70	150			$I_C = 1.0$ mA $V_{CE} = -10$ V
h_{FE}	DC Pulse Current Gain [Note 4]	40	45	400	80	150	300		$I_C = 10$ mA $V_{CE} = -10$ V
C_{obo}	Common-Base, Open Circuit Output Capacitance (f = 1.0 MHz)		2.5	4.0		2.5	4.0	pF	$V_{CB} = -20$ V $I_E = 0$

Additional Electrical Characteristics on page 2

* Planar is a patented Fairchild process.

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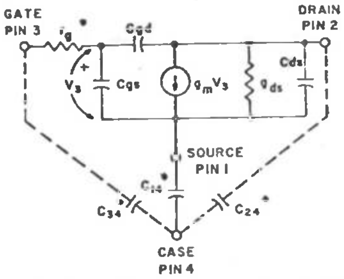
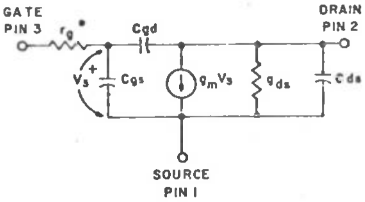
EQUIVALENT CIRCUIT



Approximate small signal equivalent circuit for the 2N4416 Field Effect Transistor.



Approximate small signal equivalent circuit for the 2N4417 Field Effect Transistor.

The 2N4416 and 2N4417 transistors are identical in every respect except for their respective package configurations. Therefore capacitance values for C_{14}, C_{24} and C_{34} should be set equal to zero, in equation 1 through 4, when computing the y parameters for the 2N4417. All of the other circuit component values are the same for both devices. Typical component values for C_{gs}, C_{gd}, g_m, and g_{ds} may be obtained for any set of bias conditions, from the curves.

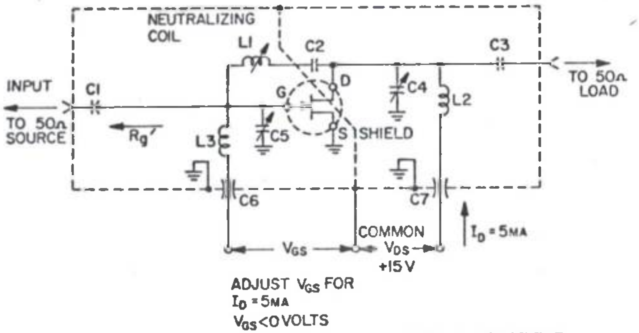
1. $y_{is} \simeq r_g[\omega(C_{gs} + C_{gd})]^2 + j\omega(C_{34} + C_{gs} + C_{gd})$
2. $y_{rs} \simeq -\omega^2 C_{gd} (C_{gs} + C_{gd}) r_g - j\omega C_{gd}$
3. $y_{fs} \simeq g_m - \omega^2 C_{gd} (C_{gs} + C_{gd}) r_g - j\omega[C_{gd} + (C_{gs} + C_{gd}) r_g g_m]$
4. $y_{os} \simeq g_{ds} + (\omega C_{gd})^2 r_g + j\omega(C_{24} + C_{gd} + C_{ds})$

Small signal common source y parameter equations for the 2N4416 and 2N-4417 Field Effect Transistors.

NOTES:

1. The above equations are accurate to about 1 GHz and are good for both the 2N4416 and 2N4417 Field Effect Transistors.
2. The case is connected to the source for the common source configuration and to the gate for common gate operation.
3. C_{14}, C_{24} and C_{34} are pin to case capacitances for the TO-72 header $C_{14} \simeq 0.6$ pF, $C_{24} \simeq 0.6$ pF, $C_{34} \simeq 0.7$ pF.
4. $C_{ds} \simeq 0.1$ pF.
5. $r_g \simeq 24$ ohms for both the 2N4416 and 2N-4417 Field Effect Transistors.
6. $g_m = |y_{fs}|$ at 1000 Hz.
7. $g_{ds} = |y_{os}|$ at 1000 Hz.
8. All references to 2N4416 are applicable to 2N4416A.

TEST CIRCUIT



100 MHz & 400 MHz NEUTRALIZED AMPLIFIER

FIGURE 22

REF. DESIG.	VALUE	
	100 MHz	400 MHz
C1	7.0 pF	1.8 pF
C2	1000 pF	27 pF
C3	3.0 pF	1.0 pF
C4	1.0-12 pF	0.8-8 pF
C5	1.0-12 pF	0.8-8 pF
C6	0.0015 μF	0.001 μF
C7	0.0015 μF	0.001 μF
L1	3.0 μH	0.2 μH
L2	0.25 μH	0.03 μH
L3	0.14 μH	0.022 μH

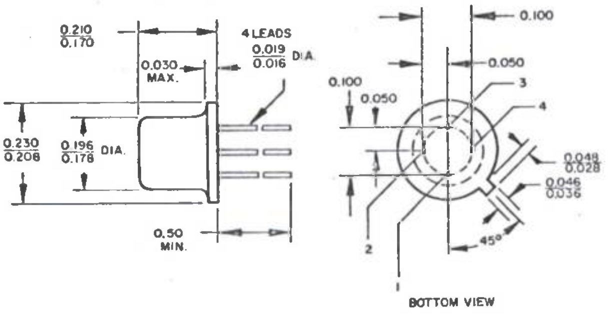
NOTES

1. Amplifier used to measure power gain and noise figure.
2. Transformed equivalent Source resistance (Rg′) is 1000 Ω at 100 MHz for 100 MHz amplifier, and 1000 Ω at 400 MHz for 400 MHz amplifier.
3. When using 2N4416, pin 4 (case) should be grounded.
4. All references to 2N4416 are applicable to 2N4416A.

MECHANICAL DATA

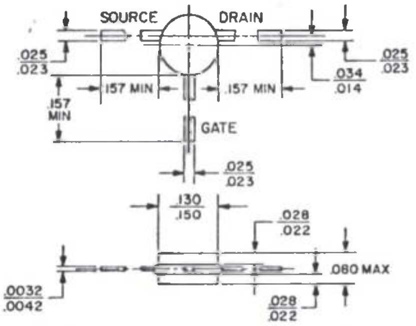
All dimensions in inches unless otherwise noted

2N4416-16A: JEDEC TO-72



TERMINAL
CONNECTIONS
1—Source
2—Drain
3—Gate
4—Case

2N4417: Union Carbide CC-3



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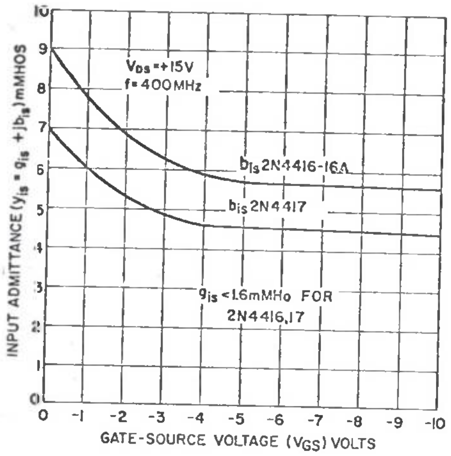
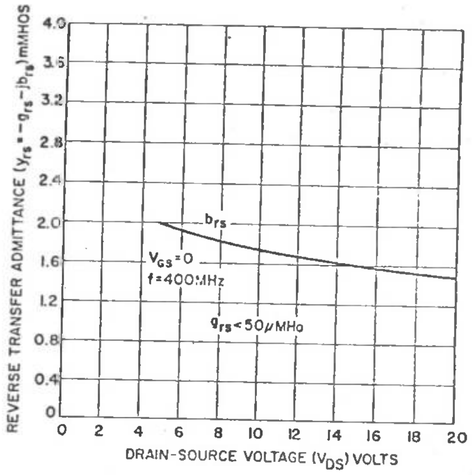
HIGH FREQUENCY COMMON SOURCE CHARACTERISTICS



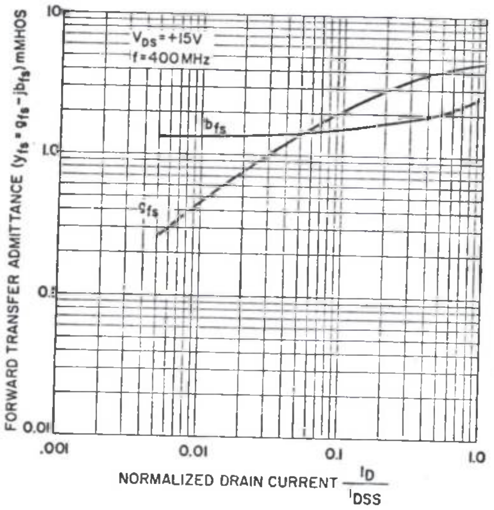
INPUT ADMITTANCE
VS.
GATE-SOURCE VOLTAGE

FIGURE 16



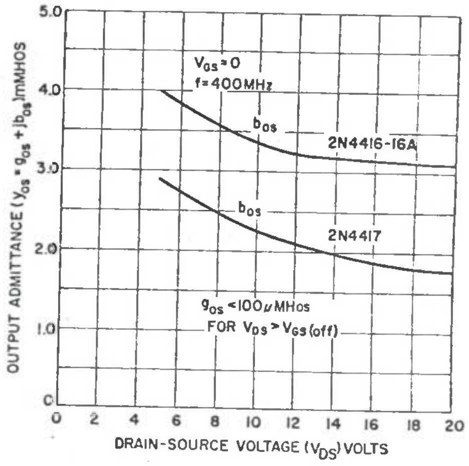
REVERSE TRANSFER ADMITTANCE
VS.
DRAIN-SOURCE VOLTAGE

FIGURE 17



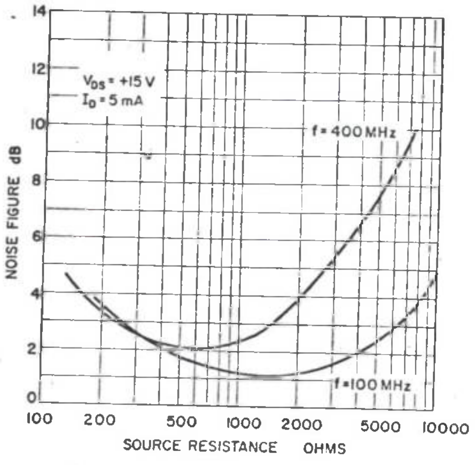
FORWARD TRANSFER ADMITTANCE
VS.
NORMALIZED DRAIN CURRENT

FIGURE 18



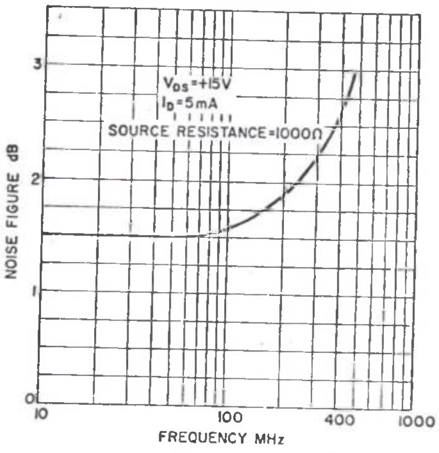
OUTPUT ADMITTANCE
VS.
DRAIN SOURCE VOLTAGE

FIGURE 19



NOISE FIGURE
VS.
SOURCE RESISTANCE

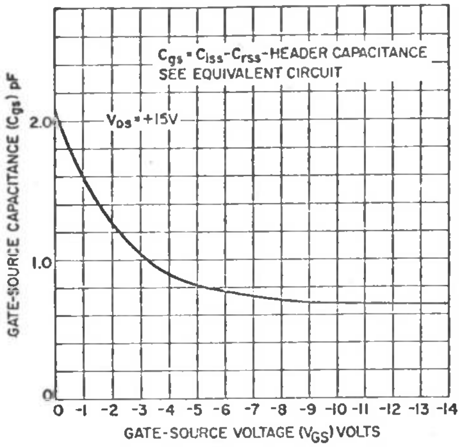
FIGURE 20



NOISE FIGURE
VS.
FREQUENCY

FIGURE 21

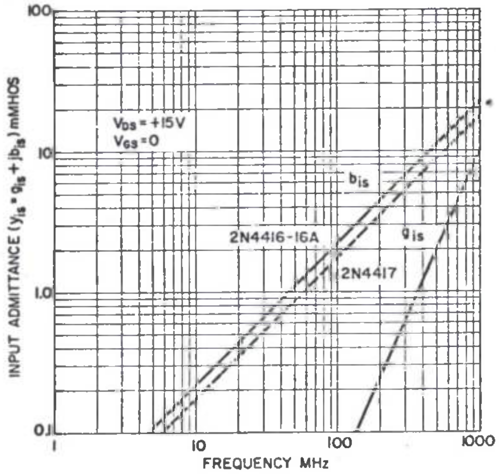
CAPACITANCE VOLTAGE CHARACTERISTIC



GATE-SOURCE CAPACITANCE
VS.
GATE-SOURCE VOLTAGE

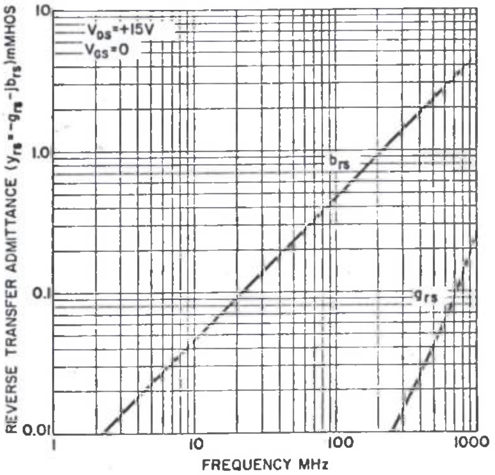
.FIGURE 11

HIGH FREQUENCY COMMON SOURCE CHARACTERISTICS



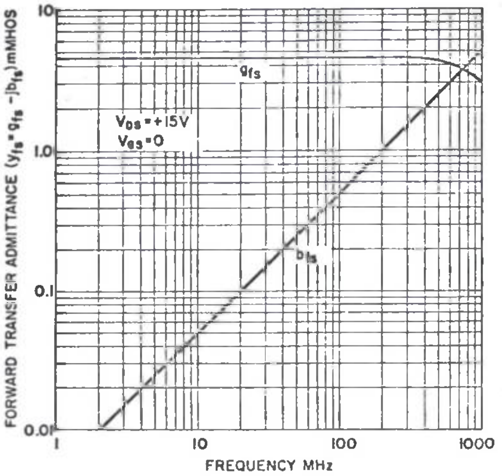
INPUT ADMITTANCE
VS.
FREQUENCY

FIGURE 12



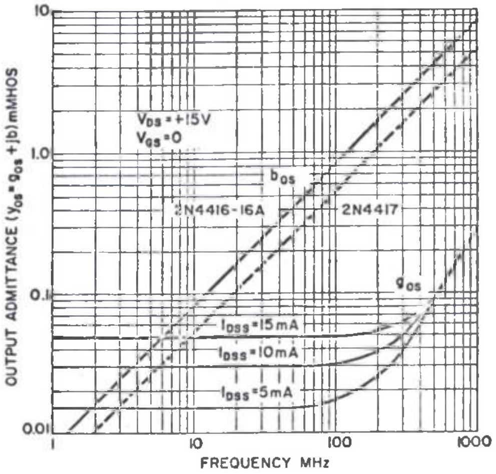
REVERSE TRANSFER ADMITTANCE
VS.
FREQUENCY

FIGURE 13



FORWARD TRANSFER ADMITTANCE
VS.
FREQUENCY

FIGURE 14

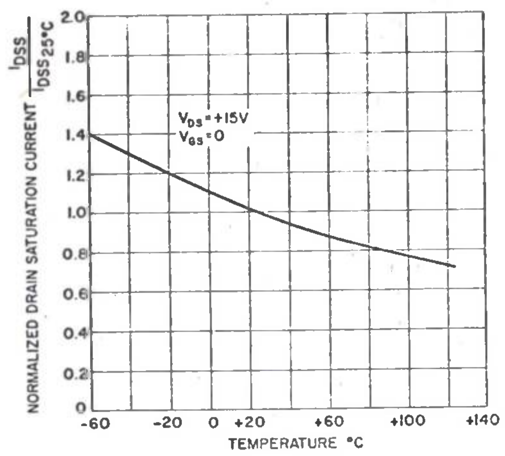


OUTPUT ADMITTANCE
VS.
FREQUENCY

FIGURE 15

N U.S.A.

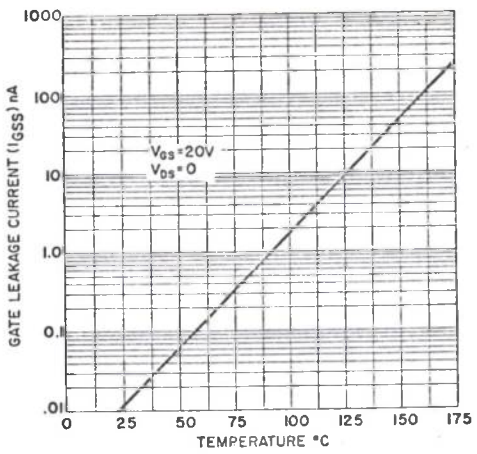
DRAIN CHARACTERISTIC



NORMALIZED DRAIN SATURATION CURRENT
VS.
TEMPERATURE

FIGURE 5

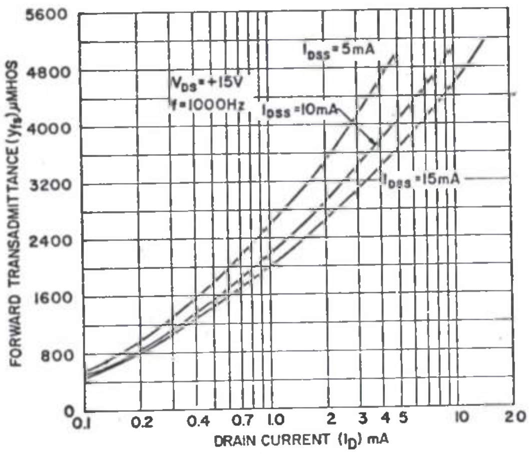
LEAKAGE CHARACTERISTIC



GATE LEAKAGE CURRENT
VS.
TEMPERATURE

FIGURE 6

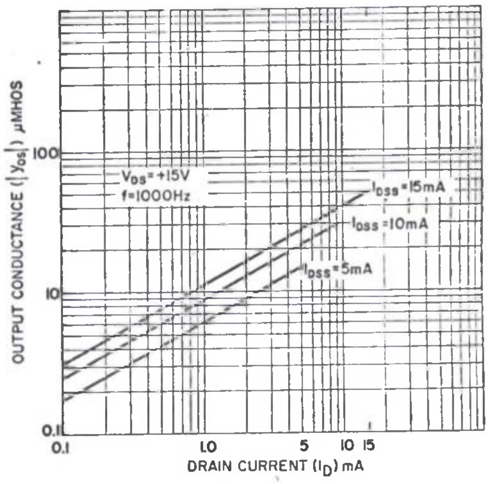
TRANSFER CHARACTERISTIC



FORWARD TRANSADMITTANCE
VS.
DRAIN CURRENT

FIGURE 7

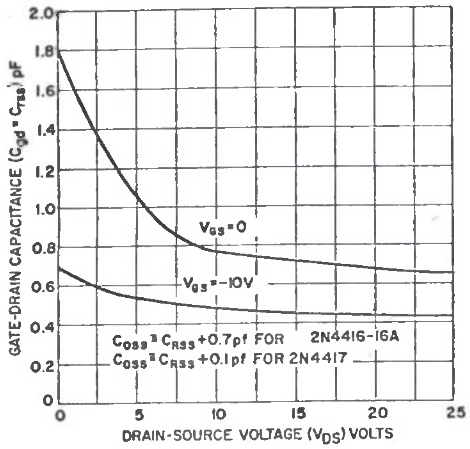
OUTPUT CHARACTERISTIC



OUTPUT CONDUCTANCE
VS.
DRAIN CURRENT

FIGURE 8

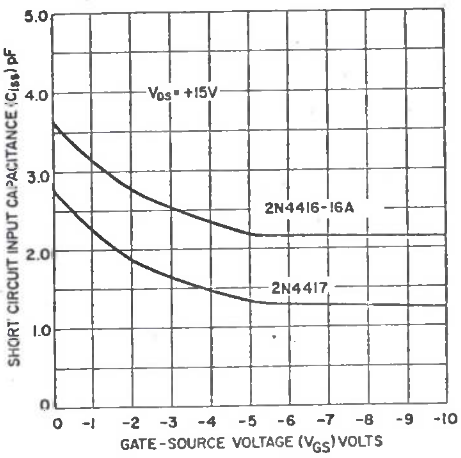
CAPACITANCE VOLTAGE CHARACTERISTIC



GATE-DRAIN CAPACITANCE
VS.
DRAIN SOURCE VOLTAGE

FIGURE 9

CAPACITANCE VOLTAGE CHARACTERISTIC



SHORT CIRCUIT INPUT CAPACITANCE
VS.
GATE-SOURCE VOLTAGE

FIGURE 10

ELECTRICAL CHARACTERISTICS

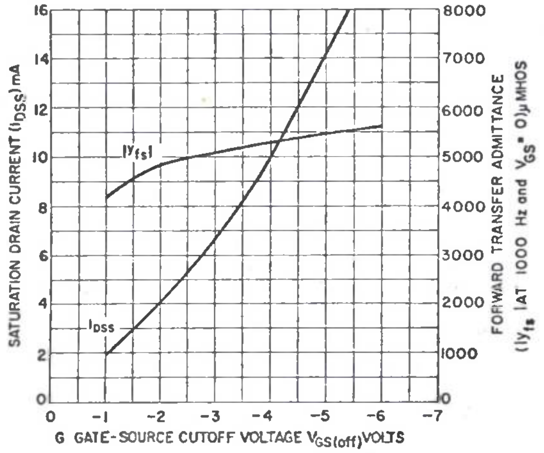
@ 25°C (UNLESS OTHERWISE NOTED)

	SYM.	2N4416 —16 A		2N4417		Units	CONDITIONS
		min.	max.	min.	max.		
Small-Signal, Common-Source, Short-Circuit Output Susceptance	IM (y_{os})		4000		3000	μmhos	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 400 MHz
Small-Signal, Common-Source, Short-Circuit Output Conductance	RE (y_{os})		75		75	μmhos	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 100 MHz
Small-Signal, Common-Source, Short-Circuit Output Susceptance	IM (y_{os})		1000		800	μmhos	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 100 MHz
Small-Signal, Common-Source, Short-Circuit Forward Transconductance	RE (y_{fs})	4000		4000		μmhos	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 400 MHz
Common-Source Power Gain	G_{ps}	10		10		dB	$V_{DS} = 15$ V, $I_D = 5$ mA, f = 400 MHz (See Fig. 1)
Common-Source Power Gain	G_{ps}	18		18		dB	$V_{DS} = 15$ V, $I_D = 5$ mA, f = 100 MHz (See Fig. 22)
Common-Source Spot Noise Figure	NF		4.0		4.0	dB	$V_{DS} = 15$ V, $I_D = 5$ mA, f = 400 MHz (See Fig. 22) $R_G = 1000$ ohms
Common-Source Spot Noise Figure	NF		2.0		2.0	dB	$V_{DS} = 15$ V, $I_D = 5$ mA, f = 100 MHz (See Fig. 22) $R_G = 1000$ ohms

TYPICAL PERFORMANCE CURVES

@ 25°C (UNLESS OTHERWISE NOTED)

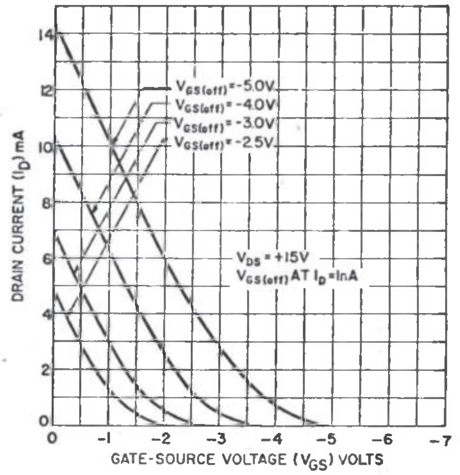
PARAMETER INTER-RELATIONSHIP



SATURATION DRAIN CURRENT
AND FORWARD TRANSFER ADMITTANCE
VS.
GATE-SOURCE CUTOFF VOLTAGE

FIGURE 1

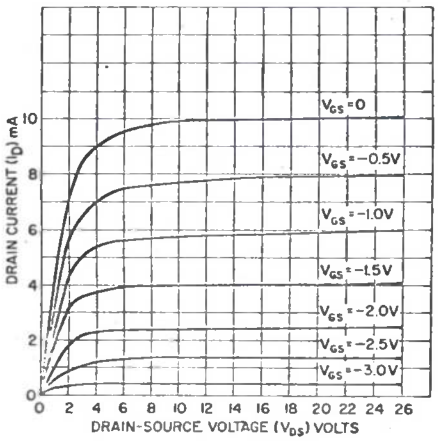
TRANSFER CHARACTERISTIC



DRAIN CURRENT
VS.
GATE-SOURCE VOLTAGE

FIGURE 2

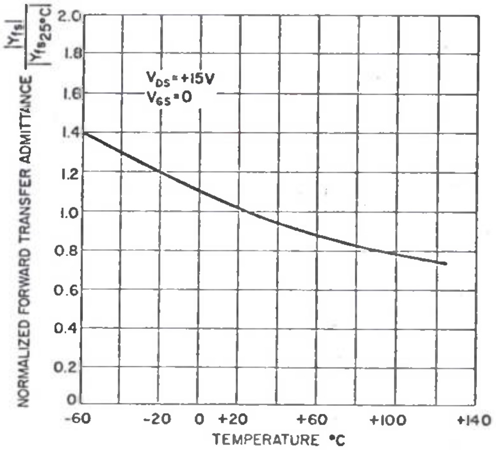
DRAIN CHARACTERISTIC



DRAIN CURRENT
VS.
DRAIN-SOURCE VOLTAGE

FIGURE 3

TRANSFER CHARACTERISTIC



NORMALIZED FORWARD TRANSFER
ADMITTANCE
VS.
TEMPERATURE

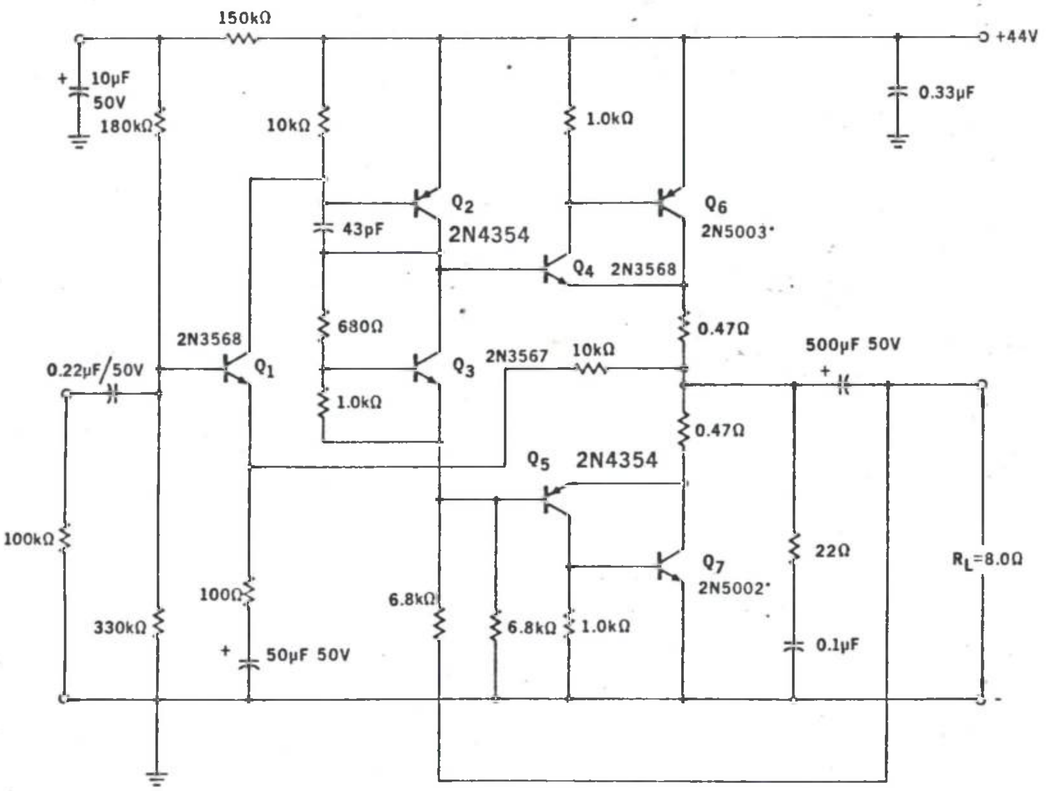
FIGURE 4

PICAL SMALL SIGNAL CHARACTERISTICS ($f = 1$ kHz)

SYMBOL	CHARACTERISTICS	TYP.	UNITS	TEST CONDITIONS	
h_{ie}	Input Resistance	800	Ω	$I_C = 10$ mA	$V_{CE} = -10$ V
h_{oe}	Output Conductance	75	µmho	$I_C = 10$ mA	$V_{CE} = -10$ V
h_{re}	Voltage Feedback Ratio	180	$X10^{-6}$	$I_C = 10$ mA	$V_{CE} = -10$ V
h_{fe}	Small Signal Current Gain	140		$I_C = 10$ mA	$V_{CE} = -10$ V

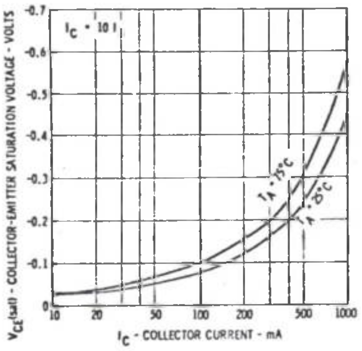
TYPICAL 25 WATT POWER AMPLIFIER

USING THE 2N4354 IN THE DRIVER STAGES

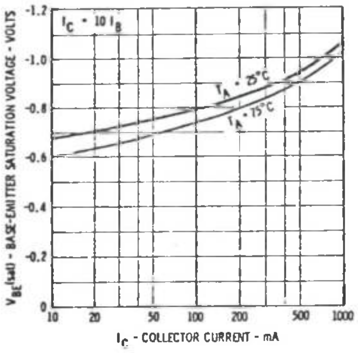


*OR EQUIVALENT SILICON OUTPUT TRANSISTOR

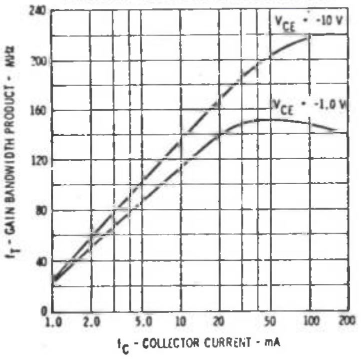
COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



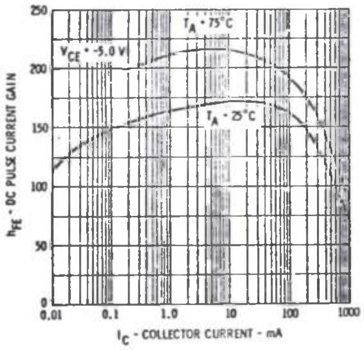
BASE SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



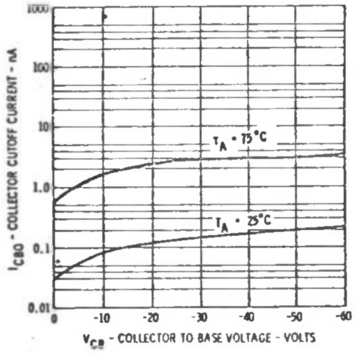
GAIN BANDWIDTH PRODUCT VERSUS COLLECTOR CURRENT



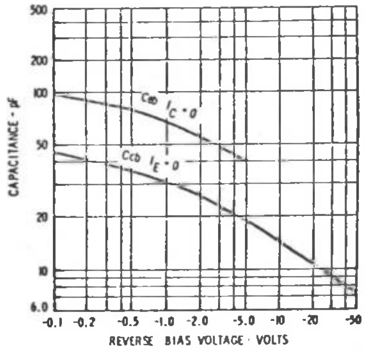
DC PULSE CURRENT GAIN VERSUS COLLECTOR CURRENT



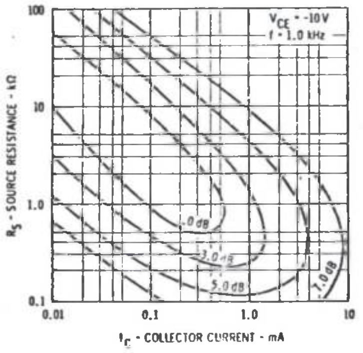
COLLECTOR CUTOFF CURRENT VERSUS REVERSE BIAS VOLTAGE



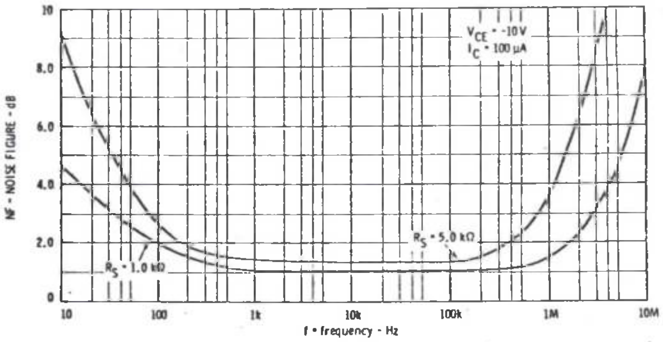
COMMON BASE OPEN CIRCUIT INPUT AND OUTPUT CAPACITANCE VERSUS REVERSE BIAS VOLTAGE



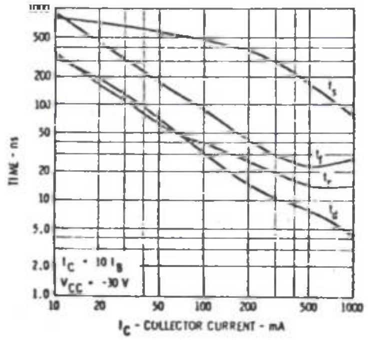
CONTOURS OF CONSTANT NARROW BAND NOISE FIGURE



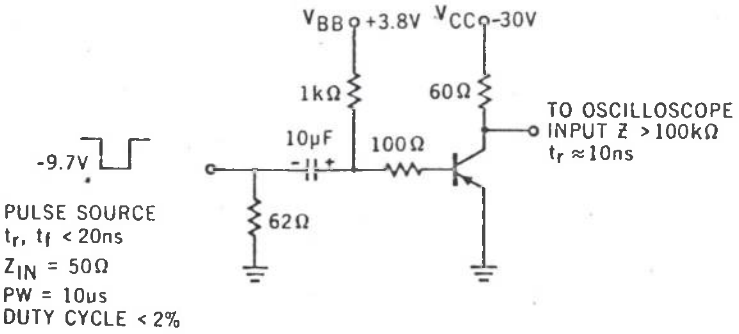
NOISE FIGURE VERSUS FREQUENCY



SWITCHING TIMES VERSUS COLLECTOR CURRENT



t_{on} AND t_{off} TEST CIRCUIT



TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

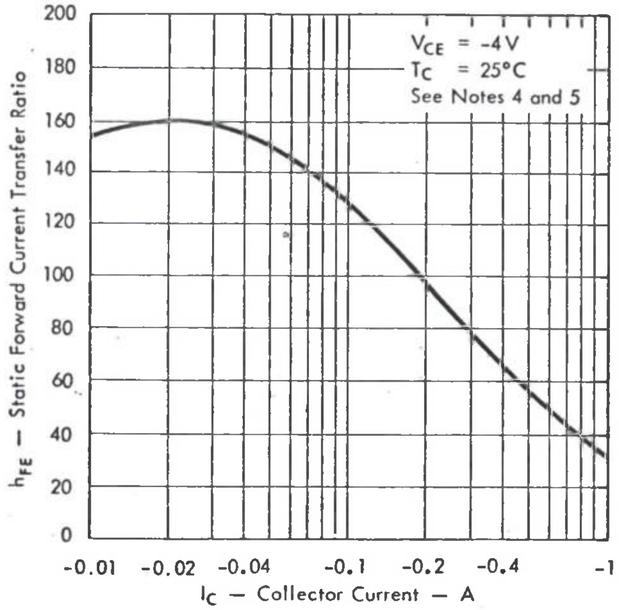


FIGURE 3

BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

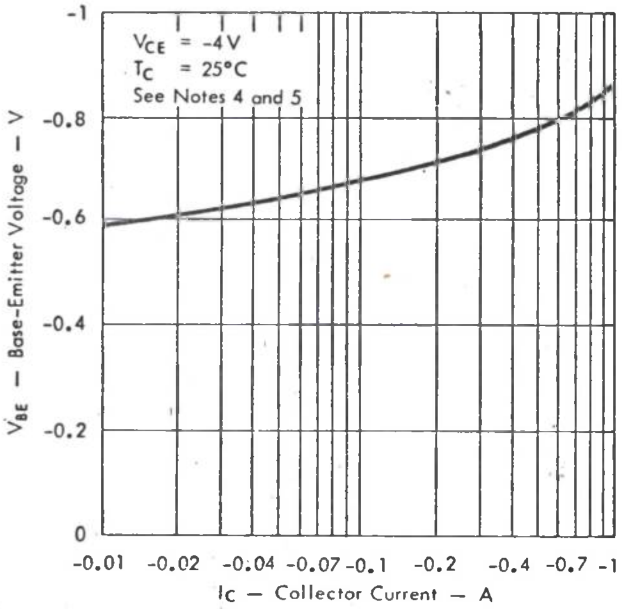


FIGURE 4

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

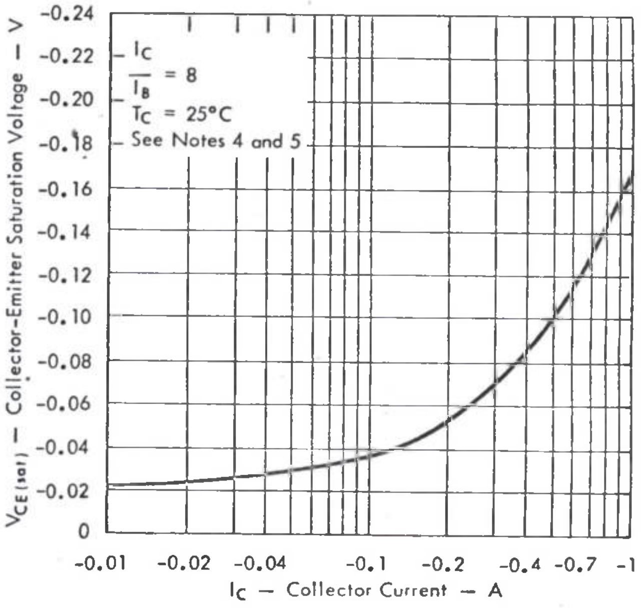


FIGURE 5

NOTES: 4. These parameters must be measured using pulse techniques. $t_p \leq 300\ \mu s$, duty cycle $\leq 2\%$.
Pulse width must be such that halving or doubling does not cause a change greater than the required accuracy of the measurement.
5. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

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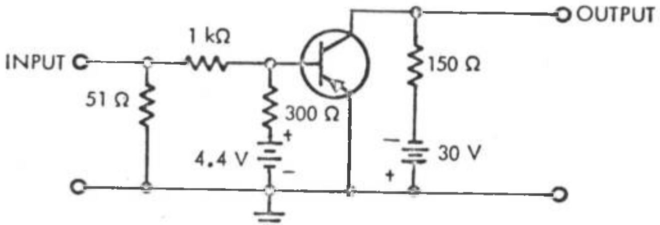
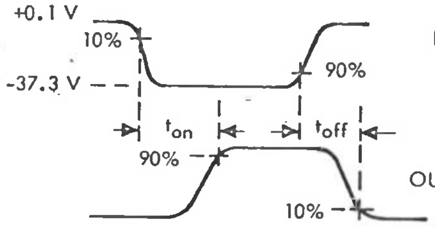
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

NOTES:
a. The input waveform is supplied by a generator with the following characteristics: $t_r \le 15$ ns, $t_f \le 15$ ns, $Z_{out} = 50\ \Omega$, $t_p = 10\ \mu s$, duty cycle $\le 2\%$.
b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \le 15$ ns, $R_{in} \ge 10\ M\Omega$, $C_{in} \le 11.5$ pF.
c. Resistors must be noninductive types.
d. The d-c power supplies may require additional bypassing in order to minimize ringing.

MAXIMUM SAFE OPERATING REGION

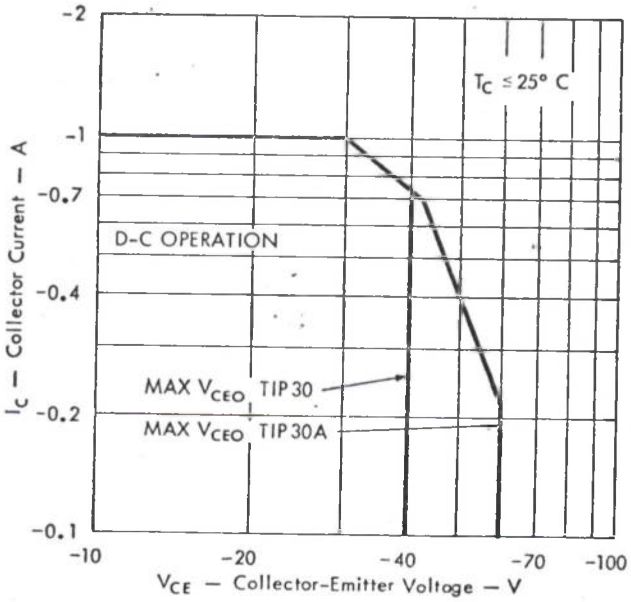


FIGURE 2

TYPES TIP30, TIP30A
P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS	TIP30		TIP30A		UNIT
			MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = -30$ mA, $I_B = 0$, See Note 4	−40		−60		V
I_{CEO}	Collector Cutoff Current	$V_{CE} = -30$ V, $I_B = 0$		−0.3		−0.3	mA
I_{CES}	Collector Cutoff Current	$V_{CE} = -40$ V, $V_{BE} = 0$		−0.2			mA
		$V_{CE} = -60$ V, $V_{BE} = 0$				−0.2	
I_{EBO}	Emitter Cutoff Current	$V_{EB} = -5$ V, $I_C = 0$		−1		−1	mA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = -4$ V, $I_C = -0.2$ A, See Notes 4 and 5	40	200	40	200	
		$V_{CE} = -4$ V, $I_C = -1$ A, See Notes 4 and 5	10		10		
V_{BE}	Base-Emitter Voltage	$V_{CE} = -4$ V, $I_C = -1$ A, See Notes 4 and 5		−1.3		−1.3	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = -125$ mA, $I_C = -1$ A, See Notes 4 and 5		−0.7		−0.7	V
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10$ V, $I_C = -0.2$ A, $f = 1$ kHz	20		20		
$\lvert h_{fe} \rvert$	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10$ V, $I_C = -0.2$ A, $f = 1$ MHz	3		3		

NOTES: 4. These parameters must be measured using pulse techniques. $t_p \leq 300$ μs, duty cycle $\leq 2\%$.
Pulse width must be such that halving or doubling does not cause a change greater than the required accuracy of the measurement.

5. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER		MAX	UNIT
$\theta_{J\text{-}C}$	Junction-to-Case Thermal Resistance	4.17	deg/W
$\theta_{J\text{-}A}$	Junction-to-Free-Air Thermal Resistance	62.5	

switching characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS†	TYP	UNIT
t_{on}	Turn-On Time	$I_C = -200$ mA, $I_{B(1)} = -20$ mA, $I_{B(2)} = 20$ mA, $V_{BE(off)} = 3.4$ V, $R_L = 150\ \Omega$, See Figure 1	0.25	μs
t_{off}	Turn-Off Time		0.90	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

TIP 30

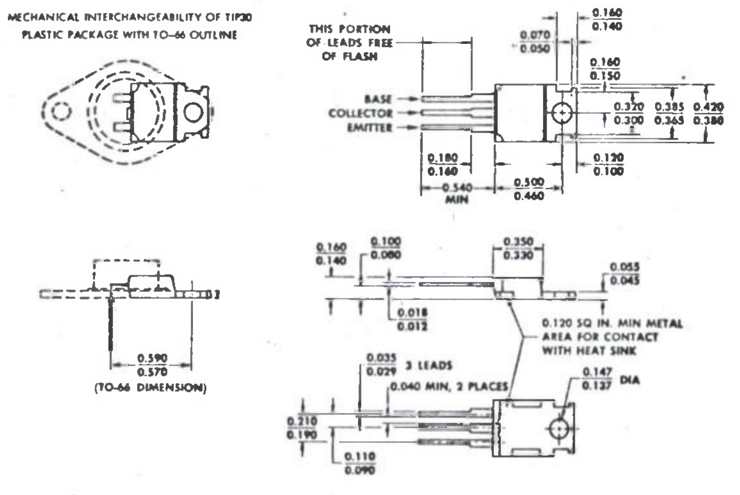
TYPES TIP30, TIP30A
BULLETIN NO. DL-S 6810956, JULY 1968

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS DESIGNED FOR COMPLEMENTARY USE WITH TIP29, TIP29A

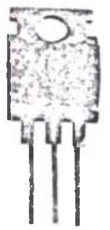
- **30 Watts at 25°C Case Temperature**
- **1 A Rated Collector Current**
- **Min f_T of 3 MHz at 10 V, 200 mA**

mechanical data

THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE MOUNTING TAB



ALL DIMENSIONS ARE IN INCHES



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP30	TIP30A
Collector-Base Voltage	−40 V	−60 V
Collector-Emitter Voltage (See Note 1)	−40 V	−60 V
Emitter-Base Voltage	← −5 V →	
Continuous Collector Current	← −1 A →	
Continuous Base Current	← −0.4 A →	
Safe Operating Region at (or below) 25°C Case Temperature	See Figure 2	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	← 30 W →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	← 2 W →	
Operating Collector Junction Temperature Range	−65°C to 150°C	
Storage Temperature Range	−65°C to 150°C	
Lead Temperature ⅛ Inch from Case for 10 Seconds	← 260°C →	

NOTES: 1. These values apply when the base-emitter diode is open-circuited.
2. Derate linearly to 150°C case temperature at the rate of 0.24 W/deg.
3. Derate linearly to 150°C free-air temperature at the rate of 16 mW/deg.

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TYPES TIP34, ~~TIP34A~~, TIP34B, TIP34C
P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

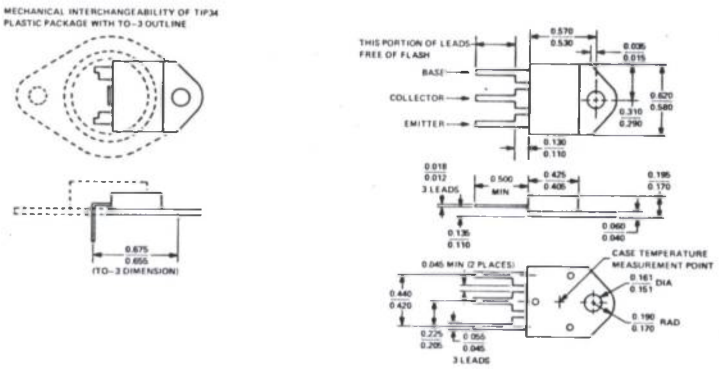
TYPES TIP34, TIP34A, TIP34B, TIP34C
BULLETIN NO. DL-S 7011405, DECEMBER 1970
REPLACES BULLETIN NO. DL-S 6810958, JULY 1968

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP33, TIP33A, TIP33B, TIP33C

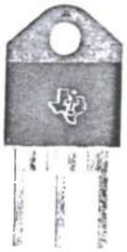
- 80 W at 25°C Case Temperature
- 10 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 500 mA

mechanical data

THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE MOUNTING TAB



ALL DIMENSIONS ARE IN INCHES



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP34	TIP34A	TIP34B	TIP34C
Collector-Base Voltage	−40 V	−60 V	−80 V	−100 V
Collector-Emitter Voltage (See Note 1)	−40 V	−60 V	−80 V	−100 V
Emitter-Base Voltage	−5 V			
Continuous Collector Current	−10 A			
Peak Collector Current (See Note 2)	−15 A			
Continuous Base Current	−3 A			
Safe Operating Region at (or below) 25°C Case Temperature	See Figure 5			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	80 W			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	3.5 W			
Unclamped Inductive Load Energy (See Note 5)	62.5 mJ			
Operating Collector Junction Temperature Range	−65°C to 150°C			
Storage Temperature Range	−65°C to 150°C			
Lead Temperature 1/8 Inch from Case for 10 Seconds	260°C			

NOTES:
1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_w \leqslant 0.3$ ms, duty cycle $\leqslant 10\%$.
3. Derate linearly to 150°C case temperature at the rate of 0.64 W/°C.
4. Derate linearly to 150°C free-air temperature at the rate of 28 mW/°C.
5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB1} = 100\ \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1\ \Omega$, $V_{CC} = 10$ V. Energy $\approx 1/2\ I_C{}^2 L/2$.

TYPES TIP34, TIP34A, TIP34B, TIP34C
P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS	TIP34		TIP34A		TIP34B		TIP34C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = -30$ mA, $I_B = 0$, See Note 6	−40		−60		−80		−100		V
I_{CEO}	Collector Cutoff Current	$V_{CE} = -30$ V, $I_B = 0$		−0.7		−0.7					mA
		$V_{CE} = -60$ V, $I_B = 0$						−0.7		−0.7	
I_{CES}	Collector Cutoff Current	$V_{CE} = -40$ V, $V_{BE} = 0$		−0.4							mA
		$V_{CE} = -60$ V, $V_{BE} = 0$				−0.4					
		$V_{CE} = -80$ V, $V_{BE} = 0$						−0.4			
		$V_{CE} = -100$ V, $V_{BE} = 0$								−0.4	
I_{EBO}	Emitter Cutoff Current	$V_{EB} = -5$ V, $I_C = 0$		−1		−1		−1		−1	mA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = -4$ V, $I_C = -1$ A, See Notes 6 and 7	40		40		40		40		
		$V_{CE} = -4$ V, $I_C = -3$ A, See Notes 6 and 7	20	100	20	100	20	100	20	100	
V_{BE}	Base-Emitter Voltage	$V_{CE} = -4$ V, $I_C = -3$ A, See Notes 6 and 7		−1.6		−1.6		−1.6		−1.6	V
		$V_{CE} = -4$ V, I_C −10 A, See Notes 6 and 7		−3		−3		−3		−3	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = -0.3$ A, $I_C = -3$ A, See Notes 6 and 7		−1		−1		−1		−1	V
		$I_B = -2.5$ A, $I_C = -10$ A, See Notes 6 and 7		−4		−4		−4		−4	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10$ V, $I_C = -0.5$ A, f = 1 kHz	20		20		20		20		
$\|h_{fe}\|$	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10$ V, $I_C = -0.5$ A, f = 1 MHz	3		3		3		3		

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300\ \mu s$, duty cycle ⩽ 2%.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

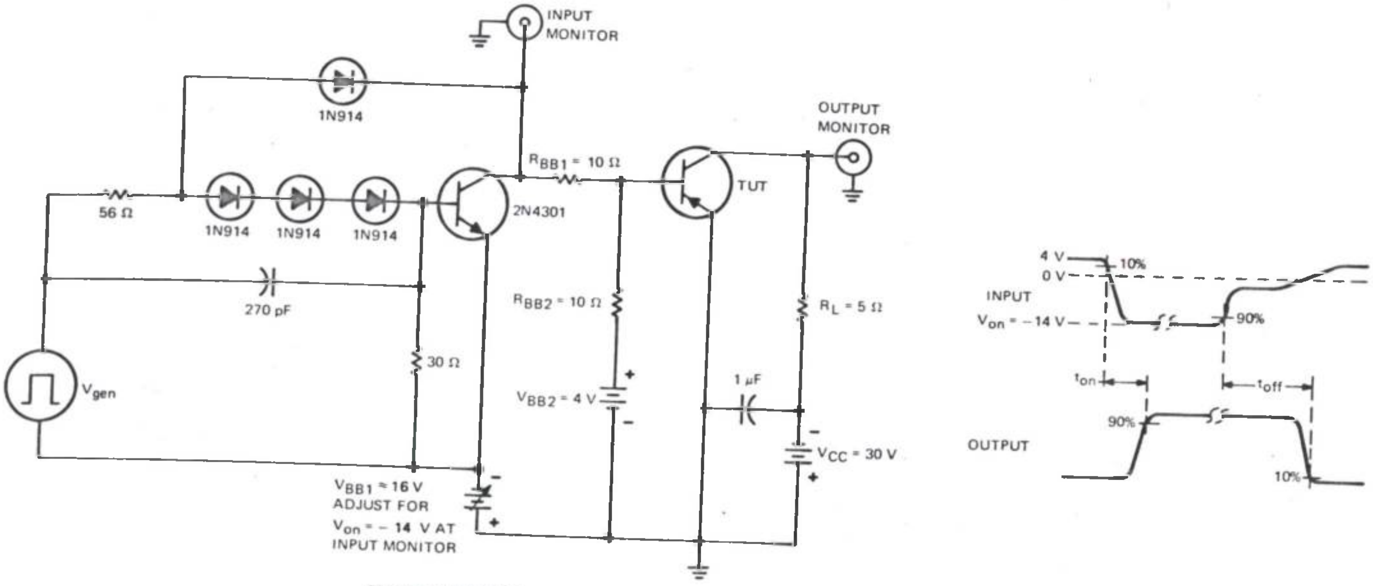
PARAMETER		MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	1.56	°C/W
$R_{\theta JA}$	Junction-to-Free-Air Thermal Resistance	35.7	

switching characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS†	TYP	UNIT
t_{on}	Turn-On Time	$I_C = -6$ A, $I_{B(1)} = -0.6$ A, $I_{B(2)} = 0.6$ A, $V_{BE(off)} = 4$ V, $R_L = 5\ \Omega$, See Figure 1	0.4	µs
t_{off}	Turn-Off Time		0.7	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



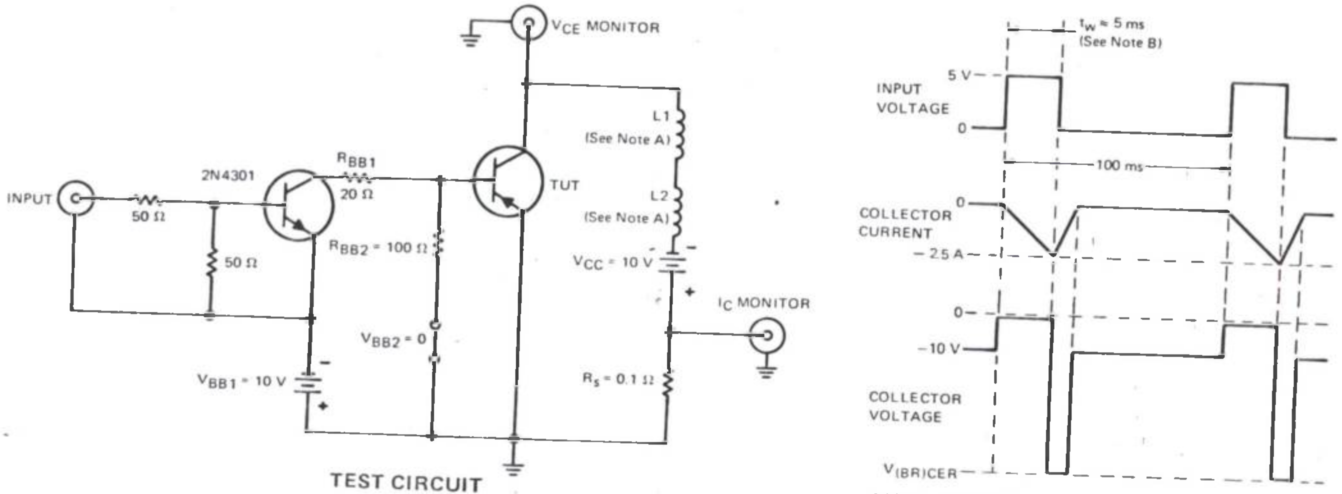
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES:
- A. V_{gen} is a 30-V pulse (from 0 V) into a 50-Ω termination.
- B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leqslant 15$ ns, $t_f \leqslant 15$ ns, $Z_{out} = 50\ \Omega$, $t_w = 20\ \mu s$, duty cycle $\leqslant 2\%$.
- C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leqslant 15$ ns, $R_{in} \geqslant 10\ M\Omega$, $C_{in} \leqslant 11.5$ pF.
- D. Resistors must be noninductive types.
- E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTES:
- A. L1 and L2 are 10 mH, 0.11 Ω, Chicago Standard Transformer Corporation C-2688, or equivalent.
- B. Input pulse width is increased until $I_{CM} = -2.5$ A.

FIGURE 2

TYPES TIP34, TIP34A, TIP34B, TIP34C
P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

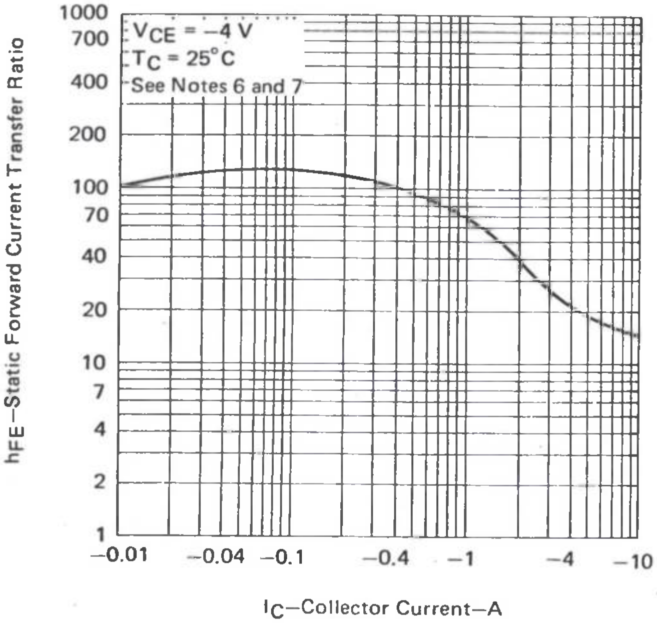


FIGURE 3

NOTES: 6. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ⩽ 2%.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

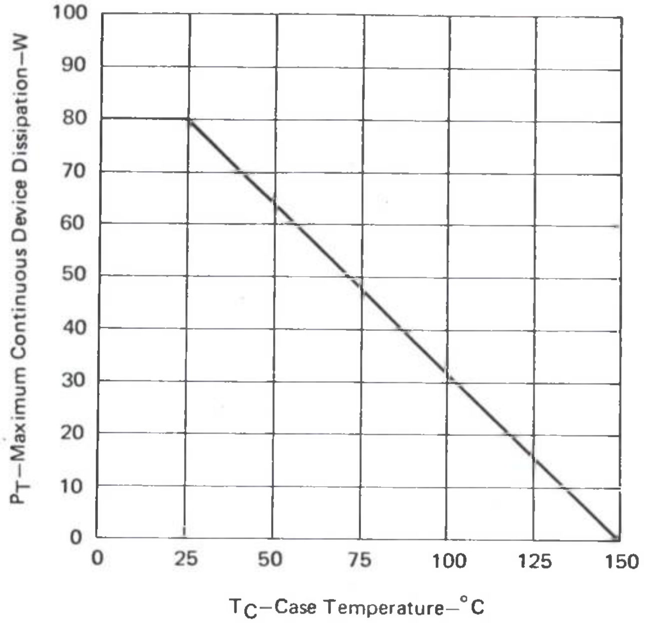


FIGURE 4

MAXIMUM SAFE OPERATING REGION

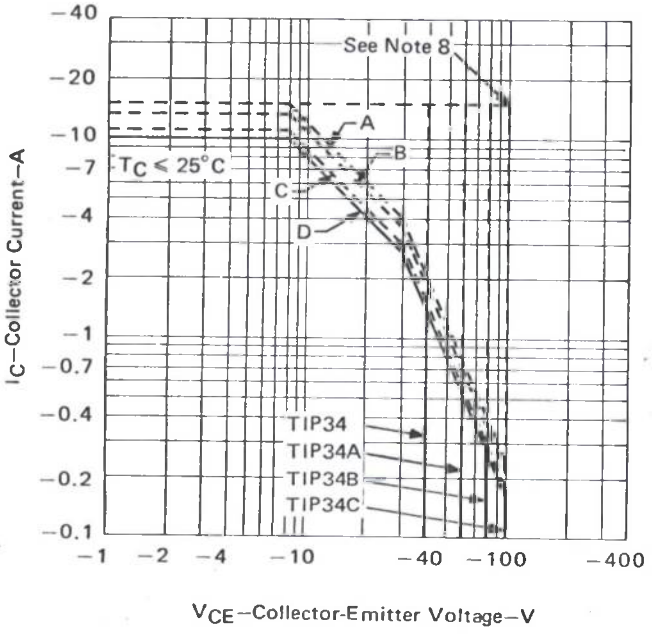


FIGURE 5

KEY FOR FIGURE 5

CURVE	CONDITIONS
A	t_w = 300 μs, d = 0.1 = 10%
B	t_w = 1 ms, d = 0.1 = 10%
C	t_w = 10 ms, d = 0.1 = 10%
D	D-C OPERATION

NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

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TYPES TIP33, TIP33A, TIP33B, TIP33C
N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

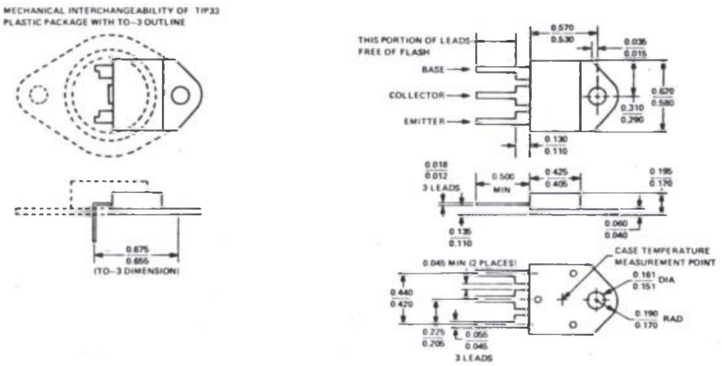
TYPES TIP33, TIP33A, TIP33B, TIP33C
BULLETIN NO. DL-S 7011404, DECEMBER 1970
REPLACES BULLETIN NO. DL-S 6810957, JULY 1968

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP34, TIP34A, TIP34B, TIP34C

- 80 W at 25°C Case Temperature
- 10 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 500 mA

mechanical data

THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE MOUNTING TAB



ALL DIMENSIONS ARE IN INCHES

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP33	TIP33A	TIP33B	TIP33C
Collector-Base Voltage	40 V	60 V	80 V	100 V
Collector-Emitter Voltage (See Note 1)	40 V	60 V	80 V	100 V
Emitter-Base Voltage	← 5 V →			
Continuous Collector Current	← 10 A →			
Peak Collector Current (See Note 2)	← 15 A →			
Continuous Base Current	← 3 A →			
Safe Operating Region at (or below) 25°C Case Temperature	← See Figure 5 →			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	← 80 W →			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	← 3.5 W →			
Unclamped Inductive Load Energy (See Note 5)	← 62.5 mJ →			
Operating Collector Junction Temperature Range	← −65°C to 150°C →			
Storage Temperature Range	← −65°C to 150°C →			
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →			

NOTES:
1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_w \leqslant 0.3$ ms, duty cycle $\leqslant 10\%$.
3. Derate linearly to 150°C case temperature at the rate of 0.64 W/°C.
4. Derate linearly to 150°C free-air temperature at the rate of 28 mW/°C.
5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB1} = 100\ \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1\ \Omega$, $V_{CC} = 10$ V. Energy $\approx I_C^2L/2$.

TEXAS INSTRUMENTS
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electrical characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS	TIP33		TIP33A		TIP33B		TIP33C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 30$ mA, $I_B = 0$, See Note 6	40		60		80		100		V
I_{CEO}	Collector Cutoff Current	$V_{CE} = 30$ V, $I_B = 0$		0.7		0.7					mA
		$V_{CE} = 60$ V, $I_B = 0$						0.7		0.7	
I_{CES}	Collector Cutoff Current	$V_{CE} = 40$ V, $V_{BE} = 0$		0.4							mA
		$V_{CE} = 60$ V, $V_{BE} = 0$				0.4					
		$V_{CE} = 80$ V, $V_{BE} = 0$						0.4			
		$V_{CE} = 100$ V, $V_{BE} = 0$								0.4	
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 5$ V, $I_C = 0$		1		1		1		1	mA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4$ V, $I_C = 1$ A, See Notes 6 and 7	40		40		40		40		
		$V_{CE} = 4$ V, $I_C = 3$ A, See Notes 6 and 7	20	100	20	100	20	100	20	100	
V_{BE}	Base-Emitter Voltage	$V_{CE} = 4$ V, $I_C = 3$ A, See Notes 6 and 7		1.6		1.6		1.6		1.6	V
		$V_{CE} = 4$ V, $I_C = 10$ A, See Notes 6 and 7		3		3		3		3	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 0.3$ A, $I_C = 3$ A, See Notes 6 and 7		1		1		1		1	V
		$I_B = 2.5$ A, $I_C = 10$ A, See Notes 6 and 7		4		4		4		4	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10$ V, $I_C = 0.5$ A, f = 1 kHz	20		20		20		20		
$\lvert h_{fe} \rvert$	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10$ V, $I_C = 0.5$ A, f = 1 MHz	3		3		3		3		

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300$ μs, duty cycle $\leqslant 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER		MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	1.56	°C/W
$R_{\theta JA}$	Junction-to-Free-Air Thermal Resistance	35.7	

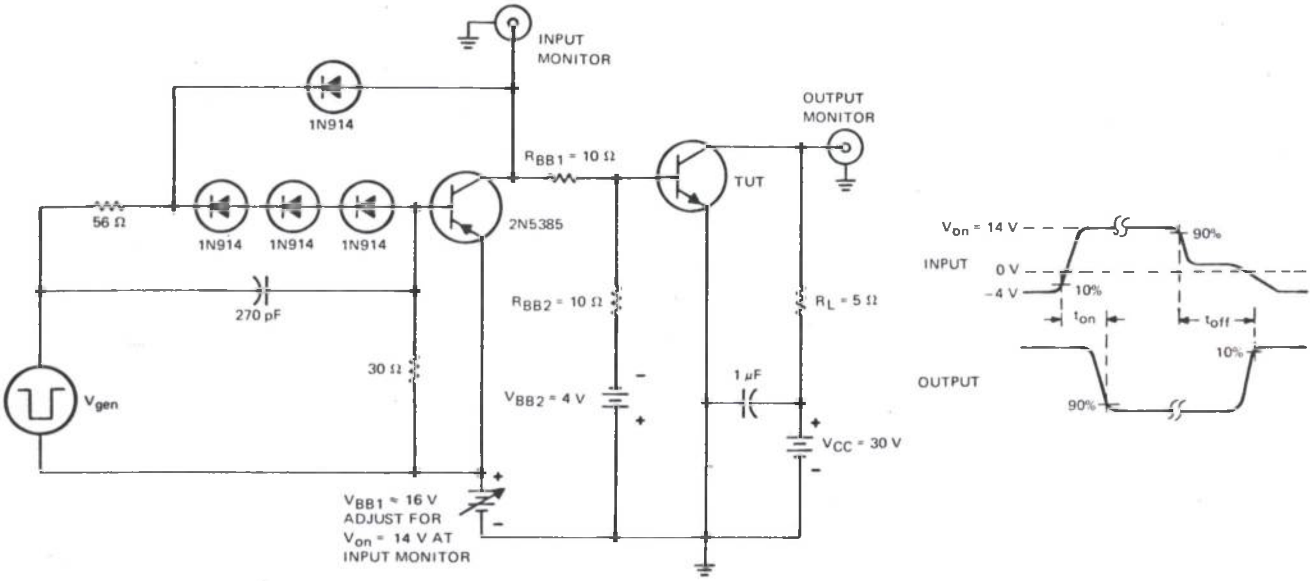
switching characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS†	TYP	UNIT
t_{on}	Turn-On Time	$I_C = 6$ A, $I_{B(1)} = 0.6$ A, $I_{B(2)} = -0.6$ A, $V_{BE(off)} = -4$ V, $R_L = 5\ \Omega$, See Figure 1	0.6	μs
t_{off}	Turn-Off Time		1	

---

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



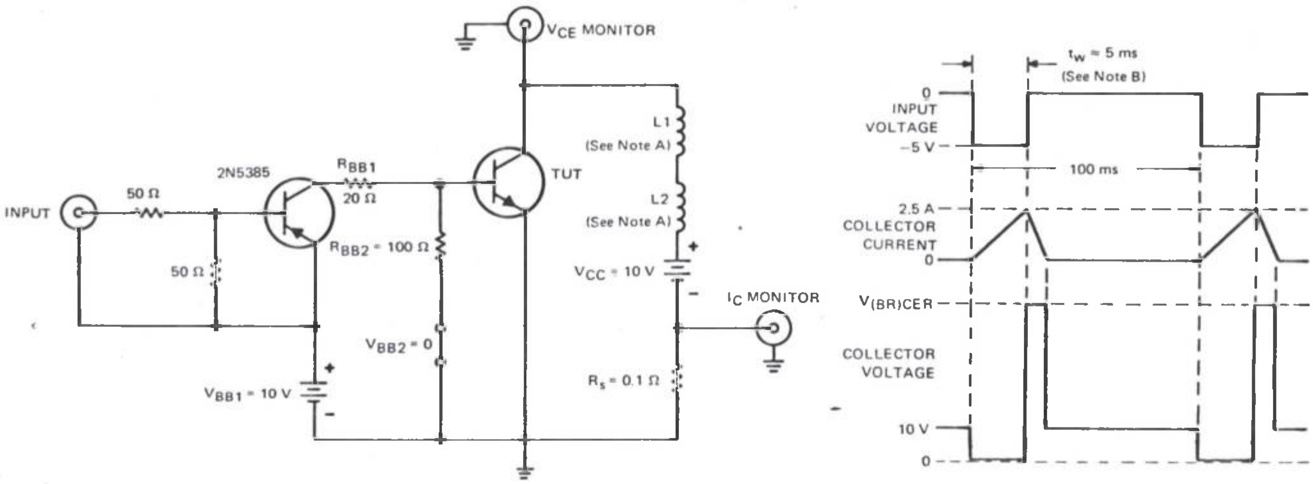
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES:
- A. V_{gen} is a −30-V pulse (from 0 V) into a 50-Ω termination.
- B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leqslant 15$ ns, $t_f \leqslant 15$ ns, $Z_{out} = 50\ \Omega$, $t_w = 20\ \mu s$, duty cycle ⩽ 2%.
- C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leqslant 15$ ns, $R_{in} \geqslant 10\ M\Omega$, $C_{in} \leqslant 11.5$ pF.
- D. Resistors must be noninductive types.
- E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTES:
- A. L1 and L2 are 10 mH, 0.11 Ω, Chicago Standard Transformer Corporation C-2688, or equivalent.
- B. Input pulse width is increased until $I_{CM} = 2.5$ A.

FIGURE 2

TYPES TIP33, TIP33A, TIP33B, TIP33C
N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

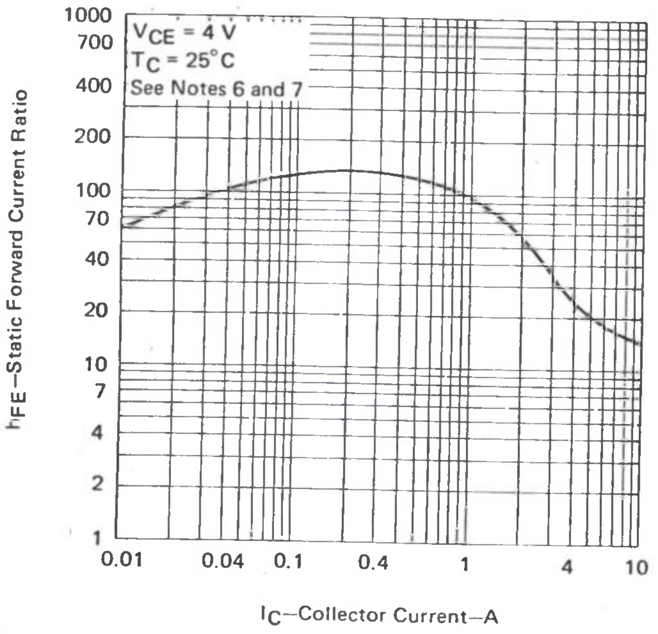


FIGURE 3

NOTES: 6. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

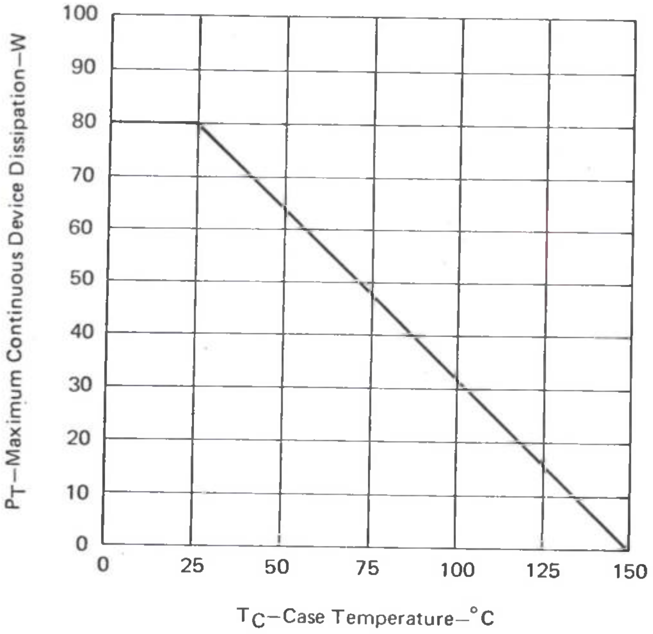


FIGURE 4

MAXIMUM SAFE OPERATING REGION

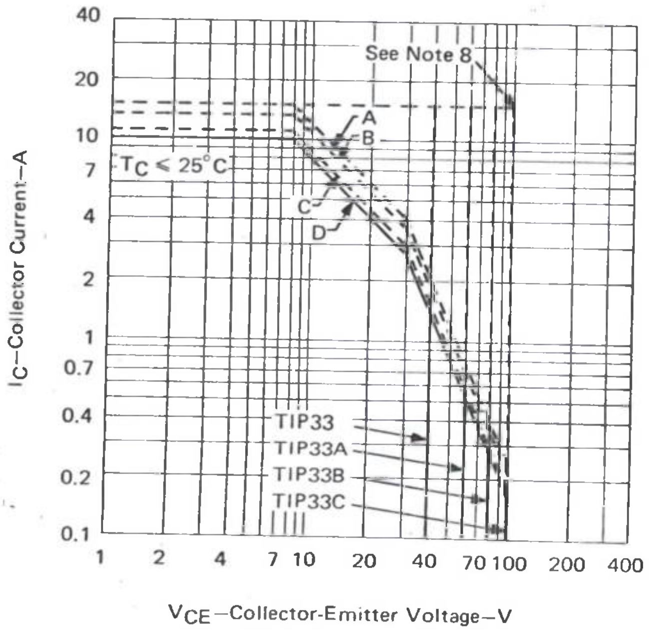


FIGURE 5

KEY FOR FIGURE 5

CURVE	CONDITIONS
A	t_w = 300 μs, d = 0.1 = 10%
B	t_w = 1 ms, d = 0.1 = 10%
C	t_w = 10 ms, d = 0.1 = 10%
D	D-C OPERATION

NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

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TYPES TIP29, TIP29A, TIP29B, TIP29C
N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

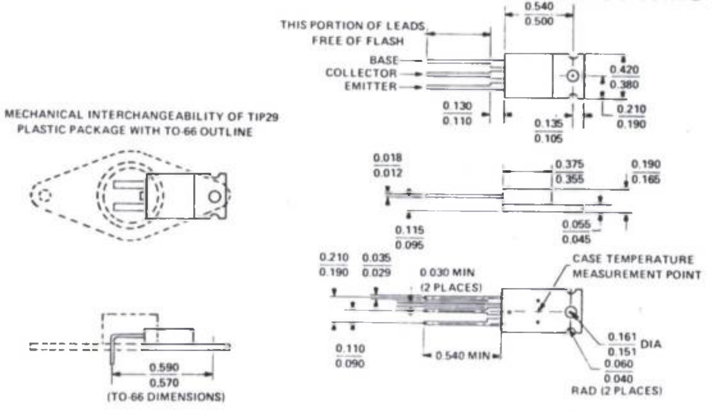
TYPES TIP29, TIP29A, TIP29B, TIP29C
BULLETIN NO. DL-S 7011371, OCTOBER 1970
REPLACES BULLETIN NO. DL-S 6810954, JULY 1968

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS DESIGNED FOR COMPLEMENTARY USE WITH TIP30, TIP30A, TIP30B, TIP30C

- 30 W at 25°C Case Temperature
- 1 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 200 mA

mechanical data

THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE MOUNTING TAB



ALL DIMENSIONS ARE IN INCHES

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP29	TIP29A	TIP29B	TIP29C
Collector-Base Voltage	40 V	60 V	80 V	100 V
Collector-Emitter Voltage (See Note 1)	40 V	60 V	80 V	100 V
Emitter-Base Voltage	5 V			
Continuous Collector Current	1 A			
Peak Collector Current (See Note 2)	3 A			
Continuous Base Current	0.4 A			
Safe Operating Region at (or below) 25°C Case Temperature	See Figure 5			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	30 W			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	2 W			
Unclamped Inductive Load Energy (See Note 5)	32 mJ			
Operating Collector Junction Temperature Range	−65°C to 150°C			
Storage Temperature Range	−65°C to 150°C			
Lead Temperature 1/8 Inch from Case for 10 Seconds	260°C			

NOTES:
1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_w \leqslant 0.3$ ms, duty cycle $\leqslant 10\%$.
3. Derate linearly to 150°C case temperature at the rate of 0.24 W/°C.
4. Derate linearly to 150°C free-air temperature at the rate of 16 mW/°C.
5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB1} = 100\ \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1\ \Omega$, $V_{CC} = 10$ V. Energy $\approx I_C{}^2L/2$.

TYPES TIP29, TIP29A, TIP29B, TIP29C
N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS	TIP29		TIP29A		TIP29B		TIP29C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 30 mA, I_B = 0, See Note 6	40		60		80		100		V
I_{CEO}	Collector Cutoff Current	V_{CE} = 30 V, I_B = 0		0.3		0.3					mA
		V_{CE} = 60 V, I_B = 0						0.3		0.3	
I_{CES}	Collector Cutoff Current	V_{CE} = 40 V, V_{BE} = 0		0.2							mA
		V_{CE} = 60 V, V_{BE} = 0				0.2					
		V_{CE} = 80 V, V_{BE} = 0						0.2			
		V_{CE} = 100 V, V_{BE} = 0								0.2	
I_{EBO}	Emitter Cutoff Current	V_{EB} = 5 V, I_C = 0		1		1		1		1	mA
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 4 V, I_C = 0.2 A, See Notes 6 and 7	40		40		40		40		
		V_{CE} = 4 V, I_C = 1 A, See Notes 6 and 7	15	75	15	75	15	75	15	75	
V_{BE}	Base-Emitter Voltage	V_{CE} = 4 V, I_C = 1 A, See Notes 6 and 7		1.3		1.3		1.3		1.3	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 125 mA, I_C = 1 A, See Notes 6 and 7		0.7		0.7		0.7		0.7	V
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	V_{CE} = 10 V, I_C = 0.2 A, f = 1 kHz	20		20		20		20		
$\|h_{fe}\|$	Small-Signal Common-Emitter Forward Current Transfer Ratio	V_{CE} = 10 V, I_C = 0.2 A, f = 1 MHz	3		3		3		3		

NOTES: 6. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER		MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	4.17	°C/W
$R_{\theta JA}$	Junction-to-Free-Air Thermal Resistance	62.5	

switching characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS†	TYP	UNIT
t_{on}	Turn-On Time	I_C = 1 A, $I_{B(1)}$ = 100 mA, $I_{B(2)}$ = −100 mA, $V_{BE(off)}$ = −4.3 V, R_L = 30 Ω, See Figure 1	0.5	μs
t_{off}	Turn-Off Time		2	

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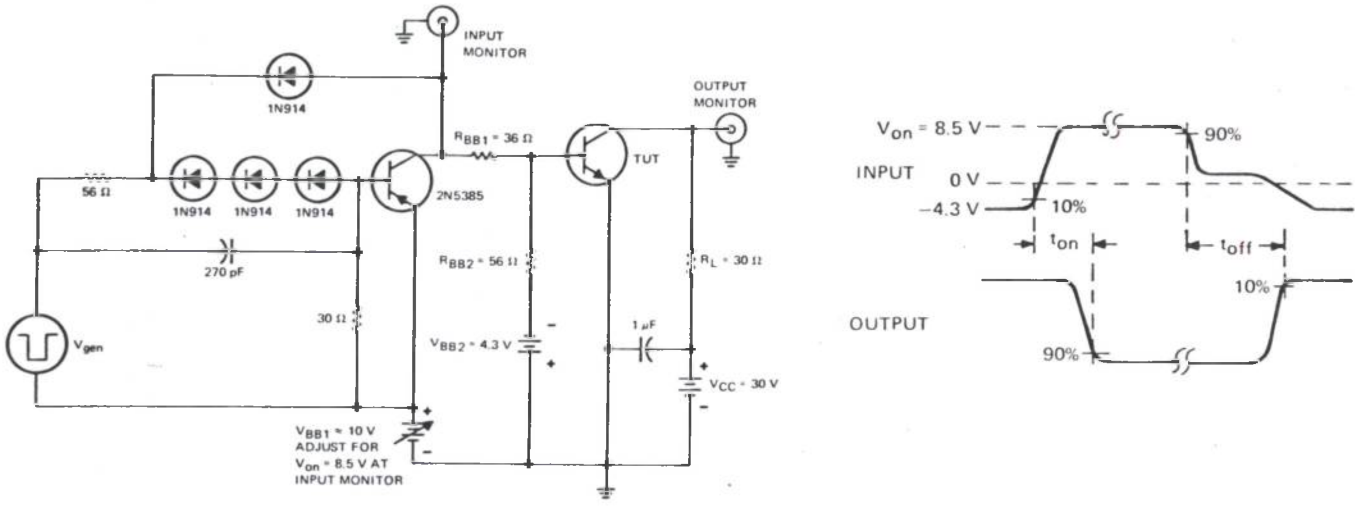
† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION



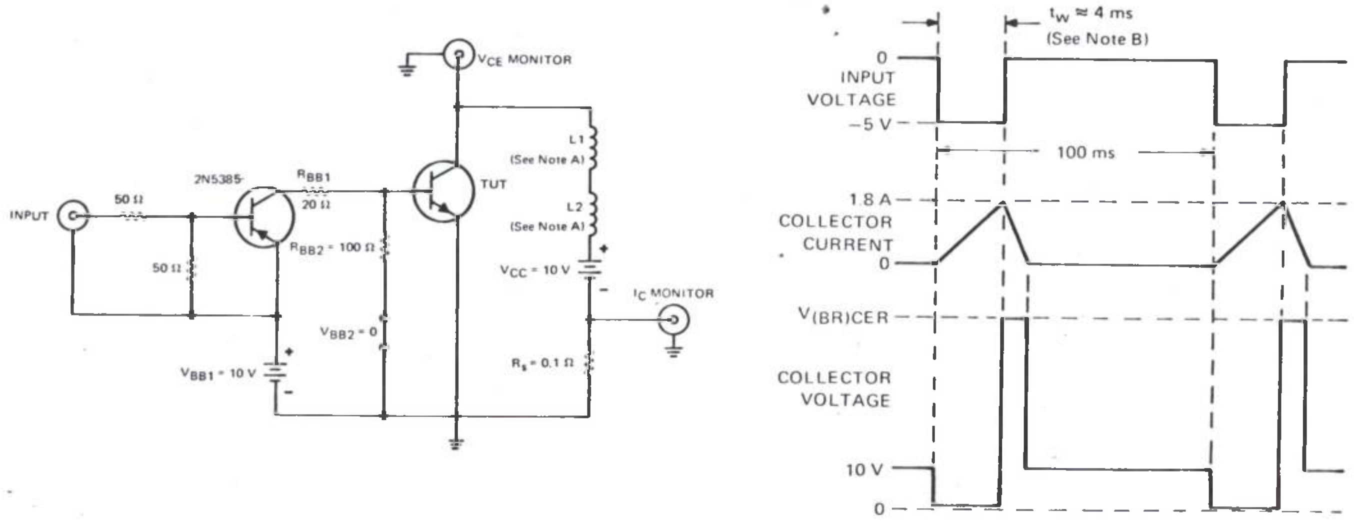
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES:
- A. V_{gen} is a −30-V pulse (from 0 V) into a 50-Ω termination.
- B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leqslant 15$ ns, $t_f \leqslant 15$ ns, $Z_{out} = 50\ \Omega$, $t_w = 20\ \mu s$, duty cycle ⩽ 2%.
- C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leqslant 15$ ns, $R_{in} \geqslant 10\ M\Omega$, $C_{in} \leqslant 11.5$ pF.
- D. Resistors must be noninductive types.
- E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTES:
- A. L1 and L2 are 10 mH, 0.11 Ω, Chicago Standard Transformer Corporation C-2688, or equivalent.
- B. Input pulse width is increased until I_{CM} = 1.8 A.

FIGURE 2

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

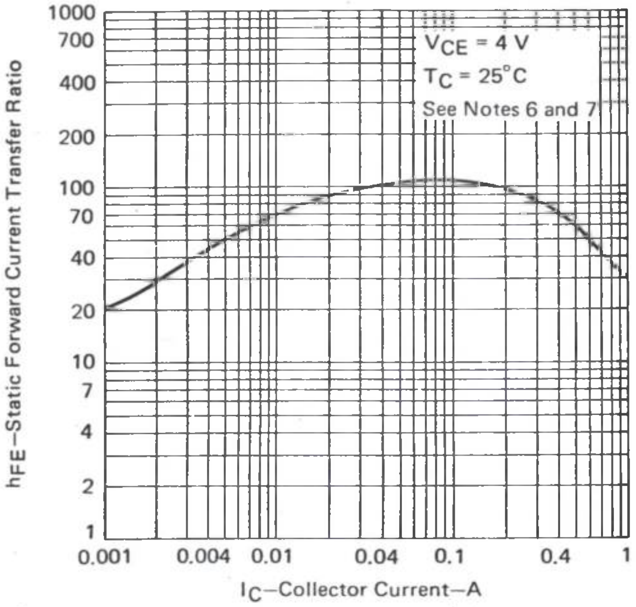


FIGURE 3

NOTES: 6. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

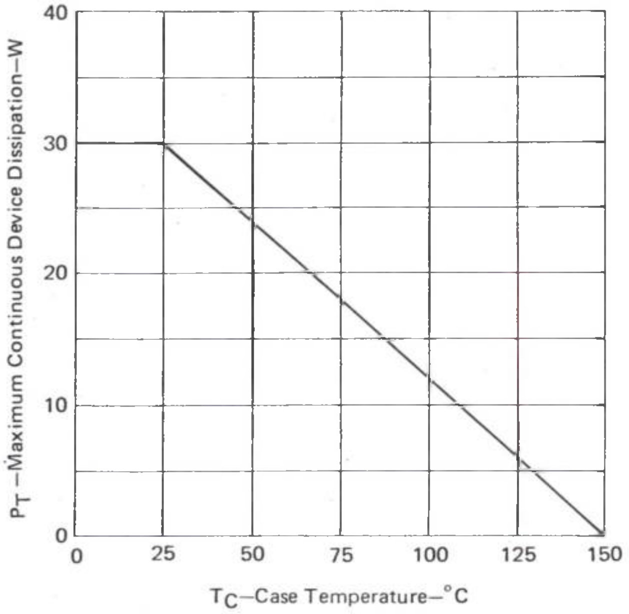


FIGURE 4

MAXIMUM SAFE OPERATING REGION

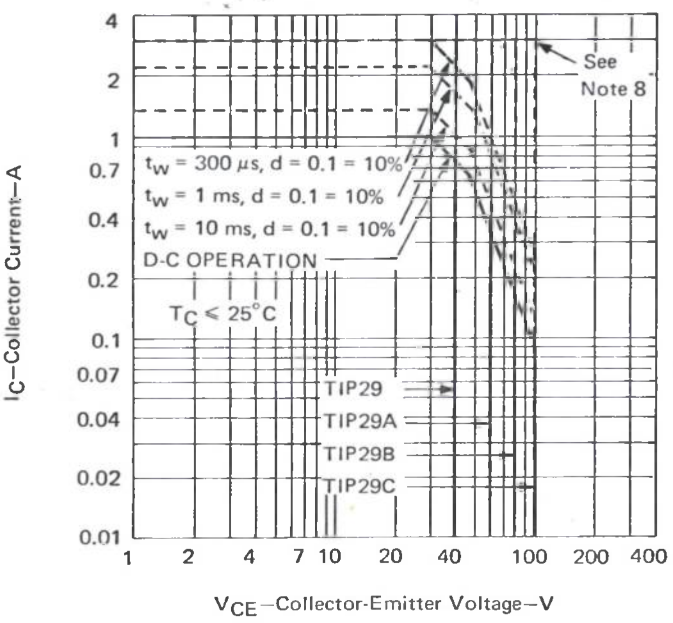


FIGURE 5

NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

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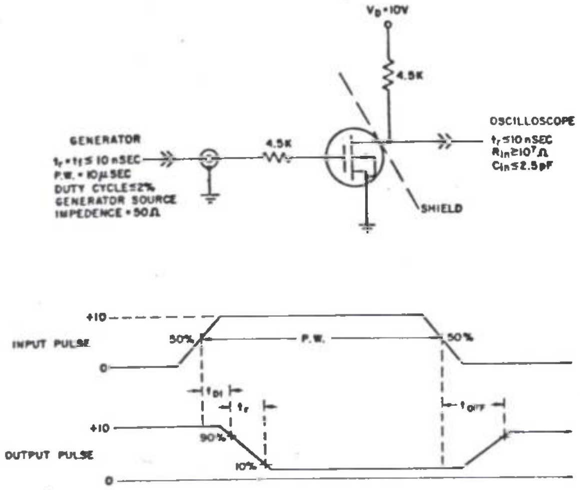
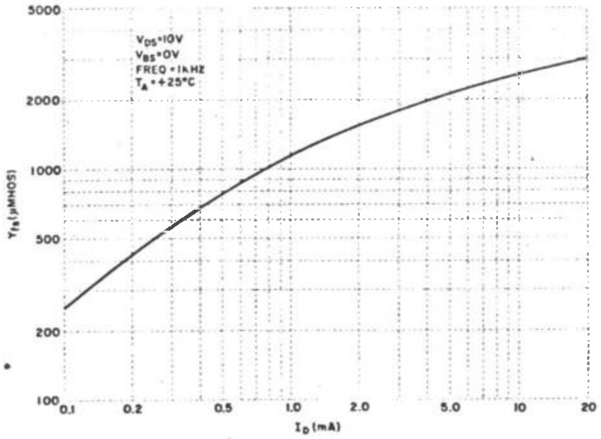
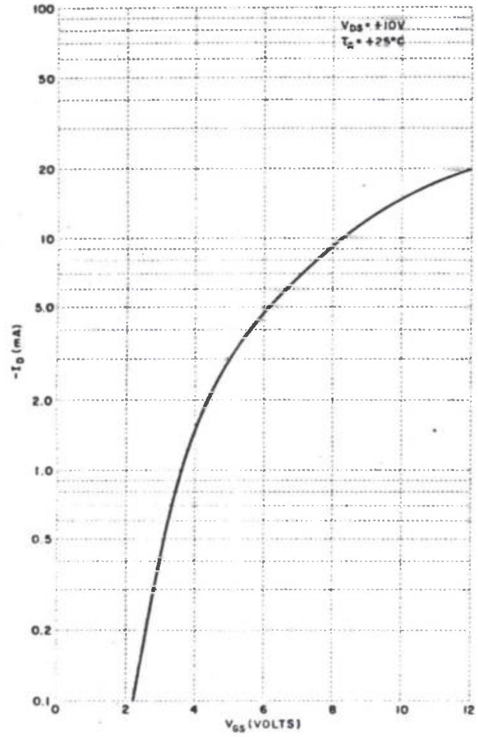
SWITCHING TEST SET MEM 562 C
FIGURE 1



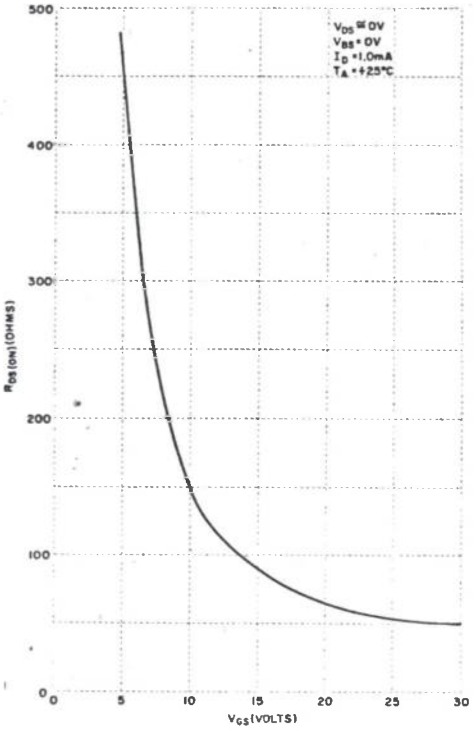
FORWARD TRANSADMITTANCE VS DRAIN CURRENT



DRAIN CURRENT VS GATE VOLTAGE TRANSFER CHARACTERISTICS



DRAIN TO SOURCE RESISTANCE VS GATE VOLTAGE



HANDLING PRECAUTIONS

The MEM 562 C insulated gate field effect transistors have very high gate resistance, (10^{15} ohm typical). This resistance, combined with the gate capacitance, requires that every precaution be taken during testing and handling in order to prevent charge build up and possible gate breakdown.

The shorting of the gate lead to the other leads during handling will protect the gate from breakdown.

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MPS-U55
MPS-U56

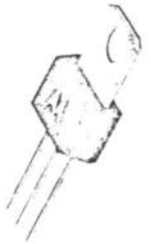
PNP SILICON ANNULAR* AMPLIFIER TRANSISTORS

MAY 1969 – DS 5327

PNP SILICON ANNULAR* AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 60 Vdc (Min) @ I_C = 1.0 mAdc – MPS-U55
  80 Vdc (Min) @ I_C = 1.0 mAdc – MPS-U56
- High Power Dissipation – P_D = 5.0 W @ T_C = 25°C
- Complements to MPS-U05 and MPS-U06



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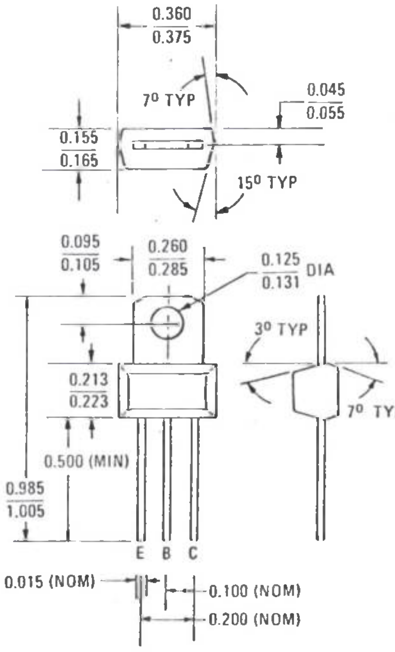
MAXIMUM RATINGS

Rating	Symbol	MPS-U55	MPS-U56	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current – Continuous	I_C	1.0		Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 9.10		Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 45.4		Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +135		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	22	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	110	°C/W



Collector connected to tab

CASE 152

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*Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0) MPS-U05 MPS-U06	BV_{CEO}	 60 80	 – –	 – –	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) MPS-U05 (V_{CB} = 60 Vdc, I_E = 0) MPS-U06	I_{CBO}	 – –	 – –	 100 100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc) (I_C = 250 mAdc, V_{CE} = 1.0 Vdc) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc) (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	 100 – 50 –	 180 125 170 100	 – – – –	–
Collector-Emitter Saturation Voltage (I_C = 250 mAdc, I_B = 10 mAdc) (I_C = 250 mAdc, I_B = 25 mAdc)	$V_{CE(sat)}$	 – –	 0.25 0.1	 0.6 –	Vdc
Base-Emitter Saturation Voltage (I_C = 250 mAdc, I_B = 25 mAdc)	$V_{BE(sat)}$	–	0.83	–	Vdc
Base-Emitter On Voltage (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	0.75	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	50	150	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	6.0	12	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{ib}	–	14	–	pF

FIGURE 1 – TYPICAL DC CURRENT GAIN

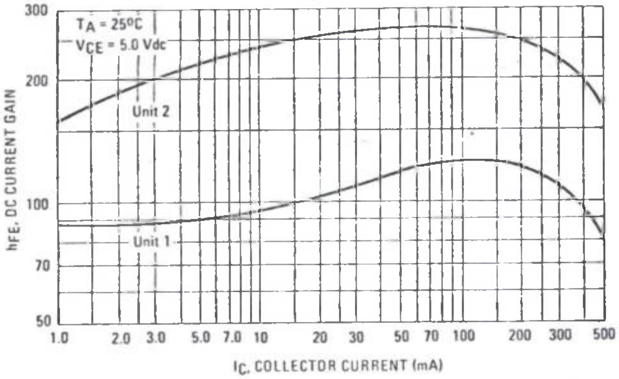


FIGURE 2 – "SATURATION" AND "ON" VOLTAGES

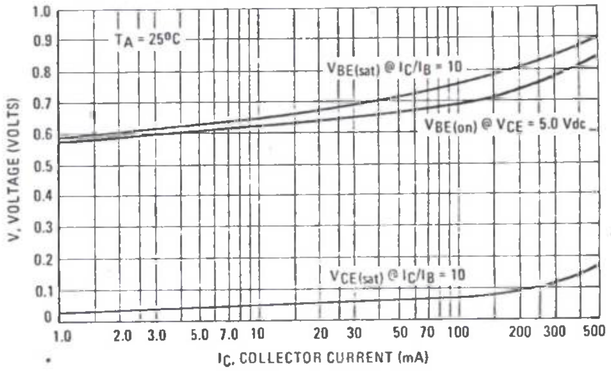
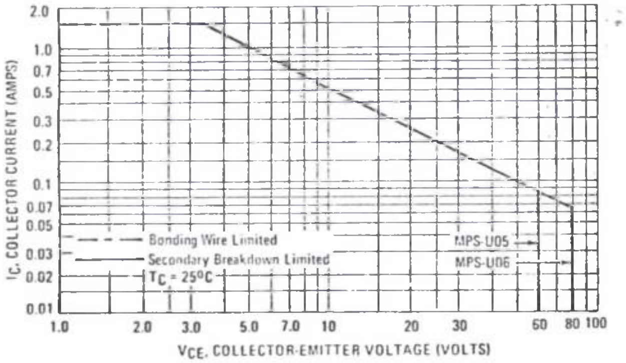


FIGURE 3 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 135°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MPS-U05
MPS-U06

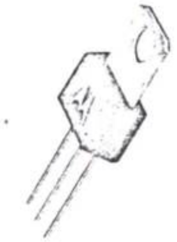
NPN SILICON ANNULAR* AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 60 Vdc (Min) @ I_C = 1.0 mAdc — MPS-U05
  80 Vdc (Min) @ I_C = 1.0 mAdc — MPS-U06
- High Power Dissipation — P_D = 5.0 W @ T_C = 25°C
- Complements to MPS-U55 and MPS-U56

NPN SILICON AMPLIFIER TRANSISTORS

MAY 1969 – DS 5326



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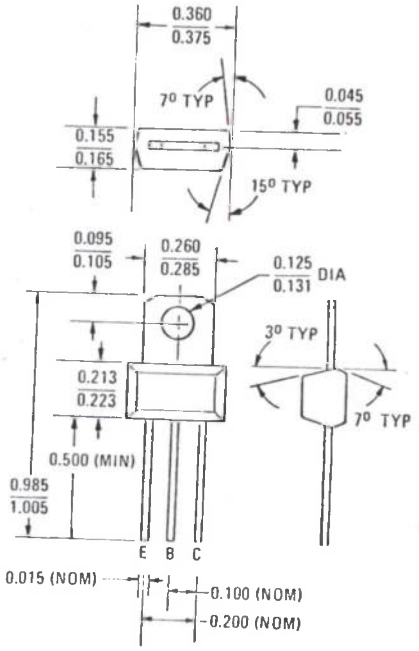
1400 West 46th Ave./DENVER, COLORADO 80216
PHONE: (303) 433-8551/TWX: 910-931-0580
EFFECTIVE APRIL 1st, 1969

AXIMUM RATINGS

Rating	Symbol	MPS-U05	MPS-U06	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current — Continuous	I_C	1.0		Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 9.10		Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 45.4		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +135		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	22	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	110	°C/W



Collector connected
to tab

CASE 152

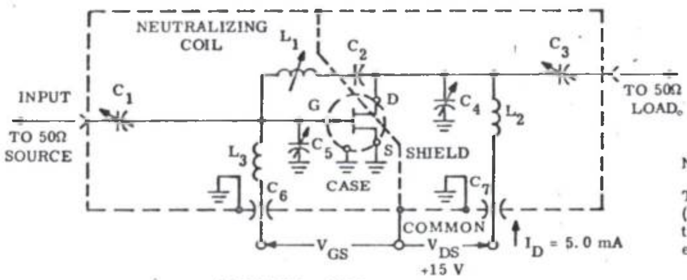
*Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (continued)

SMALL-SIGNAL CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
Forward Transadmittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5484 2N5485 2N5486	$\|y_{fs}\|$	3000 3500 4000	- - -	6000 7000 8000	µmhos
Forward Transconductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5484 2N5485 2N5486	$Re(y_{fs})$	2500 3000 3500	- - -	- - -	µmhos
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5484 2N5485 2N5486	$\|y_{os}\|$	- - -	- - -	50 60 75	µmhos
Output Conductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5484 2N5485, 2N5486	$Re(y_{os})$	- -	- -	75 100	µmhos
Input Conductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5484 2N5485, 2N5486	$Re(y_{is})$	- -	- -	100 1000	µmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	-	-	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	-	-	1.0	pF
Output Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{oss}	-	-	2.0	pF
Common-Source Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1.0 Megohm, f = 1.0 kHz) (V_{DS} = 15 Vdc, I_D = 1.0 mAdc, $R_G \approx$ 1.0 k ohm, f = 100 MHz) (V_{DS} = 15 Vdc, I_D = 1.0 mAdc, $R_G \approx$ 1.0 k ohm, f = 200 MHz) (V_{DS} = 15 Vdc, I_D = 4.0 mAdc, $R_G \approx$ 1.0 k ohm, f = 100 MHz) (V_{DS} = 15 Vdc, I_D = 4.0 mAdc, $R_G \approx$ 1.0 k ohm, f = 400 MHz)	All Types 2N5484 2N5484 2N5485, 2N5486 2N5485, 2N5486	NF	- - - - -	- - 4.0 - -	2.5 3.0 - 2.0 4.0	dB
Insertion Power Gain (V_{DS} = 15 Vdc, I_D = 1.0 mAdc, f = 100 MHz) (V_{DS} = 15 Vdc, I_D = 1.0 mAdc, f = 200 MHz) (V_{DS} = 15 Vdc, I_D = 4.0 mAdc, f = 100 MHz) (V_{DS} = 15 Vdc, I_D = 4.0 mAdc, f = 400 MHz)	2N5484 2N5484 2N5485, 2N5486 2N5485, 2N5486	G_{ps}	16 - 18 10	- 14 - -	25 - 30 20	dB

FIGURE 1 - 100 MHz & 400 MHz NEUTRALIZED AMPLIFIER



ADJUST V_{GS} FOR
I_D = 5.0 mA
V_{GS} < 0 VOLTS

NOTE:

The noise source is a hot-cold body (AIL type 70 or equivalent) with a test receiver (AIL type 136 or equivalent).

Reference Designation	VALUE	
	100 MHz	400 MHz
C_1	1-12 pF	0.8-8.0 pF
C_2	1000 pF	27 pF
C_3	1-12 pF	0.8-8.0 pF
C_4	1-12 pF	0.8-8.0 pF
C_5	1-12 pF	0.8-8.0 pF
C_6	0.0015 µF	0.001 µF
C_7	0.0015 µF	0.001 µF
L_1	3.0 µH*	0.2 µH**
L_2	0.25 µH*	0.03 µH**
L_3	0.14 µH*	0.022 µH**

* L_1 17 turns (approximately - depending upon circuit layout), AWG #28 enameled copper wire, close wound on 9/32" ceramic coil form. Tuning provided by a powdered iron slug.

L_2 4 1/2 turns, AWG #18 enameled copper wire, 5/16" long, 3/8" I. D. (AIR CORE).

L_3 3 1/2 turns, AWG #18 enameled copper wire, 1/4" long, 3/8" I. D. (AIR CORE).

** L_1 6 turns (approximately - depending upon circuit layout), AWG #24 enameled copper wire, close wound on 7/32" ceramic coil form. Tuning provided by an aluminum slug.

L_2 1 turn, AWG #16 enameled copper wire, 3/8" I. D. (AIR CORE).

L_3 1/2 turn, AWG #16 enameled copper wire, 1/4" I. D. (AIR CORE).

2N5139

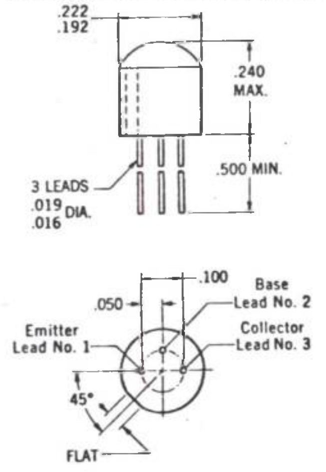
PNP HIGH-SPEED SWITCH AND RF AMPLIFIER

DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTOR

- HIGH BETA . . . . $h_{FE} = 150$ (TYP) AT 10 mA
- HIGH FREQUENCY . . . $f_T = 500$ MHz (TYP) AT 10 mA
- LOW CAPACITANCE . . . $C_{cb} = 2.2$ pF (TYP)
- HIGH VOLTAGE . . . . . $LV_{CEO} = 20$ VOLTS (MIN)

PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-106) outline



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram Package
is electrically non-conductive material

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures		
Storage Temperature		−55°C to +125°C
Operating Junction Temperature		+125°C Maximum
Lead Temperature (Soldering, 10 second time limit)		+260°C Maximum
Maximum Power Dissipation (Notes 2 and 3)		
Total Dissipation at 25°C Case Temperature		0.5 Watt
at 25°C Ambient Temperature		0.2 Watt
Maximum Voltages and Current		
V_{CBO}	Collector to Base Voltage	−20 Volts
V_{CEO}	Collector to Emitter Voltage (Note 4)	−20 Volts
V_{EBO}	Emitter to Base Voltage	−5.0 Volts
I_C	Collector Current	100 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
h_{FE}	DC Current Gain	30	70			$I_C = 100\ \mu A$	$V_{CE} = -10$ V
h_{FE}	DC Current Gain	40	100			$I_C = 1.0$ mA	$V_{CE} = -10$ V
h_{FE}	DC Pulse Current Gain (Note 5)	40	150			$I_C = 10$ mA	$V_{CE} = -1.0$ V
h_{FE}	DC Pulse Current Gain (Note 5)	15	30			$I_C = 50$ mA	$V_{CE} = -10$ V
V_{CE}(sat)	Collector Saturation Voltage			−0.15	Volts	$I_C = 1.0$ mA	$I_B = 0.1$ mA
V_{CE}(sat)	Pulsed Collector Saturation Voltage (Note 5)			−0.20	Volts	$I_C = 10$ mA	$I_B = 1.0$ mA
V_{CE}(sat)	Pulsed Collector Saturation Voltage (Note 5)		−0.2	−0.5	Volts	$I_C = 50$ mA	$I_B = 5.0$ mA
V_{BE}(sat)	Pulsed Base Saturation Voltage (Note 5)	−0.7	−0.77	−1.0	Volts	$I_C = 10$ mA	$I_B = 1.0$ mA
V_{BE}(sat)	Pulsed Base Saturation Voltage (Note 5)		−0.75	−1.25	Volts	$I_C = 50$ mA	$I_B = 5.0$ mA
t_{on}	Turn On Time (Note 6)			50	ns	$I_C \approx 50$ mA	$I_{B1} \approx 5.0$ mA
t_{off}	Turn Off Time (Note 6)			200	ns	$I_C \approx 50$ mA	$I_{B1} \approx 5.0$ mA $I_{B2} \approx -5.0$ mA
h_{fe}	High Frequency Current Gain (f = 100 MHz)	3.0	5.0			$I_C = 10$ mA	$V_{CE} = -20$ V

Additional Electrical Characteristics on page 2

*Planar is a patented Fairchild process.

NOTES:

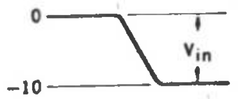
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
(3) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C); junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).
(4) Rating refers to a high-current point where collector to emitter voltage is lowest. For more information send for Fairchild Publication APP-4/2.
(5) Pulse Conditions: length = 300 μs; duty cycle = 1%.
(6) See switching circuit for exact values of I_C, I_{B1}, and I_{B2}.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

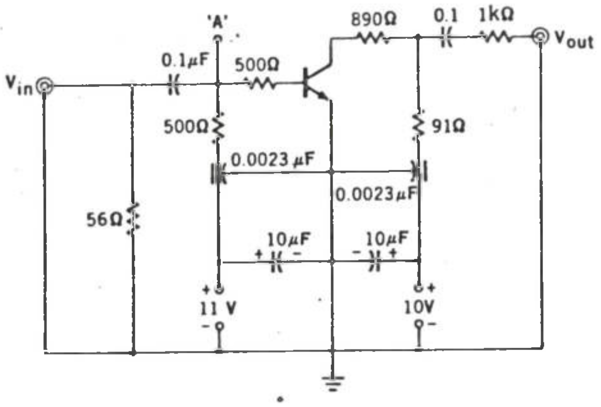
NOTES:

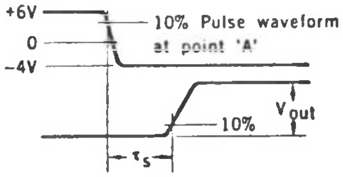
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low-duty cycle operations.
(3) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C); junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).
(4) This rating refers to a high-current point where collector to emitter voltage is lowest.
(5) Pulse Conditions: length = 300 μs; duty cycle = 1%.
(6) $R_S = 10$ kΩ, Power Bandwidth of 150 Hz.
(7) $R_S = 10$ kΩ, Power Bandwidth of 15.7 kHz with 3.0 dB points at 10 Hz and 10 kHz.
(8) $R_S = 1.0$ kΩ, Power Bandwidth of 150 Hz.

CHARGE STORAGE TIME MEASUREMENT CIRCUIT



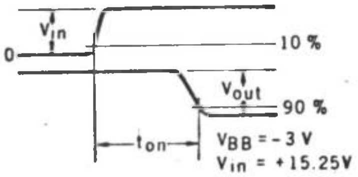
Pulse Generator
V_{in} Rise Time < 1 ns
Source Impedance = 50Ω
PW ≥ 300 ns
Duty Cycle < 2 %



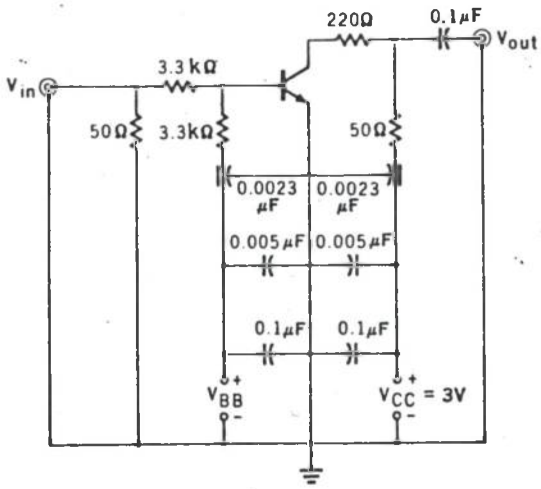


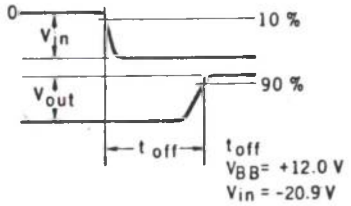
To Sampling Oscilloscope
Input Impedance = 50Ω
Rise Time ≤ 1 ns

t_{ON} — t_{OFF} MEASUREMENT CIRCUIT



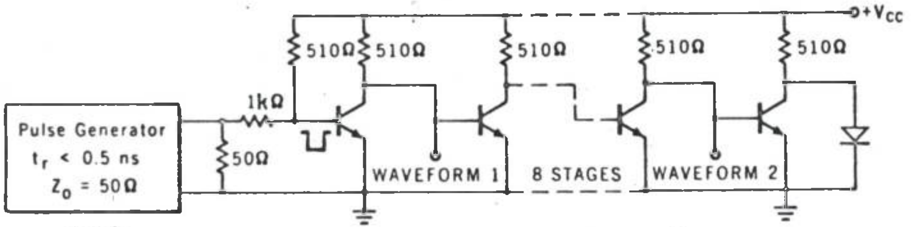
Pulse Generator
V_{in} Rise Time < 1 ns
Source Impedance = 50Ω
PW ≥ 300 ns
Duty Cycle < 2 %

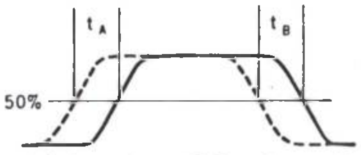




To Sampling Oscilloscope
Input Impedance = 50Ω
Rise Time ≤ 1 ns

CIRCUIT FOR MEASUREMENT OF PROPAGATION DELAY





Waveforms 1 and 2 Superimposed

$$\bar{t}pd = \frac{t_A + t_B}{20}$$

$\bar{t}pd$ = Average Propagation per Transistor

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C). Junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).

(4) Rating refers to a high-current point where collector to emitter voltage is lowest.

(5) Pulse Conditions: length = 300 μs; duty cycle = 1%.

(6) See switching circuits for exact value of I_C, I_{B1}, and I_{B2}.

2N5134

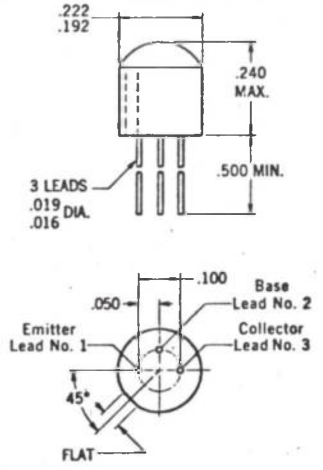
NPN HIGH-SPEED SATURATED SWITCH

DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTOR

- **HIGH FREQUENCY CURRENT GAIN . . . $f_T = 400$ MHz (MIN)**
- **LOW CAPACITANCE . . . . $C_{cb} = 4$ pF (MAX)**
- **LOW CHARGE STORAGE TIME . . . . . . $\tau_S = 18$ ns (MAX)**
- **LOW V_{CE}(sat) . . . . 0.2 VOLT (MAX) AT 10 mA**

PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-106) outline



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram. Package
is electrically non-conductive material

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures		
Storage Temperature		−55°C to +125°C
Operating Junction Temperature		125°C Maximum
Lead Temperature (Soldering, 10 second time limit)		260°C Maximum
Maximum Power Dissipation		
Total Dissipation at 25°C Case Temperature (Notes 2 and 3)		0.5 Watt
at 25°C Ambient Temperature		0.2 Watt
Maximum Voltages and Current		
V_{CBO}	Collector to Base Voltage	20 Volts
V_{CES}	Collector to Emitter Voltage	20 Volts
V_{CEO}	Collector to Emitter Voltage	10 Volts
V_{EBO}	Emitter to Base Voltage	3.5 Volts
I_C	Collector Current (10 μs Pulse)	500 mA
I_C	DC Collector Current	100 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
h_{FE}	DC Pulse Current Gain (Note 5)	20	66	150		$I_C = 10$ mA	$V_{CE} = 1.0$ V
h_{FE}	DC Pulse Current Gain (Note 5)	15	71			$I_C = 30$ mA	$V_{CE} = 0.4$ V
h_{FE}	DC Pulse Current Gain (Note 5)		40			$I_C = 100$ mA	$V_{CE} = 1.0$ V
V_{BE}(sat)	Base Saturation Voltage	0.70	0.80	0.90	Volts	$I_C = 10$ mA	$I_B = 1.0$ mA
V_{BE}(sat)	Base Saturation Voltage	0.72	0.85	1.10	Volts	$I_C = 10$ mA	$I_B = 3.3$ mA
V_{BE}(sat)	Base Saturation Voltage		0.90		Volts	$I_C = 30$ mA	$I_B = 3.0$ mA
V_{BE}(sat)	Base Saturation Voltage		1.10		Volts	$I_C = 100$ mA	$I_B = 10$ mA
V_{CE}(sat)	Collector Saturation Voltage		0.14	0.25	Volts	$I_C = 10$ mA	$I_B = 1.0$ mA
V_{CE}(sat)	Collector Saturation Voltage		0.12	0.20	Volts	$I_C = 10$ mA	$I_B = 3.3$ mA
V_{CE}(sat)	Collector Saturation Voltage		0.17		Volts	$I_C = 30$ mA	$I_B = 3.0$ mA
V_{CE}(sat) (+65°C)	Collector Saturation Voltage		0.19		Volts	$I_C = 10$ mA	$I_B = 1.0$ mA
V_{CE}(sat)	Collector Saturation Voltage		0.28		Volts	$I_C = 100$ mA	$I_B = 10$ mA
h_{fe}	High Frequency Current Gain (f = 100 MHz)	2.5	5.75			$I_C = 10$ mA	$V_{CE} = 10$ V
C_{cb}	Collector-Base Capacitance		2.3	4.0	pF	$I_E = 0$	$V_{CB} = 5.0$ V
I_{CES}	Collector Reverse Current		0.05	0.40	μA	$V_{CE} = 15$ V	$V_{BE} = 0$
I_{CBO}(65°C)	Collector Cutoff Current		1.0	10	μA	$I_E = 0$	$V_{CB} = 15$ V
BV_{CES}	Collector to Emitter Breakdown Voltage	20			Volts	$I_C = 10\ \mu$A	$V_{BE} = 0$
BV_{CBO}	Collector to Base Breakdown Voltage	20			Volts	$I_C = 10\ \mu$A	$I_E = 0$
V_{CEO}(sust)	Collector to Emitter Sustaining Voltage (Notes 4 and 5)	10			Volts	$I_C = 10$ mA (pulsed)	$I_B = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	3.5			Volts	$I_C = 0$	$I_E = 10\ \mu$A
τ_s	Charge Storage Time Constant (Note 6)		7.0	18	ns	$I_C = I_{B1} \approx 10$ mA, $I_{B2} \approx -10$ mA	
t_{on}	Turn On Time (Note 6)		8.0	18	ns	$I_C \approx 10$ mA, $I_{B1} \approx 3.3$ mA	
t_{off}	Turn Off Time (Note 6)		7.0	18	ns	$I_C \approx 10$ mA, $I_{B1} \approx 3.3$ mA, $I_{B2} \approx -3.3$ mA	

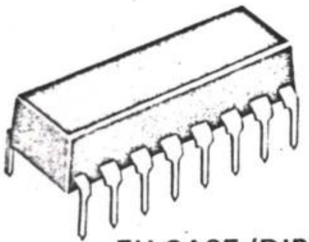
*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

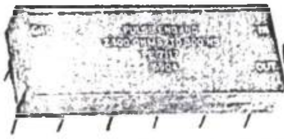
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

Pulse Engineering Inc.
P.O. Box 12235
San Diego, Calif 92112
(714) 279-5900

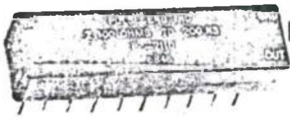
Delay Lines, Lumped Constant Series



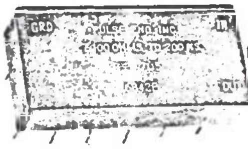
EH CASE (DIP)



DL4 CASE



DL2 CASE

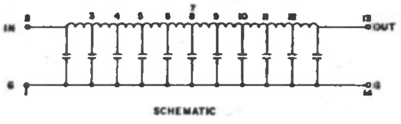


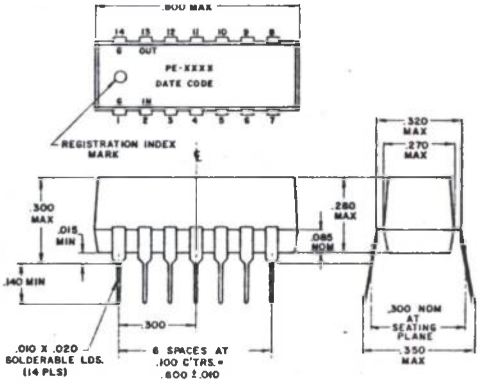
DL3 CASE

DL1 CASE

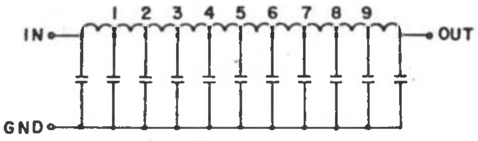
- **Fast Rise Time** – all delay lines feature fast rise time and low distortion.
- **10 Taps** - each delay line has 10 equally spaced taps.
- **Printed Circuit Board Mounting** – this series is designed for printed circuit board mounting. Both D-I-L and D-I-P packages available. (Both 14 & 16 lead).

EH CASE





DL CASE



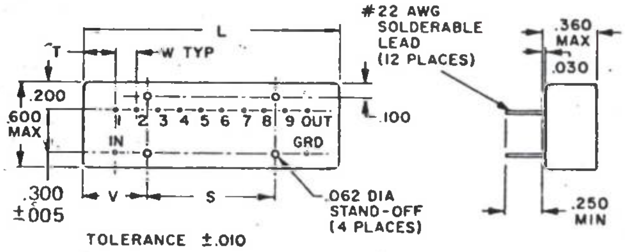


Fig. 1

		MAX.	NOM.	±.005	±.005	±.010
	CASE	L	S	T	W	V
Fig. 1	DL 1	1.800	.900	.225	.150	.450
	DL 2	2.200	1.200	.200	.200	.500
Fig. 2	DL 3	1.800	1.200	.150	.300	.300
	DL 4	2.200	1.600	.100	.400	.300

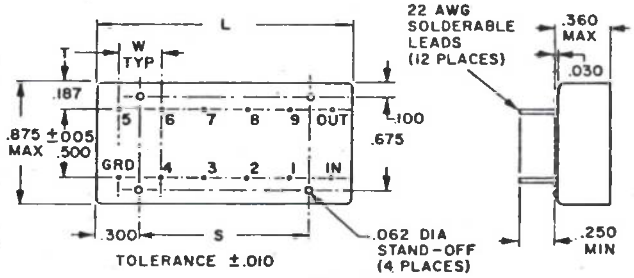


Fig. 2

These can be used to delay video or pulses

[illegible]

Catalog Number	Impedance Zo (ohms ±10%)	Total Delay (ns ±5%)	No. of Taps	Delay Per Tap (ns ±3 ns)	Rise Time (ns max.)	Total Delay Rise Time Ratio (min.)	Distortion (% max.)	Attenuation (% max.)	Case Style
7103	50	50	10	5(±2 ns)	8.5	6	10	1.6	DL1
7104	50	100	10	10	17	6	10	3.8	DL1
7105	50	125	10	12.5	21	6	10	6.5	DL1
9821	50	50	10	5(±2 ns)	8.5	6	10	1.6	EH
9822	50	100	10	10	17	6	10	3.8	EH
9823	50	125	10	12.5	21	6	10	6.5	EH
9824	100	50	10	5(±2 ns)	8.5	6	10	2.0	EH
9825	100	100	10	10	17	6	10	4.0	EH
9826	100	125	10	12.5	21	6	10	7.0	EH
9827	100	150	10	15	25	6	10	6.0	[illegible]
[illegible]	100	[illegible]	10	[illegible]	34	6	10	10.0	[illegible]
[illegible]	100	[illegible]	[illegible]	[illegible]	42	[illegible]	[illegible]	[illegible]	[illegible]
7106	100	50	10	5(±2 ns)	8.5	6	10	2.0	DL1
7107	100	100	10	10	17	6	10	4.0	DL1
7108	100	125	10	12.5	21	6	10	7.0	DL1
7109	100	150	10	15	25	6	10	6.0	DL2
7110	100	200	10	20	34	6	10	10.0	DL2
7111	100	250	10	25	42	6	10	12.0	DL2
7112	100	100	10	10	10	10	10	4.0	DL3
7113	100	125	10	12.5	12.5	10	10	6.5	DL3
7114	100	150	10	15	15	10	10	7.0	DL3
7115	100	200	10	20	20	10	10	8.0	DL3
7116	100	250	10	25	25	10	10	15.0	DL3
7117	100	300	10	30	30	10	10	12.0	DL4
Z 7118	100	400	10	40	40	10	10	20.0	DL4
7119	100	500	10	50	50	10	10	22.0	DL4

Rating Range

Total Delay	50 to 500 nsec
Delay Per Tap	5 to 50 nsec
Rise Time	8.5 to 50 nsec
Impedance	50 and 100 ohm
Distortion	10% maximum
Temperature Coefficient	Approximately 100 PPM/°C
Peak Pulse Voltage	100 volts

Prices

Quantities 1-9. Available from stock.

DL1 case style	$20.00 each
DL2 case style	$20.00 each
DL3 case style	$30.00 each
DL4 case style	$30.00 each
EH case style	$24.00 each

[illegible]

This series of Lumped Constant Delay Lines offers maximum reliability in a high density package. Designed for computer applications, these units are fully encapsulated in epoxy resin. The units in the GH case are transfer molded and suitable for automatic machine insertion.

All units feature 10 equally spaced taps, fast rise time, and printed circuit board mounting.

Generally, a delay line is used to control the timing between two signals by delaying one with respect to the other. A delay line can be defined as a low pass filter which, up to a given frequency (the cut-off frequency), has a constant attenuation and a linear phase shift. When these conditions are met, a signal, such as a pulse, passing through the delay line will arrive at the load after the specified delay time interval. When the pulse rise time is compatible with the design cut-off frequency and the delay line is matched on both ends with the proper impedance, the pulse will arrive with minimum attenuation and distortion.

[illegible]

Distributed delay lines can be designed for impedances of 50 ohms to 1000 ohms and with or without TAPS. The Delay to Rise Time Ratio varies from approximately 1.5 to 4 depending on requirements of the application. The lower the ratio the lower the cost.

They are available in EH Case (DIP) and in other packages as need dictates. Distributed lines are custom designed and are manufactured in Pulse Engineering's new Mexico delay line facility. If you have volume requirements, Pulse can offer you significant savings. Contact any office listed on the back cover of this catalog.

FM 3958
Dual FET

[illegible] 3676
'75
National
Semicomp

NOVEMBER 1968

LM 304 negative regulator

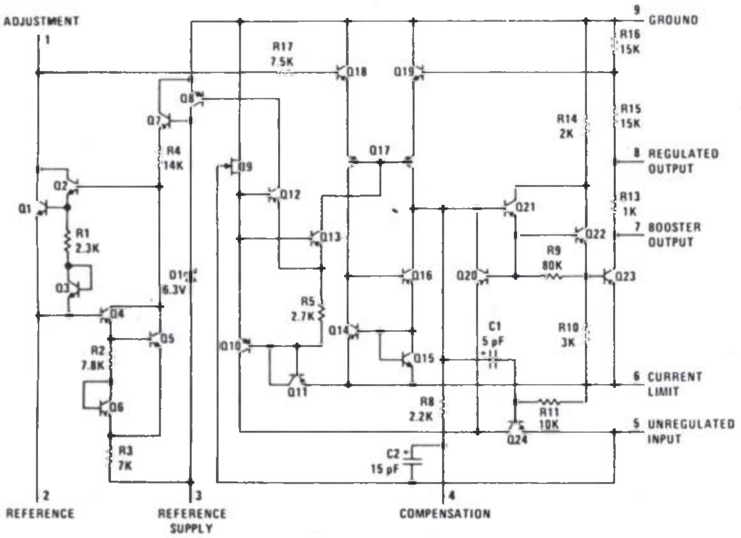
general description

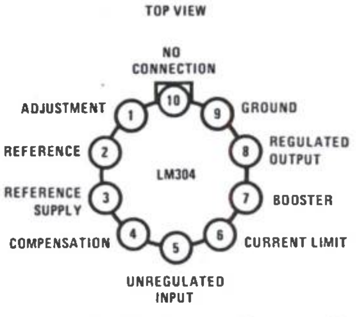
The LM304 is a precision voltage regulator which can be programmed by a single external resistor to supply any voltage from 30V down to zero while operating from a single unregulated supply. It can also provide 0.01-percent regulation in circuits using a separate, floating bias supply, where the output voltage is limited only by the breakdown of external pass transistors. Although designed primarily as a linear, series regulator, the circuit can be used as a switching regulator, a current regulator or in a number of other control applications. Typical performance characteristics are:

- 1 mV regulation no load to full load
- 0.01%/V line regulation
- 0.2 mV/V ripple rejection

The LM304 is a complement of the LM300 and LM305 positive regulators, intended for systems requiring regulated negative voltages which have a common ground with the unregulated supply. By itself, it can deliver output currents to 25 mA, but external transistors can be added to get any desired current. The output voltage is set by external resistors, and either constant or foldback current limiting is made available. The LM304 is a commercial/industrial version of the LM104 and LM204.

schematic and connection diagrams

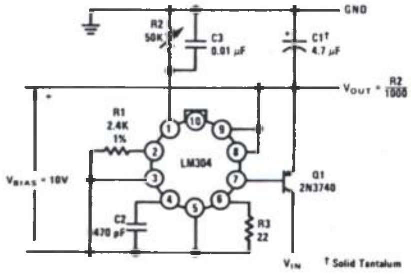




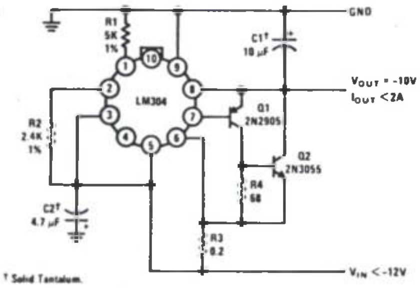
Note: Pin 5 Connected to Case

typical applications

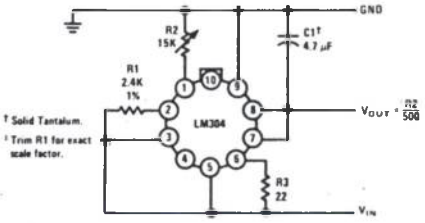
Operating with Separate Bias Supply



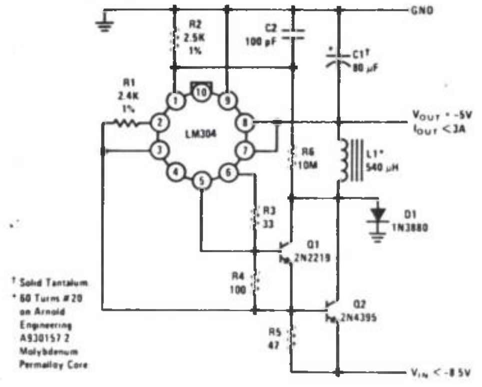
High Current Regulator



Basic Regulator Circuit



Switching Regulator



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absolute maximum ratings

Input Voltage	40V
Input-Output Voltage Differential	40V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 60 sec)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		–40		–8	V
Output Voltage Range		–30		–0.035	V
Output-Input Voltage Differential (Note 3)	$I_O = 20$ mA	2.0		40	V
	$I_O = 5$ mA	0.5		40	V
Load Regulation (Note 4)	$0 \leq I_O \leq 20$ mA				
	$R_{SC} = 15\Omega$		1	5	mV
Line Regulation (Note 5)	$V_{OUT} \leq -5V$				
	$\Delta V_{IN} = 0.1\ V_{IN}$		0.056	0.1	%
Ripple Rejection	$C_{19} = 10\ \mu F$, f = 120 Hz				
	$V_{IN} < -15V$		0.2	0.5	mV/V
	$-7V \geq V_{IN} \geq -15V$		0.5	1.0	mV/V
Output Voltage Scale Factor	$R_{23} = 2.4K$	1.8	2.0	2.2	V/KΩ
Temperature Stability	$V_O \leq -1V, 0°C \leq T_A \leq 70°C$		0.3	1.0	%
Output Noise Voltage	$10\ Hz \leq f \leq 10\ KHz$				
	$V_O \leq -5V, C_{19} = 0$		0.001		%
	$C_{19} = 10\ \mu F$		5		µV
Standby Current Drain	$I_L = 5$ mA, $V_O = 0$		1.7	2.5	mA
	$V_O = -30V$		3.6	5.0	mA
Long Term Stability	$V_O \leq -1V$		0.1	1.0	%

Note 1: For operating at elevated temperatures, the device must be derated based on an 85°C maximum junction temperature and a thermal resistance of 45°C/W junction to case or 150°C/W junction to ambient. Peak dissipations to 1.0W are allowable providing the dissipation rating is not exceeded with the power averaged over a two second interval.

Note 2: These specifications apply for junction temperatures between 0°C and 85°C and for input and output voltages within the ranges given, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

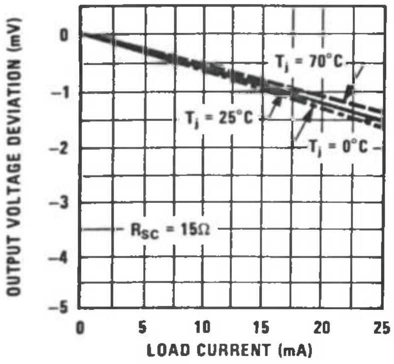
Note 3: When external booster transistors are used, the minimum output-input voltage differential is increased, in the worst case, by approximately 1V.

Note 4: The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

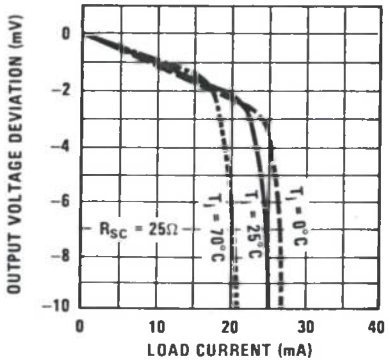
Note 5: With zero output, the dc line regulation is determined from the ripple rejection. Hence, with output voltages between 0V and –5V, a dc output variation, determined from the ripple rejection, must be added to find the worst-case line regulation.

typical performance characteristics

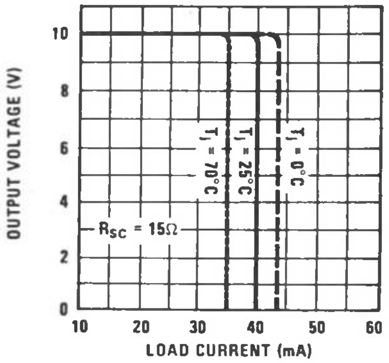
Load Regulation



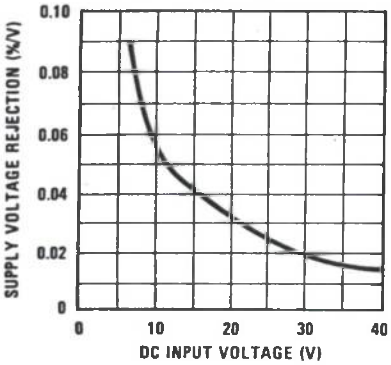
Load Regulation



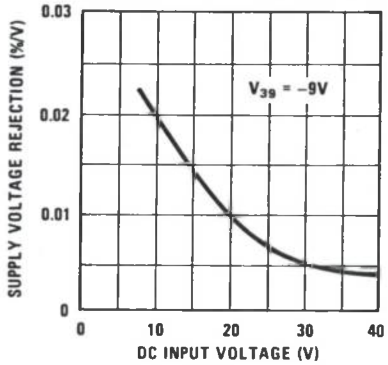
Current Limiting



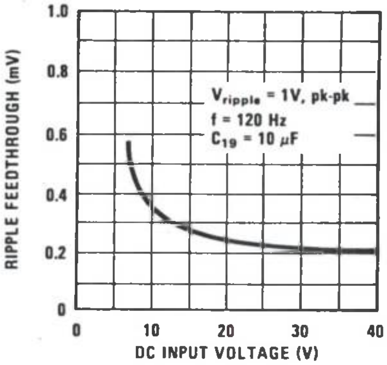
Supply Voltage Rejection



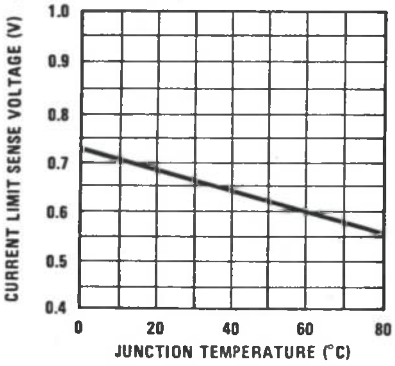
Supply Voltage Rejection With Preregulated Reference Supply



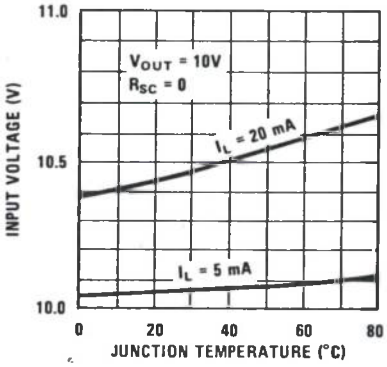
Ripple Rejection



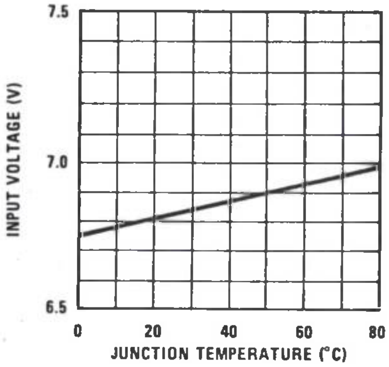
Current Limit Sense Voltage



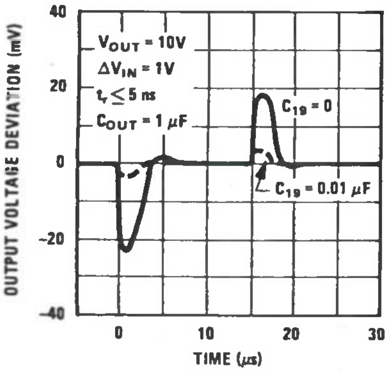
Regulator Dropout Voltage



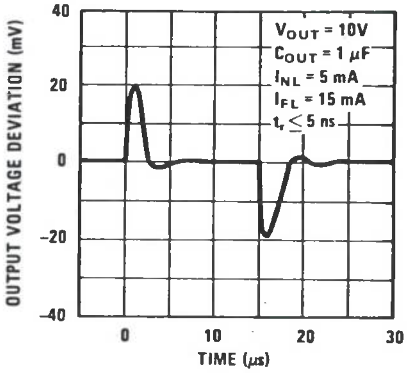
Minimum Input Voltage



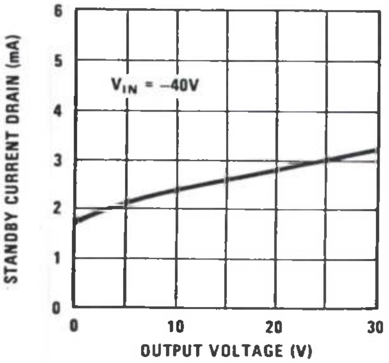
Line Transient Response



Load Transient Response



Standby Current Drain



definition of terms

Input Voltage Range: The range of dc input voltages on the unregulated input and the reference supply over which the regulator will operate within specifications.

Output Voltage Range: The range of regulated output voltages over which the specifications apply.

Output-Input Voltage Differential: The difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate within specifications.

Line Regulation: The change in regulated output voltage for a change in voltage on the unregulated input and reference supply terminals.

Ripple Rejection: The line regulation for ac input signals at or above a given frequency with a specified value of bypass capacitor on the adjustment terminal.

Load Regulation: The change in regulated output voltage for a change in load from zero to the maximum load current specified.

Current-Limit Sense Voltage: The voltage across the current limit terminals required to cause the regulator to go into current limiting. This voltage is used to determine the value of the external current limit resistor when external booster transistors are used.

Temperature Stability: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

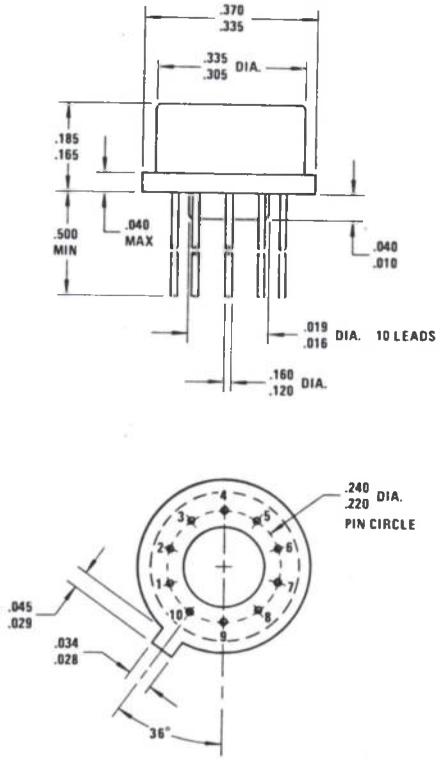
Output Voltage Scale Factor: The output voltage obtained for a unit value of resistance between the adjustment terminal and ground.

Output Noise Voltage: The average ac voltage at the output with constant load and no input ripple.

Standby Current Drain: That part of the operating current of the regulator which does not contribute to the load current.

Long Term Stability: Output voltage stability under accelerated life-test conditions at 125°C with maximum rated voltages and power dissipation for 1000 hours.

physical dimensions



Order Number LM304H

National Semiconductor Corporation
2975 San Ysidro Way, Santa Clara, California 95051
(408) 245-4320/TWX (910) 339-9240

Composition Fixed Resistors
Explanation of Part Numbers

B5000B

December 1965

All Allen-Bradley composition fixed resistors are identified by a part number which will provide information as to the type of resistor, resistance value and tolerance. The information below shows how these part numbers can be interpreted.

None of the Allen-Bradley composition fixed resistors have the part number put directly on the resistor. The part number is merely for identification on drawings, specifications, ordering and other places where it is convenient to use a part number to describe a particular resistor.

The only thing that appears on the resistor itself, in the way of identification is the standard EIA color coding. For your convenience, we are also giving you on this sheet a break down of this color coding.

GB1035

Type of Resistor Wattage Rating

Resistor Type	Wattage
BB	⅛ Watt
CB	¼ Watt
EB	½ Watt
GB	1 Watt
HB	2 Watt
GM	3 Watt
HM	4 Watt
TS	⅛ Watt
CS	¼ Watt
ES	½ Watt

Resistance Value

First two digits are significant figure.

Third digit or letter is the multiplier as follows:

Digit or Letter	Multiplier	Number of zeros to add
0	1	None
1	10	1
2	100	2
3	1,000	3
4	10,000	4
5	100,000	5
6	1,000,000	6
7	10,000,000	7
G	0.1	None

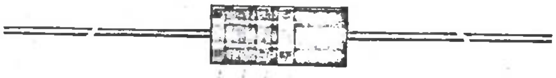
Tolerance

5 — ± 5%
1 — ±10%
2 — ±20%
4 — ± 2%

Examples:—

1000 Ohms — 102
1200 Ohms — 122
100 Ohms — 101
2.7 Ohms — 27G
10 Megohms — 106

Color Code



First Band — 1st Digit

Second Band — 2nd Digit

Third Band — Number of Zeroes or Decimal Multiplier

Fourth Band — Tolerance

Color	Digit	Multiplier
Black	0	1
Brown	1	10
Red	2	100
Orange	3	1000
Yellow	4	10,000
Green	5	100,000
Blue	6	1,000,000
Violet	7	10,000,000
Gray	8	100,000,000
White	9	1,000,000,000

Color	Digit	Multiplier
Red (Fourth Band)	± 2% Tolerance	
Gold	± 5% Tolerance	0.1
Silver	± 10% Tolerance	0.01
No Color	± 20% Tolerance	

Preferred Number Series

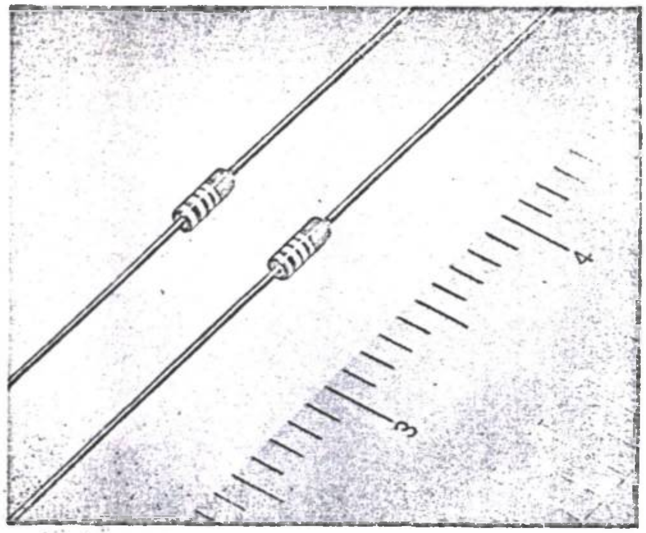
±5% Tolerance	10	15	22	33	47	68
	11	16	24	36	51	75
	12	18	27	39	56	82
	13	20	30	43	62	91
±10% Tolerance	10	15	22	33	47	68
	12	18	27	39	56	75
±20% Tolerance	10	15	22	33	47	68

Supersedes Technical Bulletin B5000B Dated June, 1965.

Composition Fixed Resistors
Type CB — ¼ Watt

August 1, 1957

Technical Bulletin **5000D**



Application

Type CB resistors are recommended primarily for application in industrial and commercial electronic equipments where small size, uniform mechanical and electrical characteristics and the highest degree of reliability are desired. They are ideal for use in mobile, airborne, and portable military equipments including transistorized and miniaturized designs. They are recommended also for entertainment devices such as portable radio and television receivers, tape recorders, and high fidelity equipments, etc., where the high quality of these devices is the prime consideration.

Construction

The Type CB resistor is identical in basic design with the Allen-Bradley types EB, GB, and HB resistors which have proven to be the most reliable of ALL electronic components. The resistance material, the mineral filled insulation material, and the headed lead wires are all molded together at one time by means of the exclusive Allen-Bradley hot molding process into a single solid integral structure. There are no cracks or crevices to admit moisture. Lead wires are hardened in the region immediately adjacent the resistor body for superior vibration performance. Headed portions of the lead wires are molded within and are surrounded by resistance material to ensure permanent low resistance contact. The insulation material completely surrounds the resistance material. The resistance material has a relatively large uniform cross section which results in low uniform current densities and complete absence of localized high temperatures or "hot spots". The efficient distribution of heat throughout the mass of the resistor with the elimination of these "hot spots" results in superior performance with respect to the life and short time overloads of several times rating.

Outstanding Features

Reliable

These resistors when used according to published ratings and recommendations will not open circuit nor exhibit erratic changes of resistance value. They are dependable.

Uniform

Rigid quality control insures consistent characteristics and predictable performance.

Small

Type CB resistors are substantially SMALLER than competitive products of comparable ratings.

Easy to Solder

The hot solder coated lead wires can be soldered with ease even after long periods of time in stock.

Packaging

Packaging in strips or in reels for use in automatic assembly operations, prevents the lead wires from becoming bent and tangled.

Rugged

The exclusive Allen-Bradley hot molding process results in a single solid integral structure which is mechanically strong without cracks or crevices.

Appearance

Type CB resistors have a smooth, glossy, attractive surface. The color coding is applied in well defined bands which are clear and distinct. The colors adhere permanently to the resistor body and retain their color when resistors are operated continuously at maximum rated temperature. Color bands are unaffected by most solvents.

Noise

Small rapid variations of resistance which in some applications result in noise or other modulation effects, are extremely low—being of the same order as those resulting from thermal agitation.

Moisture Resistance

These resistors when tested in accordance with MIL-STD-202A Method 106 meet the moisture resistance requirement of MIL-R-11B for ½, 1 and 2 watt resistors.

Temperature Cycling and Thermal Shock

Type CB resistors, as well as Types EB, GB, and HB resistors, are not damaged and exhibit little if any resistance change as a result of exposure to conventional temperature cycling and thermal shock tests including SALT WATER IMMERSION. See MIL-STD-202A.

Commercial and Military Specifications

The performance of Type CB resistors exceeds the highest requirements of Electronic Industries Assn. (formerly RETMA—Radio-Electronic-Television Mfgs. Assn.) standard RS-172 and Military Specification MIL-R-11B.

Specifications

Ambient Temperatures—Suitable for continuous use throughout ambient temperature range of −55°C to +150°C.

Marking—Electronic Industries Assn. standard and MIL-R-11B Color Code (MIL-STD-221).

Resistance—Electronic Industries Assn. standard and MIL-R-11B values presently—47 ohms to 22.0 megohms inclusive.

Resistance Tolerance—±5%, ±10%, and ±20%.

Power—Maximum continuous power 0.25 watt at +70°C. ambient provided maximum continuous voltage rating not exceeded. Derate linearly from maximum continuous power rating at +70°C. ambient to zero at +150°C. ambient.

Voltage—Maximum continuous 250 volts D.C. or 60 cycle RMS provided maximum continuous power rating not exceeded.

Voltage Coefficient—Less than 0.035% resistance change per volt.

Insulation Dielectric Strength—In excess of 500 volts D.C. or 60 cycle RMS.

Insulation Resistance—More than 100,000 MEGOHMS. (Clean and dry).

Test Specification Details—The performance specifications listed in this technical bulletin are based upon results of tests conducted in accordance with the environmental test conditions and procedure details specified in Electronic Industries Assn. standard RS-172 and Military Specifications MIL-R-11B and MIL-STD-202A.

Load Life—Permanent change of resistance less than 6% as a result of operation for 1000 hours (1½ hours "ON" ½ hour "OFF") at 0.25 watt with +70°C. ambient temperature provided maximum continuous voltage of 250 volts D.C. or 60 cycle RMS not exceeded. Compliance with this requirement is the basis for the power and voltage ratings.

Short Time Over Load—Less than 2.5% change of resistance and no mechanical damage as a result of 5 seconds at 6.25 times power rating—1.56 watts, provided voltage across resistor does not exceed 400 volts D.C. or peak 60 cycle A.C. ambient temperature +25° ±5°.

Temperature Cycling and Thermal Shock—Less than 2.0% change of resistance and no mechanical damage as a result of 5 cycles in accordance with Electronic Industries Assn. standard RS-172 or Military Specification MIL-R-11B.

No resultant damage when tested in accordance with the temperature cycling or thermal shock tests, described in Military Specification MIL-STD-202A and listed below.

Method 102A Temperature Cycling—all test conditions.

Method 107 Thermal Shock—test conditions A and B.

Method 104A Immersion Saturated Salt Water—all test conditions.

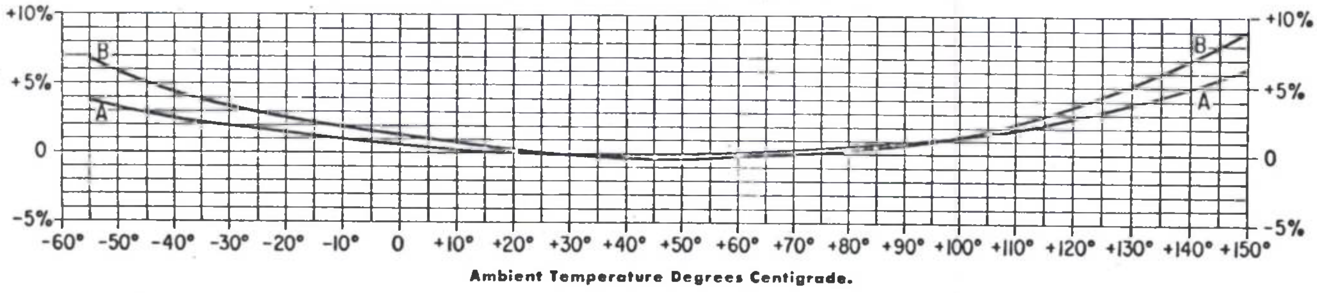
Temperature Characteristic—Same as types EB, GB, and HB. See table and graph.

Temperature Characteristics

Resistance At +25°C.	Maximum Percent Temporary Resistance Change From +25°C. Value At							
	−55°C.	−25°C.	0°C.	+55°C.	+85°C.	+110°C.	+130°C.	+150°C.
47 Ohm	+6.5	+3.5	+2	±2	±2.5	+4.5	+6.5	+8.5
100 Ohm	+6.5	+3.5	+2	±2	±2.5	+4.5	+6.5	+8.5
1,000 Ohm	+8.5	+4.5	+2	±2	±3	+5.5	+8	+10.5
10,000 Ohm	+10	+5.5	+2.5	±2	±3.5	+6.5	+9.5	+12.5
0.1 Megohm	+12	+6.0	+2.5	±2	±4	+7.5	+11	+15
1 Megohm	+14	+7.0	+3.0	±2	±4.5	+8.5	+12.5	+17
10 Megohm	+15	+7.5	+3.0	±2	±5	+9	+13	+18
22 Megohm	+15	+7.5	+3.0	±2	±5	+9	+13	+18

Curves Showing Per Cent Temporary Resistance Changes from Plus 25° Centigrade Values.

A=Resistance 10,000 Ohms; B=Resistance 0.5 Megohm.
Typical data not necessarily average. See above table for Maximum Values.



Specifications

Low Temperature Storage—Less than 2.0% change of resistance and no mechanical damage as a result of 24 hours at −63° +0° −2°C.

Low Temperature Operation—Less than 3.0% change of resistance and no mechanical damage as a result of 45 minutes at ambient temperature of −55° +0° −2°C. under electrical load of 0.25 watt—maximum of 250 volts D.C. or 60 cycle RMS.

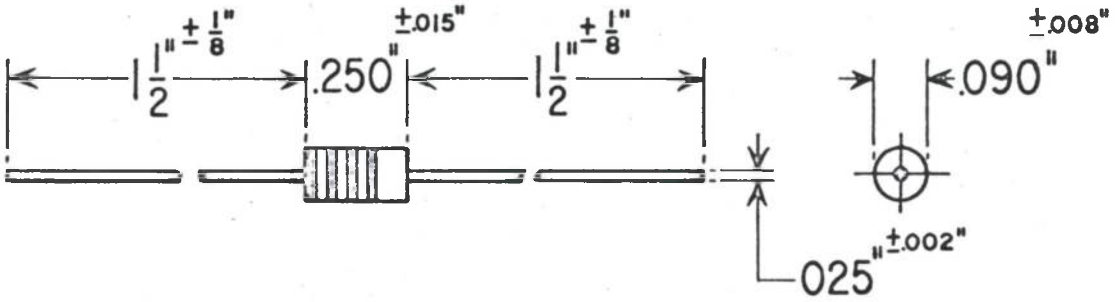
Humidity (Steady State)—Temporary change of resistance less than 10% as a result of exposure to 90 to 95% relative humidity at +40°C. ambient temperature for 250 hours. See MIL-R-11B and MIL-STD-202A, Method 103A all test conditions or Electronic industries Assn. standard RS-172 for details.

Moisture Resistance (Cycling)—Temporary change of resistance less than 10% average as a result of exposure to the cycling test specified in MIL-R-11B and MIL-STD-202A Method 106.

Soldering Characteristic—Change of resistance less than 3.0% as a result of immersion of lead wires one at a time for 3 ± ½ seconds each in a pot of molten solder at a temperature of 350° ± 5°C. to a point within ⅛ to 3/16 inch from the resistor body.

Commercial and Military Specifications—The performance of Type CB resistors exceeds the highest requirements of Electronic Industries Assn. (formerly RETMA—Radio-Electronic-Television Mfgs. Assn.) standard RS-172 and Military Specification MIL-R-11B.

Dimensions



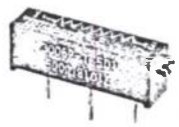
BOURNS INC

Model 3006
Commercial TRIMPOT® Potentiometer
Cermet Element

FEATURES

- Low cost.
- Low PC board profile, only ¼″ off the board.
- Stable cermet element offers continuous resolution.
- High power rating: 0.75 watt at 70°C
- Low temperature coefficient: 100 ppm/°C over —55° to +125°C temperature range.
- Sealed to MIL-R-22097 standard; withstands industrial cleaning processes.
- 16 independent wiper contacts assure excellent setability.
- Wiper assembly idles at both ends of travel eliminating the possibility of damage from forced adjustment.

Actual Size



3006P

3006W

STANDARD RESISTANCES

Resistance (Ohms)	Part Numbers*	
	3006P Printed Circuit Pins	3006W Printed Circuit Pins
10	3006P-1-100	3006W-1-100
20	3006P-1-200	3006W-1-200
50	3006P-1-500	3006W-1-500
100	3006P-1-101	3006W-1-101
200	3006P-1-201	3006W-1-201
500	3006P-1-501	3006W-1-501
1,000	3006P-1-102	3006W-1-102
2,000	3006P-1-202	3006W-1-202
5,000	3006P-1-502	3006W-1-502
10,000	3006P-1-103	3006W-1-103
20,000	3006P-1-203	3006W-1-203
50,000	3006P-1-503	3006W-1-503
100,000	3006P-1-104	3006W-1-104
200,000	3006P-1-204	3006W-1-204
500,000	3006P-1-504	3006W-1-504
1,000,000	3006P-1-105	3006W-1-105
2,000,000	3006P-1-205	3006W-1-205

SPECIAL RESISTANCES AVAILABLE FROM 10 TO 5,000,000 OHMS

*The last three digits of the part number represent the resistance in standard code.

Model 3006 TRIMPOT® Potentiometer

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Standard Resistance Range (see chart on front)	10 to 2,000,000 ohms
Resistance Tolerance*	±10% standard, closer tolerances available
Absolute Minimum Resistance*	3.0% or 1.0 ohm, whichever is greater
Continuity*	Maintained for full mechanical range
Insulation Resistance, 500 volts DC	100 megohms minimum
Contact Resistance Variation, Maximum*	3 ohms or 3%, whichever is greater
Resolution	Infinite
Setability (Voltage Divider)	0.02%

ENVIRONMENTAL CHARACTERISTICS

Power Ratings:	
70°C	0.75 watt
125°C	0 watt
Operating Temperature Range	−55° to +125°C
Temperature Coefficient	±100 ppm/°C all resistances maximum
Humidity, MIL-STD-202, Method 106	20 megohms minimum insulation resistance after removal from chamber
Seal	Meets immersion requirements of MIL-R-22097
Vibration	20Gs
Contact Bounce	0.1 millisecond maximum
Wiper Shift, Maximum	2.0%
Shock	50Gs
Contact Bounce and Wiper Shift	Same as vibration
Load Life	1,000 hours 0.75 watt at 70°C
Mechanical Life	200 cycles without discontinuity
Dielectric Strength	
Room Conditions	1,000 volts AC
80,000 feet (0.8" hg)	250 volts AC

PHYSICAL CHARACTERISTICS

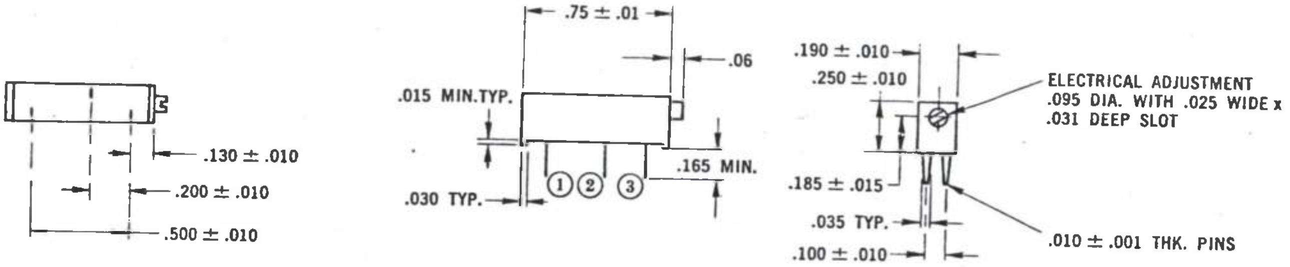
Shaft Torque	5.0 oz.-in. maximum
Markings	Manufacturer's name, wiring diagram, date code, resistance and manufacturer's part number (customer's part number optional)
Appearance	Legible markings, no physical defects
Mechanical Adjustment	15 turns nominal
Mechanical Stops	Wiper assembly idles
Weight	Approximately 0.1 oz.
Terminals	Printed circuit pins

*Inspection Note: 100% or statistical sampling inspection performed to insure highest quality.

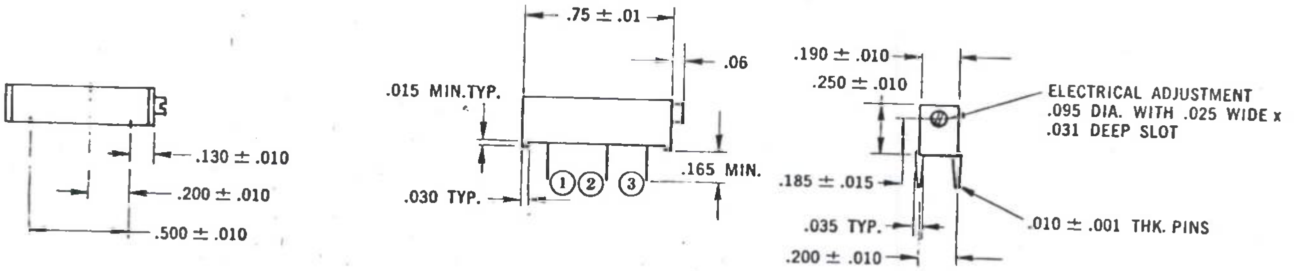
Specification Note: Closer performance tolerances can be supplied upon request.

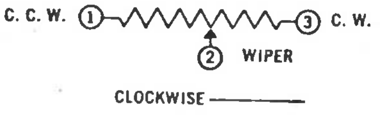
Specifications are subject to change without notice.

3006P



3006W





BOURNS

BOURNS, INC., ELECTRONIC COMPONENTS OPERATIONS, TRIMPOT PRODUCTS DIVISION
1200 COLUMBIA AVENUE, RIVERSIDE, CALIFORNIA 92507
SUBSIDIARY: BOURNS (CANADA) LTD. 36 CRANFIELD RD. EAST YORK, TORONTO, ONTARIO CANADA

Commercial/Industrial
Precision Wirewound
Potentiometers

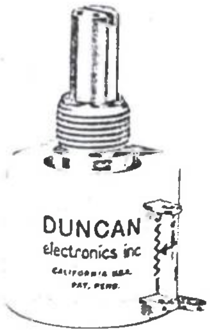
DIAMETER: ⅞"
TURNS: 10
MOUNTING: Bushing

FEATURES

- Low Cost
- Life: 500,000 shaft revolutions
- Power: 2 watts at 20°C
- Temperature range: −25°C to +85°C
- Slotted Stainless Steel Shaft
- Commercial/Industrial type
- High impact plastic housing and rear lid
- Gold-plated terminals
- Welded terminations

B

POTENTIOMETERS



SERIES 3250

DUNCAN ELECTRONICS, INC.

DUNCAN SERIES 3250

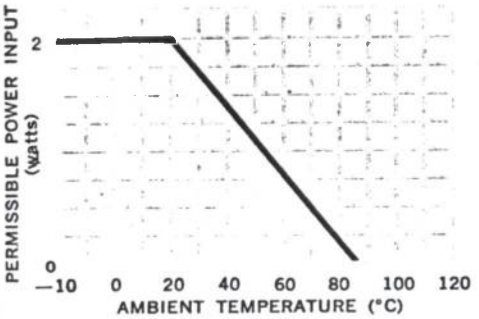
DIAMETER: ⅞"
TURNS: 10
MOUNTING: [illegible]

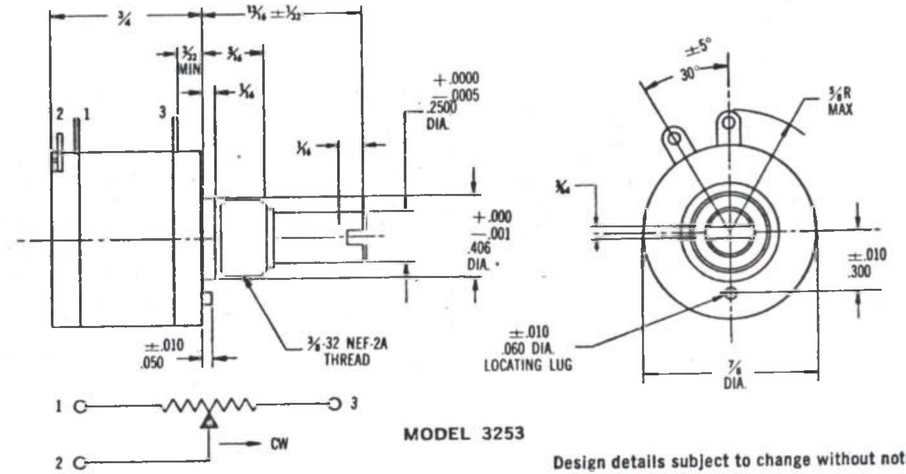
SPECIFICATIONS

Unless shown otherwise, specifications apply to all models of the Series 3250.

ELECTRICAL

Actual Electrical travel (+10° −0°)	3600°
Normal resistance range	100Ω to 100K(¹)
Extended resistance range	25Ω to 150K(¹)
Resistance tolerance, standard	±5%
best practical	±2%
Power rating at 20°C derating to 0 at 85°C (watts—see chart)	2
End resistance	within linearity tolerance or 0.1Ω whichever is greater
Linearity, independent, tolerance, standard	±0.25%
best practical	±0.1%
Equivalent noise resistance, max. (ohms)	100
Insulation resistance at 500 VDC, min. (megohms)	1,000
Dielectric withstanding voltage (volts RMS)	1,000
Total applied voltage, max. (volts DC) (²)	550





MODEL 3253

NOTE: Lock washer and hex nut supplied with each unit.

Design details subject to change without notice.
Certified Drawings available on request.
Tolerances unless otherwise specified:
Fractional: ±1/64" Decimal: ±.005" Angular: ±1°

MECHANICAL

Total mechanical travel (+15° −0°)	3600°
Mechanical life, shaft revolutions, normal conditions	500,000
Cups, max. (number)	1
Moment of inertia, approx. (gm-cm²)	0.3
Weight (oz)	0.5
Stop strength, static (oz-in)	50
Torque: Standard starting, max. (oz.-in)	1.0
Special (designated H.T.) (oz.-in)	.5 ±3

ENVIRONMENTAL

Temperature range, standard	−25°C to +85°C
Humidity and dust protection	enclosed construction
Vibration	10G to 2,000 cycles
Shock	50G

TYPICAL SPECIAL FEATURES AVAILABLE

Shaft lock
Any resistance within the range
Flatted shaft
High Torque

TYPICAL COIL CHARACTERISTICS FOR STOCKED RESISTANCES

RESISTANCE (OHMS)	THEORETICAL RESOLUTION NOMINAL (%)	MAXIMUM APPLIED VOLTAGE (VOLTS DC)
100	.051	14
200	.042	20
500	.036	32
1K	.025	45
2K	.023	63
5K	.021	100
10K	.016	140
20K	.015	200
50K	.011	316
100K	.008	447

All resistances shown are manufactured with resistance wire with temperature coefficient of .002%/°C (20 ppm) nominal.

(¹) All specifications listed apply to units with a total resistance within the normal resistance range. Higher or lower resistances may require some degradation of the listed specifications because of resistance wire composition or size.

(²) Not to exceed specified power rating.

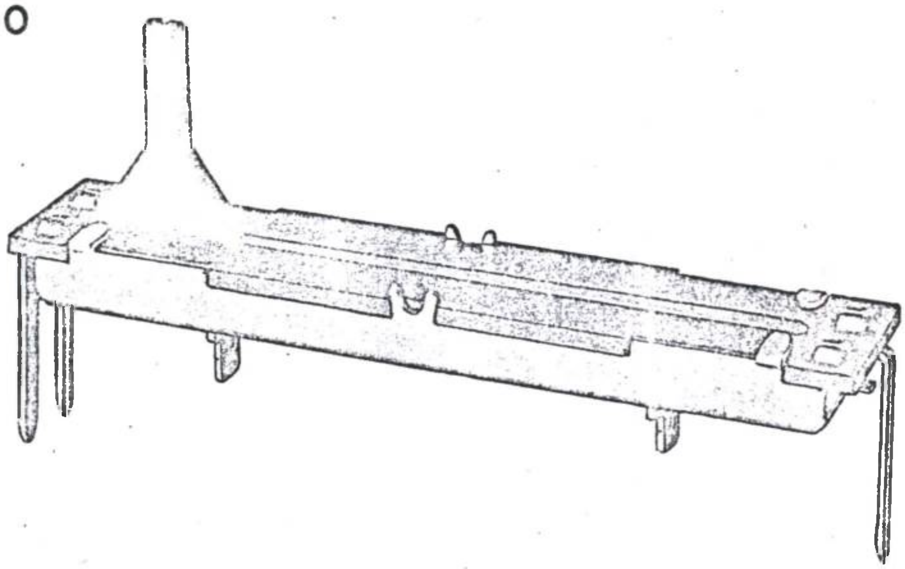
DUNCAN ELECTRONICS
SUBSIDIARY
SYSTRON + DONNER

CTS SERIES 480

LINEAR MOTION COMPOSITION SLIDE CONTROL

- 2" SLIDER TRAVEL
- WIDE RESISTANCE RANGE
- ECONOMICAL
- 1/4 TO 1/2 WATT POWER

SERIES 480



electrical and mechanical specifications

Power Rating:
(Mounted on a metal panel)
100Ω thru 10KΩ at 55°C-1/2 watt
10.1KΩ thru 100KΩ at 55°C-1/3 watt
Above 100KΩ at 55°C - 1/4 watt

Voltage Rating:
Across end terminals
Linear curves -500 VDC
Tapered curves-350 VDC
Between case and end terminals
900 VAC
(Not to exceed wattage rating)

Resistance Range:
100Ω thru 10 MegΩ

Resistance Tolerance:
Std.
100Ω thru 5 MegΩ ±30%
5.1 MegΩ thru 10 MegΩ ±40%
Special
Available

Travel
Mechanical slider travel - 2 inches
Effective electrical " - 2 inches

Operating Force
Either direction-1 1/2 to 6 1/2 ozs.

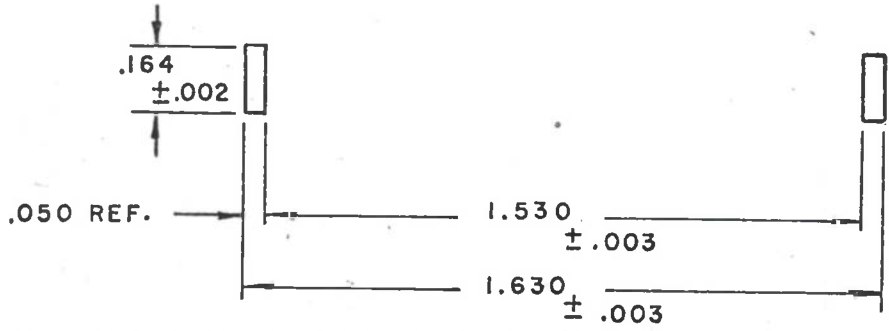
Stop strength
Max. 35 lbs.

Taps:
None available

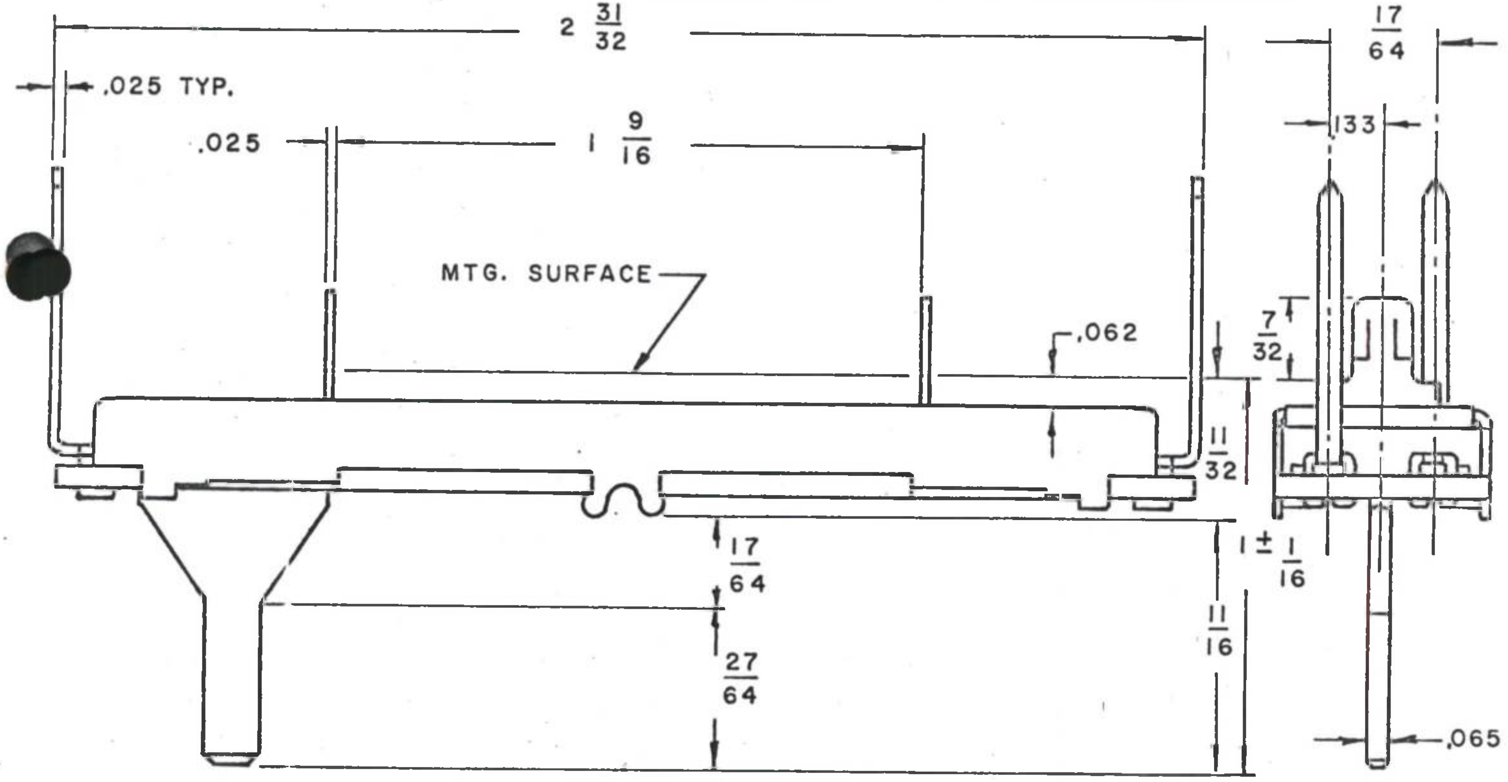
Terminals:
P.C. or wire wrap - formed 90° from plane of slide.
Length - 33/64" FMS

Tapers:
Std. - linear
Special tapers available on request.
On a tapered unit the gradual resistance portion is at the beginning of slider movement away from the double terminal end.

CTS SERIES 480



SUGGESTED PIERCING FOR MOUNTING EARS ON 480 SERIES



GENERAL TOLERANCES: Decimal dimensions ±.005".
Fractional dimensions ±1/64".

order from:

CTS OF ELKHART 1142 W. Beardsley Ave./Elkhart, Indiana

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	MAX.	UNITS	TEST CONDITIONS	
$R_{e(hie)}$	Real Part of Common-Emitter High-Frequency Input Impedance (f = 300 MHz)		60	Ω	$I_C = 20$ mA	$V_{CE} = 20$ V
BV_{CBO}	Collector to Base Breakdown Voltage	60		Volts	$I_C = 10\ \mu A$	$I_E = 0$
V_{CEO}(sust)	Collector to Emitter Sustaining Voltage (Notes 4 and 5)	30		Volts	$I_C = 10$ mA	$I_B = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	5.0		Volts	$I_E = 10\ \mu A$	$I_C = 0$

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operation.
(3) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 143°C/Watt (derating factor of 7.0 mW/°C); junction to ambient thermal resistance of 286°C/Watt (derating factor of 3.5 mW/°C) for the EN2219. For the EN2222 junction to case thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C); junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).
(4) This rating refers to a high-current point where collector to emitter voltage is lowest. For more information send for Fairchild Publication APP-4/2.
(5) Pulse Conditions: length = 300 µs; duty cycle ≤2%.

Fairchild cannot assume responsibility for use of any circuitry described. No circuit patent licenses are implied

EN2219 · EN2222

NPN GENERAL PURPOSE AMPLIFIERS AND SWITCHES

DOUBLE DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

FOR TEST CIRCUITS ADDITIONAL DESIGN INFORMATION SEE FAIRCHILD 2N3299 DATA SHEET

- ELECTRICAL REPLACEMENTS FOR 2N2219 AND 2N2222
- HIGH GAIN - - $h_{FE} = 100\text{-}300$ AT 150 mA
  $h_{FE} = 35$ (MIN) AT 100 μA
  $h_{FE} = 30$ (MIN) AT 500 mA
- MEDIUM VOLTAGE - - $LV_{CEO} = 30$ V (MIN)
- HIGH FREQUENCY - - $f_T = 250$ MHz (MIN) AT 20 mA
- LOW SATURATION VOLTAGE - - $V_{CE}(sat) = 0.4$ V(MAX) AT 150 mA

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Storage Temperature	−65°C to +125°C
Operating Junction Temperature	−65°C to +125°C
Lead Temperature (Soldering, 10 second time limit)	260° Maximum

Maximum Power Dissipation

		EN2219	EN2222
Total Dissipation at 25°C Case Temperature	(Notes 2 and 3)	0.7 Watt	0.5 Watt
at 25°C Ambient Temperature	(Notes 2 and 3)	0.35 Watt	0.2 Watt

Maximum Voltages and Current

V_{CBO}	Collector to Base Voltage		60 Volts
V_{CEO}	Collector to Emitter Voltage	(Note 4)	30 Volts
V_{EBO}	Emitter to Base Voltage		5.0 Volts
I_C	Collector Current		800 mA

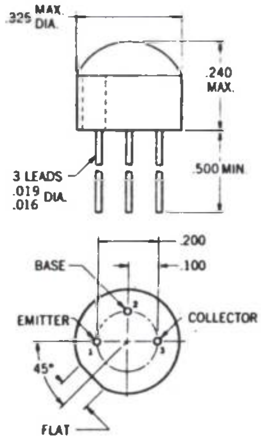
ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	MAX.	UNITS	TEST CONDITIONS	
h_{FE}	DC Pulse Current Gain (Note 5)	100	300		$I_C = 150$ mA	$V_{CE} = 10$ V
h_{FE}	DC Pulse Current Gain (Note 5)	50			$I_C = 150$ mA	$V_{CE} = 1.0$ V
h_{FE}	DC Current Gain	75			$I_C = 10$ mA	$V_{CE} = 10$ V
h_{FE}	DC Current Gain	50			$I_C = 1.0$ mA	$V_{CE} = 10$ V
h_{FE}	DC Current Gain	35			$I_C = 0.1$ mA	$V_{CE} = 10$ V
h_{FE}	DC Pulse Current Gain (Note 5)	30			$I_C = 500$ mA	$V_{CE} = 10$ V
$V_{CE}(sat)$	Collector Saturation Voltage (pulsed, note 5)		0.4	Volts	$I_C = 150$ mA	$I_B = 15$ mA
$V_{CE}(sat)$	Collector Saturation Voltage (pulsed, note 5)		1.6	Volts	$I_C = 500$ mA	$I_B = 50$ mA
$V_{BE}(sat)$	Base Saturation Voltage (pulsed, note 5)		1.3	Volts	$I_C = 150$ mA	$I_B = 15$ mA
$V_{BE}(sat)$	Base Saturation Voltage (pulsed, note 5)		2.6	Volts	$I_C = 500$ mA	$I_B = 50$ mA
h_{fe}	High Frequency Current Gain (f = 100 MHz)	2.5			$I_C = 20$ mA	$V_{CE} = 20$ V
f_T	Gain-Bandwidth Product (f = 100 MHz)	250		MHz	$I_C = 20$ mA	$V_{CE} = 20$ V
I_{CBO}	Collector Cutoff Current		50	nA	$I_E = 0$	$V_{CB} = 50$ V
$I_{CBO}(100°C)$	Collector Cutoff Current		10	μA	$I_E = 0$	$V_{CB} = 50$ V
I_{EBO}	Emitter Cutoff Current		50	nA	$I_C = 0$	$V_{EB} = 3.0$ V
C_{obo}	Output Capacitance		8.0	pF	$I_E = 0$	$V_{CB} = 10$ V

Additional Electrical Characteristics on page 2

PHYSICAL DIMENSIONS

in accordance with JEDEC (TO-105) outline

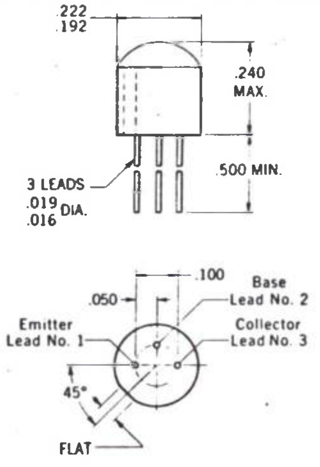


NOTES All dimensions in inches
Leads are gold plated kovar
Package is electrically Non-conductive material
Package weight is 0.66 gram

EN2219

PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-106) outline



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram. Package is electrically non conductive material

EN2222

*Planar is a patented Fairchild process.

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SILICON N-P-N PLANAR TRANSISTOR

2N2270

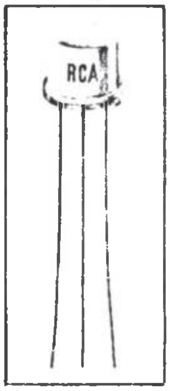
File No. 24

RCA-2N2270 is a *triple-diffused-junction* planar transistor of the silicon n-p-n type intended for a wide variety of small-signal and medium-power applications in military and industrial equipment. It features exceptionally low noise and leakage characteristics, and very low output capacitance.

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE:		
With emitter open.	60 max.	volts
COLLECTOR-TO-EMITTER VOLTAGE:		
With external $R_{BE} \leq$ 10 ohms. .	60 max.	volts
With base open	45 max.	volts
EMITTER-TO-BASE VOLTAGE:		
With collector open.	7 max.	volts
COLLECTOR CURRENT.	1 max.	amp
TRANSISTOR DISSIPATION:		
At case temperatures up to 25° C . .	5 max.	watts
At case temperatures above 25° C . .	See *Rating Chart*	
At free-air temperature up to 25° C . . .	1 max.	watt
At free-air temperature above 25° C . . .	See *Rating Chart*	
TEMPERATURE RANGE:		
Storage.	-65 to +200	°C
Operating (Junction)	-65 to +200	°C
LEAD TEMPERATURE:		
1/16" ± 1/32" from case for 10 sec. max. immersion . .	255 max.	°C

For Small-Signal and Medium-Power Applications



JEDEC TO-5

- minimum gain-bandwidth product = 60 Mc, useful in applications from dc to 20 Mc
- operation at high junction temperatures — up to 200° C
- planar construction — insures low noise and low leakage characteristics
- very low output capacitance

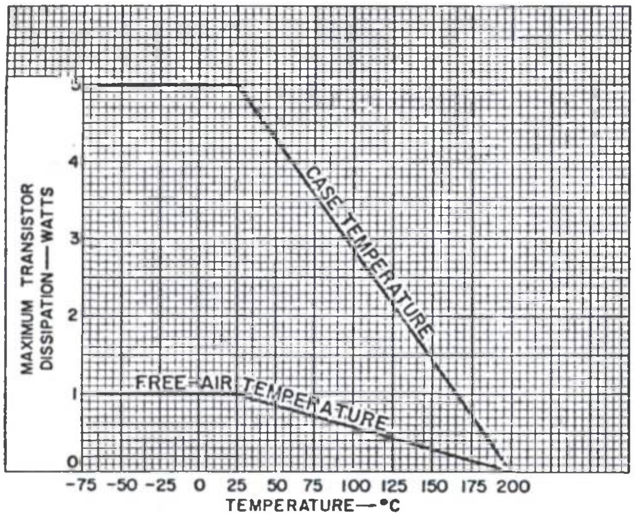


Fig. 1 Rating Chart for Type 2N2270.

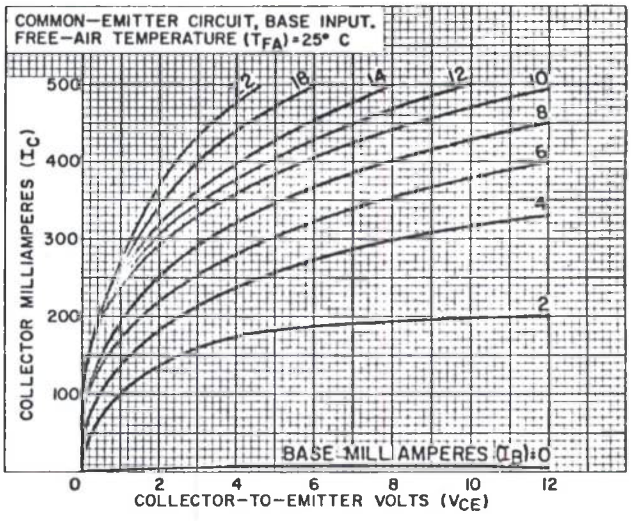


Fig. 2 - Typical Collector Characteristics at 25° C for Type 2N2270.

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ELECTRONIC COMPONENTS AND DEVICES, HARRISON, N.J.

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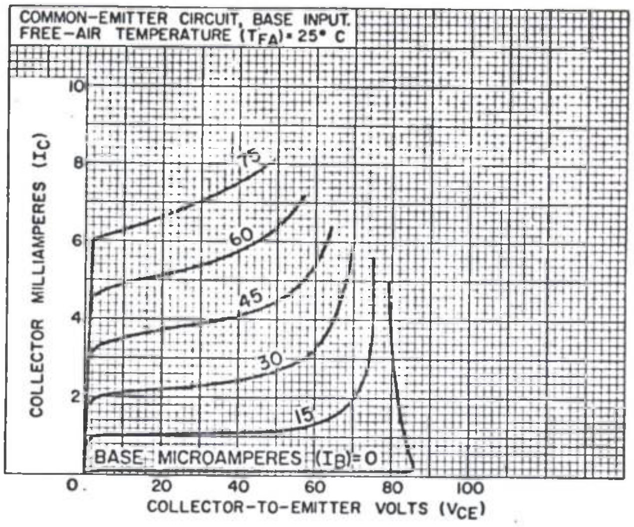
Printed in U.S.A.
2N2270 6/66
Reprinted from 2N2270 2/62

ELECTRICAL CHARACTERISTICS:

At Case Temperature (T_C) of 25° C, unless otherwise specified.

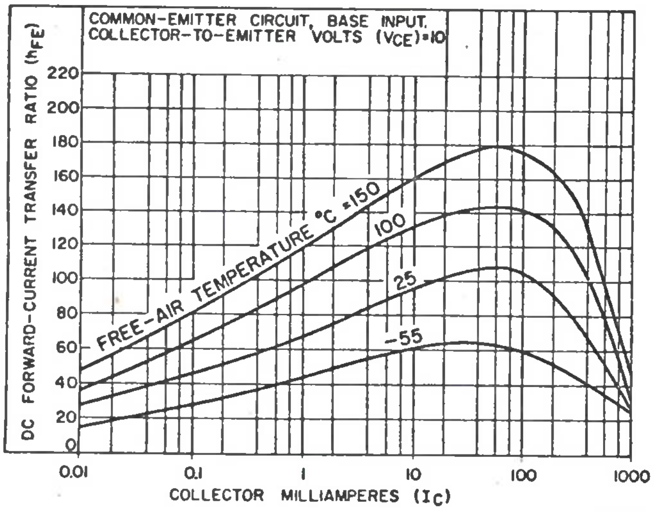
Characteristic	Symbol	TEST CONDITIONS						LIMITS		Units
		DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Emitter-to-Base Voltage V_{EB}	DC Collector Current I_C	DC Emitter Current I_E	DC Base Current I_B	Type 2N2270		
		volts	volts	volts	ma	ma	ma	Min.	Max.	
Collector-Cutoff Current: T_C = 25° C = 150° C	I_{CBO}	60 60				0 0		- -	0.1 50	μa μa
Emitter-Cutoff Current	I_{EBO}			5	0			-	0.1	μa
DC Forward-Current Transfer Ratio	h_{FE}		10 10		150* 1			50 35	200 -	
Collector-to-Base Breakdown Voltage	BV_{CBO}				0.1			60	-	volts
Emitter-to-Base Breakdown Voltage	BV_{EBO}					0.1		7	-	volts
Collector-to-Emitter Sustaining Voltage	$V_{CEO}(sus)$				100*			45	-	volts
Collector-to-Emitter Sustaining Voltage with External Base-to-Emitter Resistance (R_{BE}) = 10 ohms	$V_{CER}(sus)$				100*			60	-	volts
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				150		15	-	0.9	volt
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$				150		15	-	1.2	volts
Small-Signal Forward-Current Transfer Ratio: At frequency of 1 Kc 20 Mc	h_{fe}		10 10		5 50			30 3	180 -	
Noise Figure: Generator resistance (R_G) = 1000 ohms, circuit bandwidth (BW) = 15 Kc, input frequency (f) = 1 Kc	NF		10		0.3			-	6	db
Output Capacitance	C_{ob}	10				0		-	15	pf
Input Capacitance	C_{ib}			0.5	0			-	80	pf
Thermal Resistance: Junction-to-case Junction-to-free air	θ_{J-C} θ_{J-FA}							- -	35 175	°C/W °C/W

* Pulse Test: Pulse duration, 300 μsec; duty factor, 1.8%.



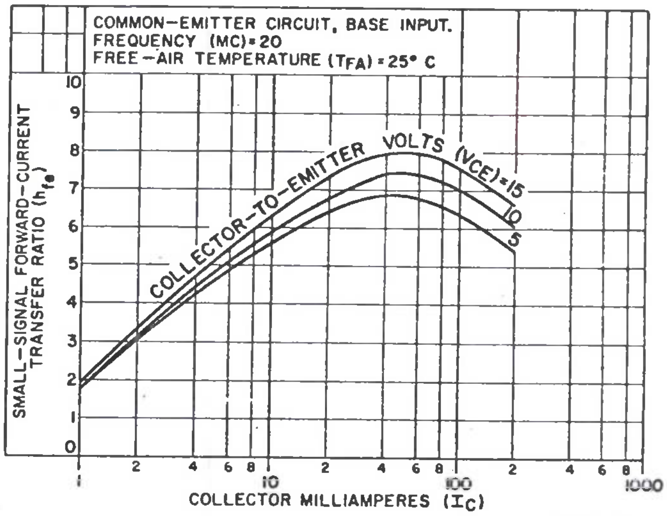
92CS-11175

Fig. 3 - Typical Collector Charaoteristics at 25° C for Type 2N2270.



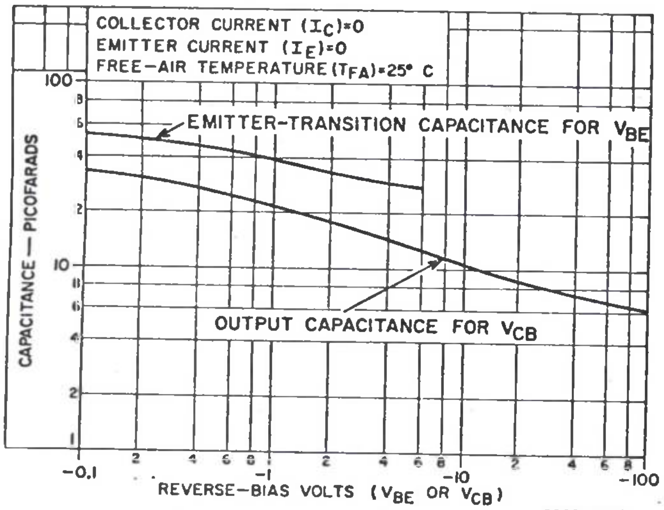
92CS-11181R1

Fig. 4 - Typical DC-Forward-Current Transfer-Ratio Characteristics for Type 2N2270.



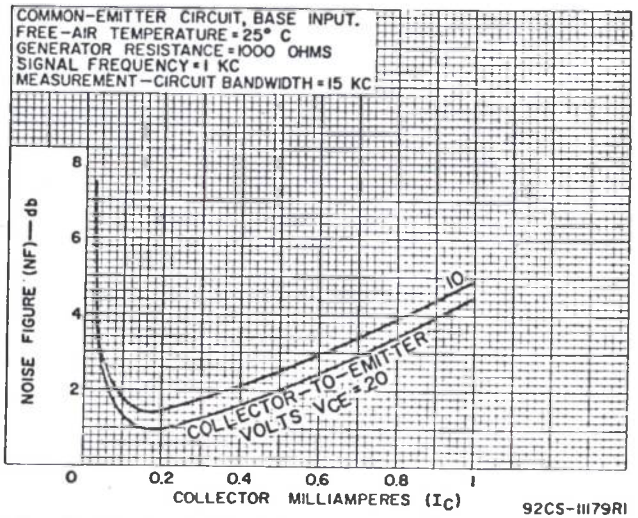
92CS-11171

Fig. 5 - Typical Small-Signal Forward-Current Transfer-Ratio Characteristics for Type 2N2270.



92CS-11195

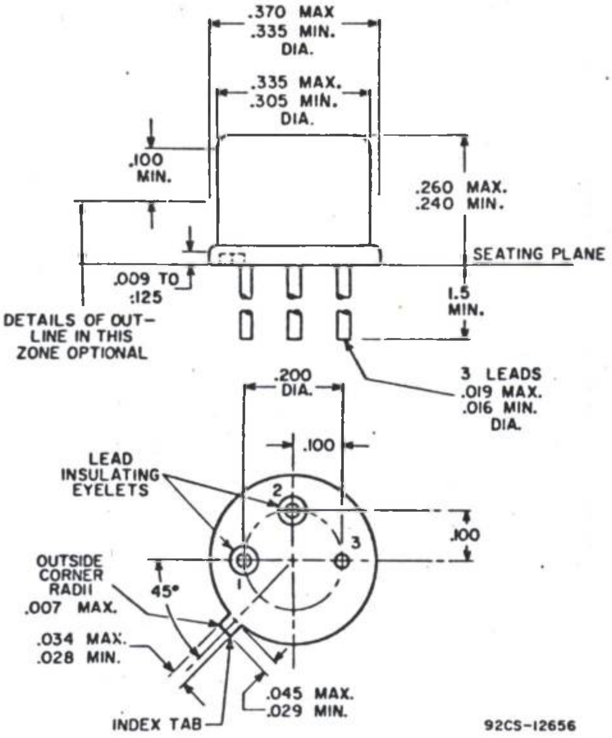
Fig. 6 - Typical Emitter-Transition-Capacitance and Output-Capacitance Characteristics for Type 2N2270.



92CS-11179R1

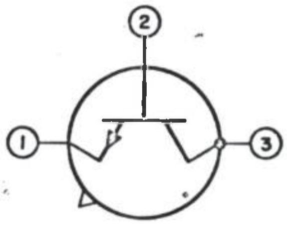
Fig. 7 - Typical AF-Noise-Figure Characteristics for Type 2N2270.

DIMENSIONAL OUTLINE
for Type 2N2270
JEDEC No. TO-5



TERMINAL DIAGRAM

LEAD 1 – EMITTER
LEAD 2 – BASE



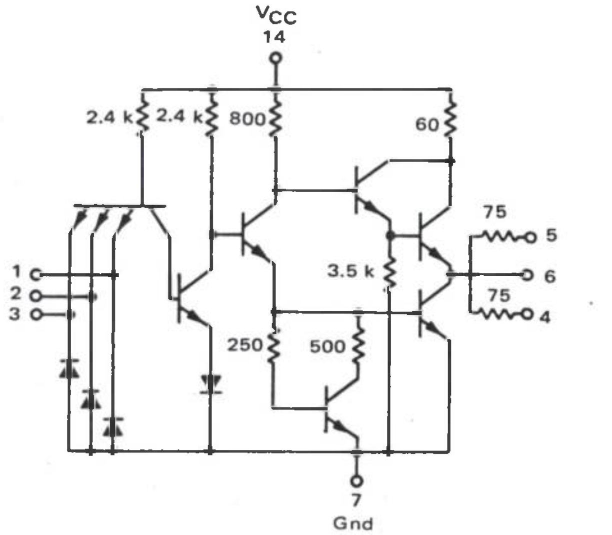
LEAD 3 – COLLECTOR, CASE

DUAL 3-INPUT 3-OUTPUT "AND" SERIES TERMINATED LINE DRIVER

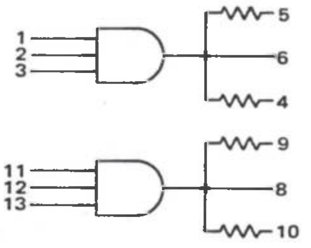
MC3128F • MC3028F
MC3128L • MC3028L,P

MAY 1971

CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN



This device is a dual 3-input/3-output series-terminated AND line driver that minimizes switching transients on long lines by approximating line impedance. Two outputs are provided through 75-ohm resistors for use when driving 93 to 120-ohm lines. These outputs should be paralleled when driving 50 to 93-ohm lines. In addition, an output is provided directly at the gate output node for driving adjacent gates.



Positive Logic: 4, 5, 6, = 1 • 2 • 3
Negative Logic: 4, 5, 6, = 1 + 2 + 3

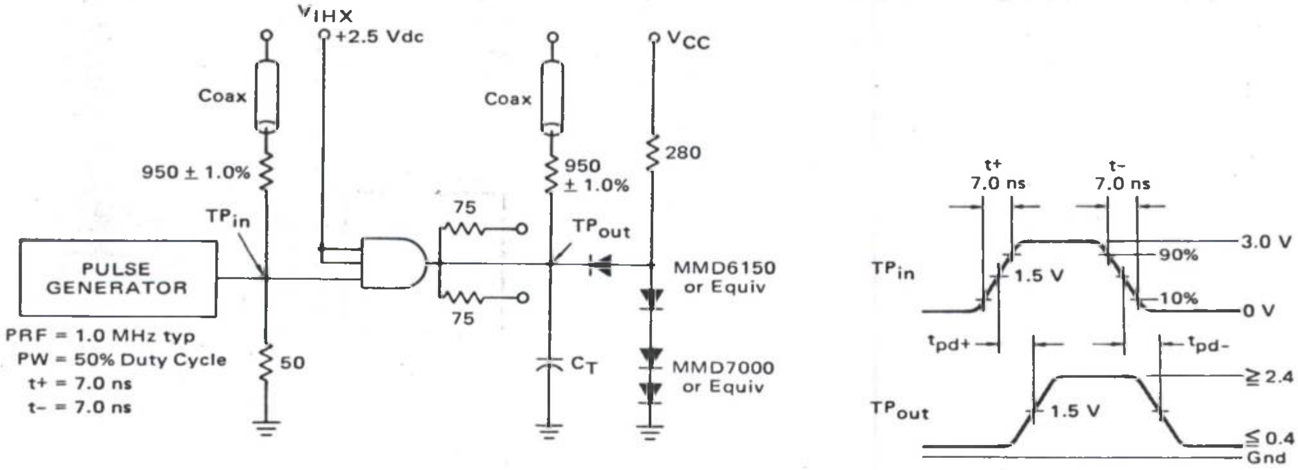
Input Loading Factor = 1

Output Loading Factor, Direct Output (Pins 6 & 8) = 8 minus the number of resistor-terminated outputs being used.

Output Loading Factor, Resistors (Pins 4, 5, 9, & 10) = 1

Total Power Dissipation = 56 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



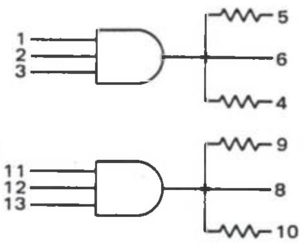
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one line driver. The other line driver is tested in the same manner. Further, test procedures are shown for only one input of the line driver being tested. To complete testing, sequence through remaining inputs.



@ Test Temperature		TEST CURRENT/VOLTAGE VALUES																	
		mA								Volts									
		I_{OLA}	I_{OLB}	I_{OLC}	I_{OHA}	I_{OHB}	I_{OHC}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC3128	-55°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
	+25°C	16	2.0	2.0	-1.8	-0.1	-0.1	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
	+125°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3028	0°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
	+25°C	16	2.0	2.0	-1.8	-0.1	-0.1	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
	+75°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

Characteristic	Symbol	Pin Under Test	MC3128 Test Limits						MC3028 Test Limits						Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																		Gnd
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C																					
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		I_{OLA}	I_{OLB}	I_{OLC}	I_{OHA}	I_{OHB}	I_{OHC}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	
Input Forward Current	I_{F2}	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc	-	-	-	-	-	-	-	-	-	-	1	-	2, 3*	-	-	-	14	-	7
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	-	-	-	-	1	*	-	-	-	14	-	2, 3, 7
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	-	-	-	-	1	-	-	-	-	-	*	-	-	-	14	-	2, 3, 7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	-	-	-	-	1	-	-	-	-	*	-	-	14	-	-	7
Output Output Voltage	V_{OL1}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	5	4	-	-	-	-	-	1	-	-	-	2, 3*	-	-	14	-	-	7
	V_{OL2}	5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	Vdc	6	5	4	-	-	-	-	-	1	-	-	-	2, 3*	-	-	14	-	-	7
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	-	-	6	5	4	-	-	-	1	-	-	2, 3*	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	6	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3*	-	-	-	14	-	6, 7
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	18	-	-	-	-	-	18	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	14	-	-	-	-	7
Power Supply Drain	I_{PDH}	14	-	13.2	-	13.2	-	13.2	-	13.2	-	13.2	-	13.2	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	-	-	-	14	-	7
	I_{PDL}	14	-	26.4	-	26.4	-	26.4	-	26.4	-	26.4	-	26.4	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 3, 7 11, 12, 13
Switching Parameters																Pulse In	Pulse Out																	
Turn-On Delay	t_{pd-}	1, 6	-	-	-	15	-	-	-	-	-	15	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	-	*	-	14	-	-	2, 3	7
Turn-Off Delay	t_{pd+}	1, 6	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	-	*	-	14	-	-	2, 3	7

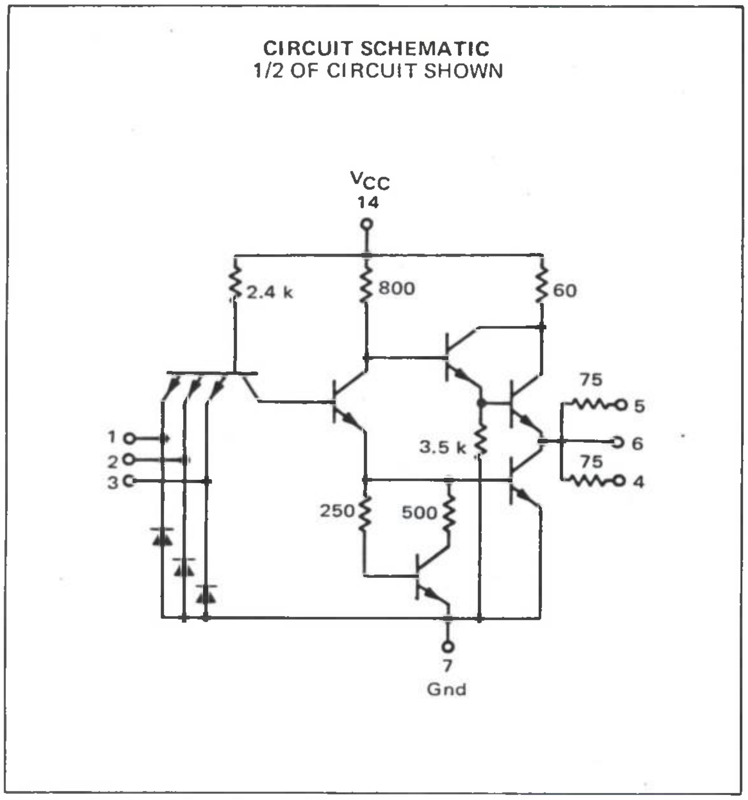
*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}.

3552-21 PRINTED IN USA 4-71 IMPERIAL LITHO B22347 5M

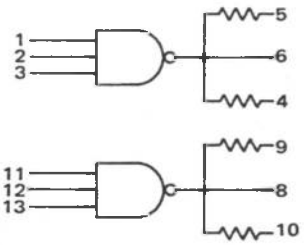
DUAL 3-INPUT 3-OUTPUT
"NAND" SERIES TERMINATED
LINE DRIVER

MC3129F • MC3029F
MC3129L • MC3029L,P

MAY 1971


CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN

This device is a dual 3-input/3-output series-terminated NAND line driver that minimizes switching transients on long lines by approximating line impedance. Two outputs are provided through 75-ohm resistors for use when driving 93 to 120-ohm lines. These outputs should be paralleled when driving 50 to 93-ohm lines. In addition, an output is provided directly at the gate output node for driving adjacent gates.



Positive Logic: 4, 5, 6 = $\overline{1 \cdot 2 \cdot 3}$

Negative Logic: 4, 5, 6 = $\overline{1 + 2 + 3}$

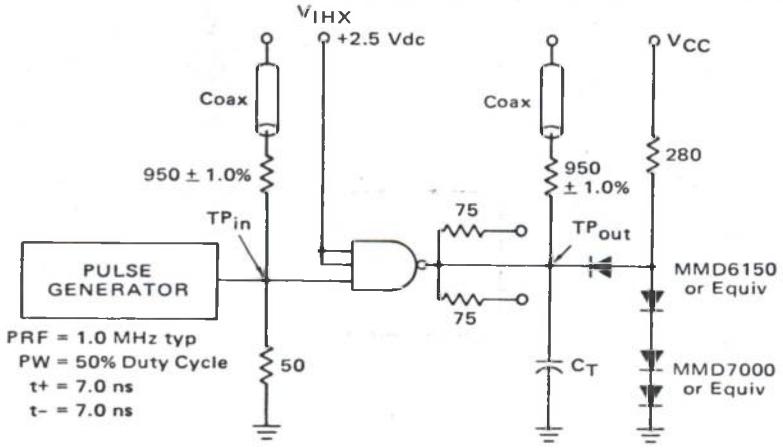
Input Loading Factor = 1

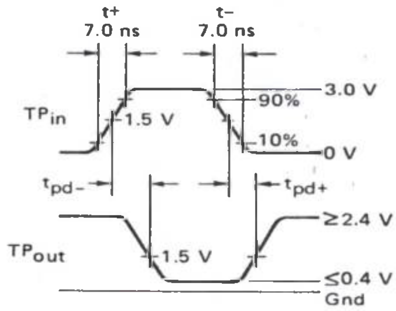
Output Loading Factor, Direct Output (Pins 6 and 8) = 8 Minus The Number of Resistor-Terminated Outputs Being Used.

Output Loading Factor, Resistors (Pins 4, 5, 9 and 10) = 1

Total Power Dissipation = 44 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





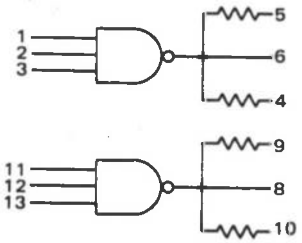
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one line driver The other line driver is tested in the same manner. Further, test procedures are shown for only one input of the line driver under test. To complete testing sequence through remaining inputs.



	@ Test Temperature	$I_{OL A}$ (mA)	$I_{OL B}$ (mA)	$I_{OL C}$ (mA)	$I_{OH A}$ (mA)	$I_{OH B}$ (mA)	$I_{OH C}$ (mA)	I_{in} (mA)	I_D (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_{RH} (Volts)	V_{max} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	V_{IHX} (Volts)
MC3129	−55°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
	+25°C	16	2.0	2.0	-1.8	-0.1	-0.1	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
	+125°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3029	0°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
	+25°C	16	2.0	2.0	-1.8	-0.1	-0.1	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
	+75°C	16	2.0	2.0	-1.8	-0.1	-0.1	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

Characteristic	Symbol	Pin Under Test	MC3129 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3029 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	mAdc
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	µAdc
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc
Output Output Voltage	V_{OL1}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc
	V_{OL2}	5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	Vdc
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc
Short-Circuit Current	I_{SC}	6	-40	-100	-40	-100		-100	-40	-100	-40	-100	-40	-100	mAdc
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	12	-	-	-	-	-	12	-	-	mAdc
Power Supply Drain	I_{PDH}	14	-	19	-	19	-	19	-	19	-	19	-	19	mAdc
	I_{PDL}	14	-	9.6	-	9.6	-	9.6	-	9.6	-	9.6	-	9.6	mAdc
Switching Parameters Turn-On Delay	t_{pd-}	1, 6	-	-	-	10	-	-	-	-	-	10	-	-	ns
Turn-Off Delay	t_{pd+}	1, 6	-	-	-	10	-	-	-	-	-	10	-	-	ns

TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:

Characteristic	Symbol	$I_{OL A}$	$I_{OL B}$	$I_{OL C}$	$I_{OH A}$	$I_{OH B}$	$I_{OH C}$	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Forward Current	I_F	-	-	-	-	-	-	-	-	-	-	1	-	2, 3	-	-	-	14	-	7*
Leakage Current	I_R	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 3, 7*
Breakdown Voltage	BV_{in}	-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 3, 7*
Clamp Voltage	V_D	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7*
Output Voltage	V_{OL1}	6	5	4	-	-	-	-	-	-	1	-	-	2, 3	-	-	14	-	-	7*
	V_{OL2}	6	5	4	-	-	-	-	-	-	1	-	-	2, 3	-	-	14	-	-	7*
	V_{OH}	-	-	-	6	4	5	-	-	1	-	-	-	2, 3	-	-	14	-	-	7*
Short-Circuit Current	I_{SC}	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 3, 6, 7*
Maximum Power Supply Current	I_{max}	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 3, 7, 11, 12, 13
Power Supply Drain	I_{PDH}	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	-	-	-	14	-	7
	I_{PDL}	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1, 2, 3, 7, 11, 12, 13
Turn-On Delay	t_{pd-}	Pulse In 1	Pulse Out 6	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	2, 3	7*
Turn-Off Delay	t_{pd+}	1	6	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	2, 3	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

MOTOROLA Semiconductor Products Inc.
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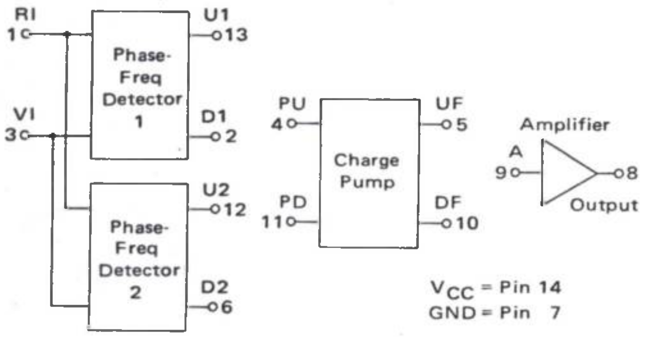
3552-21 PRINTED IN USA 4-71 IMPERIAL LITHO B22347 5M

PHASE-FREQUENCY
DETECTOR

OCTOBER 1970

MC4344F,L*
MC4044F,L,P*



Input Loading Factor: RI, VI = 3

Output Loading Factor (Pin 8) = 10

Total Power Dissipation = 85 mW typ/pkg

Propagation Delay Time = 9.0 ns typ (thru phase detector)

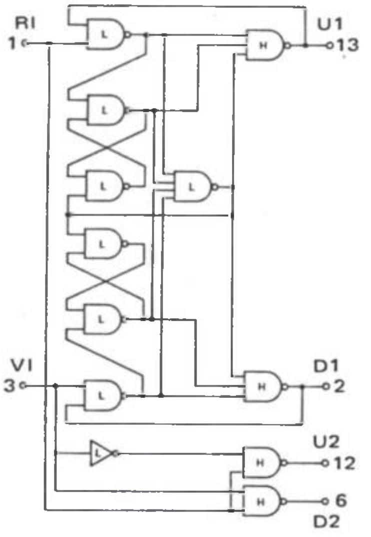
This device contains two digital phase detectors and a charge pump circuit which converts MTTL inputs to a dc voltage level for use in frequency discrimination and phase-locked-loop applications.

The two phase detectors have common inputs. Phase-frequency detector 1 is locked in (indicated by both outputs high) when the negative transitions of the variable input (VI) and reference input (RI) are equal in frequency and phase. If the variable input is lower in frequency or lags in phase, the U1 (up) output goes low; conversely the D1 (down) output goes low when the variable input is higher in frequency or leads the reference input in phase. It is important to note that the duty cycles of the variable input and the reference input are not important since negative transitions control system operation.

Phase detector 2, on the other hand, is locked in when the variable input phase lags the reference phase by 90° (indicated by the U2 and D2 outputs alternately going low with equal pulse widths). If the variable input phase lags by more than 90°, U2 will remain low longer than D2, and, conversely, if the variable input phase lags the reference phase by less than 90°, D2 remains low longer. In this phase detector the variable input and the reference must have 50% duty cycles.

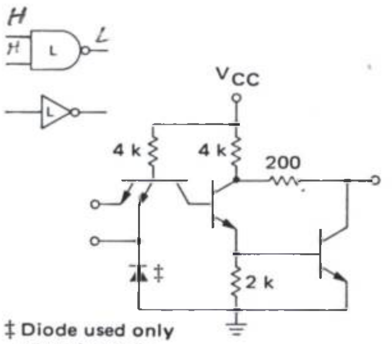
The charge pump accepts the phase detector outputs (U1 or U2 applied to PU, and D1 or D2 applied to PD) and converts them to fixed amplitude positive and negative pulses at the UF and DF outputs respectively. These pulses are applied to a lag-lead active filter, which incorporates external components, as well as the amplifier provided in the MC4344/4044 circuit. The filter provides a dc voltage proportional to the phase error.

PHASE DETECTOR



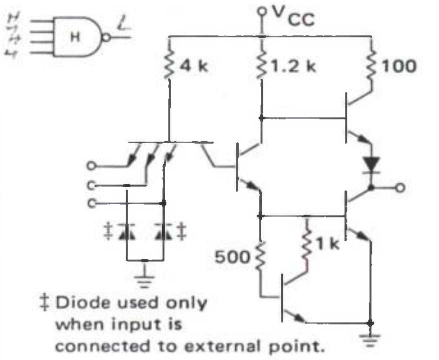
The phase detector portion of this device is constructed using low and high-level gates interconnected as shown by the logic diagram.

LOW-LEVEL "NAND" GATE



‡ Diode used only when input is connected to external point.

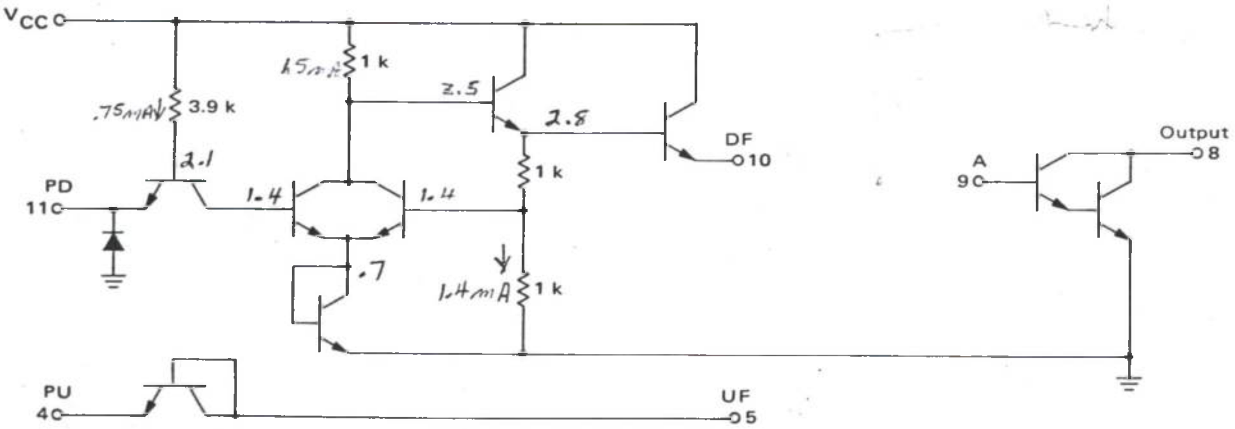
HIGH-LEVEL "NAND" GATE



‡ Diode used only when input is connected to external point.

CHARGE PUMP

AMPLIFIER



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*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

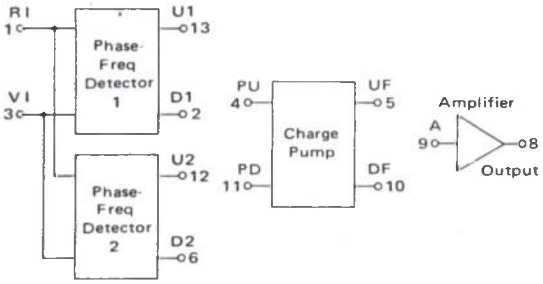
INPUT STATE	INPUT RI	INPUT VI	OUTPUT U1	OUTPUT D1	OUTPUT U2	OUTPUT D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	X	X	1	1
8	1	0	X	X	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not show all possible modes of operation. It is useful for dc testing.

1. X indicates output state unknown.
2. U1 and D1 outputs are sequential; i.e., they must be sequenced in order shown.
3. U2 and D2 outputs are combinational; i.e., they need only inputs shown to obtain outputs.

ELECTRICAL CHARACTERISTICS



TEST CURRENT/VOLTAGE VALUES

	@ Test Temperature	I_{OL} (mA)	I_{OH1} (mA)	I_{OH2} (mA)	I_{in} (mA)	I_D (mA)	I_A (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_{RH} (Volts)	V_{out} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)
MC4344	-55°C	20	-1.6	-1.0	–	–	0.002	1.1	2.0	0.4	2.4	4.5	1.5	5.0	4.5	5.5
	+25°C	20	-1.6	-1.0	1.0	-10	0.002	1.1	1.8	0.4	2.4	4.5	1.5	5.0	4.5	5.5
	+125°C	20	-1.6	-1.0	–	–	0.002	0.9	1.8	0.4	2.4	4.5	1.5	5.0	4.5	5.5
MC4044	0°C	20	-1.6	-1.0	–	–	0.002	1.1	2.0	0.4	2.5	4.5	1.5	5.0	4.75	5.25
	+25°C	20	-1.6	-1.0	1.0	-10	0.002	1.1	1.8	0.4	2.5	4.5	1.5	5.0	4.75	5.25
	+75°C	20	-1.6	-1.0	–	–	0.002	0.9	1.8	0.4	2.5	4.5	1.5	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4344 Test Limits -55°C Min	Max	+25°C Min	Max	+125°C Min	Max	MC4044 Test Limits 0°C Min	Max	+25°C Min	Max	+75°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH1}	I_{OH2}	I_{in}	I_D	I_A	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{out}	V_{CC}	V_{CCL}	V_{CCH}	Pulse 1	Gnd
Input Forward Current	I_F	1	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	mAdc	–	–	–	–	–	–	–	–	1	–	–	–	–	–	14	–	7
		3	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	↓	–	–	–	–	–	–	–	–	3	–	–	–	–	–	↓	–	↓
		11	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	–	–	–	11	–	–	–	–	–		–	
Leakage Current	I_R	1	–	120	–	120	–	120	–	120	–	120	–	120	µAdc	–	–	–	–	–	–	–	–	–	1	–	–	–	–	14	–	7
		3	–	120	–	120	–	120	–	120	–	120	–	120	↓	–	–	–	–	–	–	–	–	–	3	–	–	–	–	14	–	7
		4	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0		–	–	–	–	–	–	–	–	–	–	–	–	–	–	4	–	5,7
		11	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	–	–	–	11	–	–	–	–	14	–	7
Breakdown Voltage	BV_{in}	1	–	–	5.5	–	–	–	–	–	5.5	–	–	–	Vdc	–	–	–	1	–	–	–	–	–	–	–	–	–	–	14	–	7
		3	–	–	↓	–	–	–	–	–	↓	–	–	–	↓	–	–	–	3	–	–	–	–	–	–	–	–	–	–	↓	–	↓
		11	–	–		–	–	–	–	–		–	–	–		–	–	–	11	–	–	–	–	–	–	–	–	–	–		–	
Clamp Voltage	V_D	1	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	1	–	–	–	–	–	–	–	–	14	–	–	7
		3	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	3	–	–	–	–	–	–	–	–	14	–	–	7
Output (Note 1) Output Voltage	V_{OH}	6	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	6	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
		12	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	12	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	**	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OL}	6	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	6	–	–	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
	V_{OH}	12	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	12	–	–	–	–	–	1,3	–	–	–	–	–	14	–	–	7
	**	–	–	–	–	–	–	–	–	–	–	–	–	–	Vdc	–	–	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	**	–	–	–	–	–	–	–	–	–	–	–	–	–	Vdc	–	–	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OH}	6	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	6	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OL}	12	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	12	–	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	**	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	**	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OL}	13	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	13	–	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OL}	13	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	13	–	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
		13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
		13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OL}	2	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	2	–	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OL}	2	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	2	–	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1	3	–	–	–	–	–	14	–	–	7
	V_{OL}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	2	–	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
	V_{OL}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	2	–	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	3	1	–	–	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
		13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	1,3	–	–	–	–	–	–	14	–	–	7
Short-Circuit Current	I_{SC}	2	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	–	–	–	3	1	–	–	–	–	–	–	–	14	2,7
		6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	–	–	1,3	–	–	–	–	–	14	–	–	–	6,7
		12														–	–	–	–	–	–	1,3	–	–	–	–	–	↓	–	–	–	7,12
		13														–	–	–	–	–	–	3	1	–	–	–	–		–	–	–	7,13
Leakage Current	I_{OLK}	2	–	250	–	250	–	250	–	250	–	250	–	250	µAdc	–	–	–	–	–	–	3	1	–	–	–	–	14	–	–	–	7
		6	–	↓	–	↓	–	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	–	–	1,3	–	–	–	–	–	↓	–	–	–	↓
		12	–		–		–		–		–		–			–	–	–	–	–	–	1,3	–	–	–	–	–		–	–	–	
		13	–		–		–		–		–		–			–	–	–	–	–	–	3	1	–	–	–	–		–	–	–	
Collector-Emitter Voltage	V_{CE}	5	–	–	0.5	–	–	–	–	–	0.5	–	–	–	Vdc	–	–	–	5	–	–	–	–	–	–	–	–	–	–	–	–	4,7
Output Voltage	V_{EH}	10	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	Vdc	–	–	10	–	–	–	11	–	–	–	–	–	–	14	–	–	7
Output Current	I_O	8	0.2	–	0.8	–	1.0	–	0.5	–	0.8	–	1.0	–	mAdc	–	–	–	–	–	9	–	–	–	–	–	–	–	–	8	–	7
Leakage Current	I_{OLK}	8	–	120	–	120	–	120	–	120	–	120	–	120	µAdc	–	–	–	–	–	–	–	–	–	–	–	–	–	–	8	–	7,9
		10	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	µAdc	–	–	–	–	–	–	–	–	–	11	10	–	–	–	14	–	7
Power Requirements (Total Device) Power Supply Drain	I_{PD}	14	–	40	–	40	–	40	–	40	–	40	–	40	mAdc	–	–	–	–	–	–	–	–	–	–	–	–	14	–	–	–	7

Note 1. The outputs of the device must be tested by sequencing through the indicated input states according to the truth table and functional diagram. All input, power supply and ground voltages must be maintained between tests unless otherwise noted. Procedures identified by a double asterisk (**) in the Symbol column are necessary to change the state of the sequential logic.

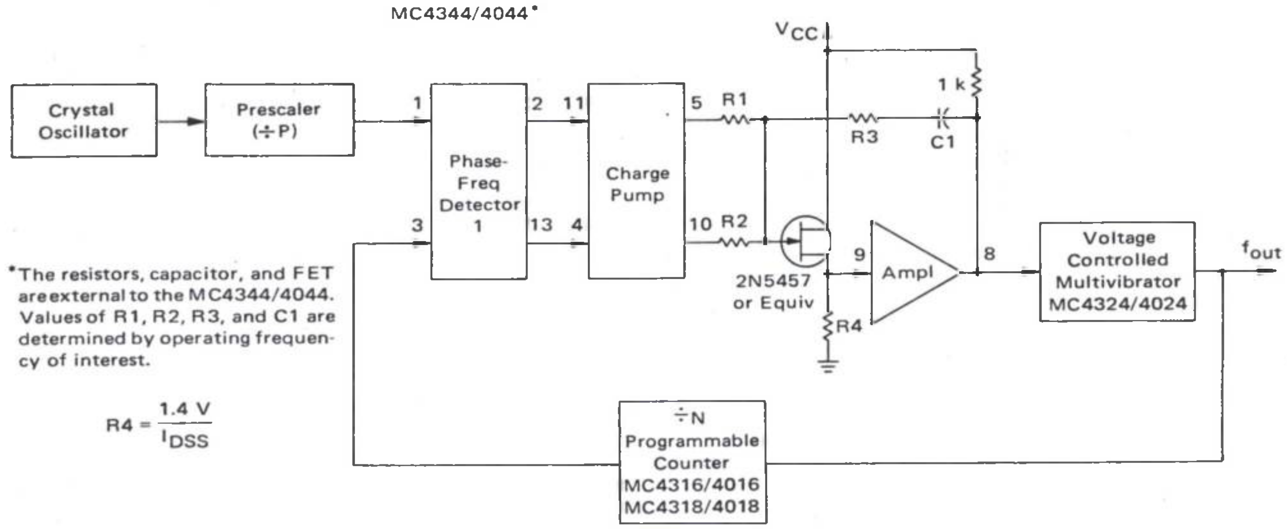
Pulse 1: $V_{CCL} \to V_{CC}$ Used to change power supply voltage from previous test.

APPLICATIONS INFORMATION

FIGURE 1 – PHASE-LOCKED,
FREQUENCY SYNTHESIZER LOOP

Figure 1 shows the MC4344/4044 in a phase-locked loop with the following features:

1. Zero phase error between the reference frequency and the output of the divide-by-N feedback, achieved because phase-frequency detector 1 locks negative edges in the system;
2. Adjustable channel spacing, achieved by changing the prescaling factor (÷ P) when generating the reference frequency;
3. Digitally programmed tuning of the output, in multiples of the reference frequency, accomplished by changing N in the divide-by-N chain in the feedback loop.

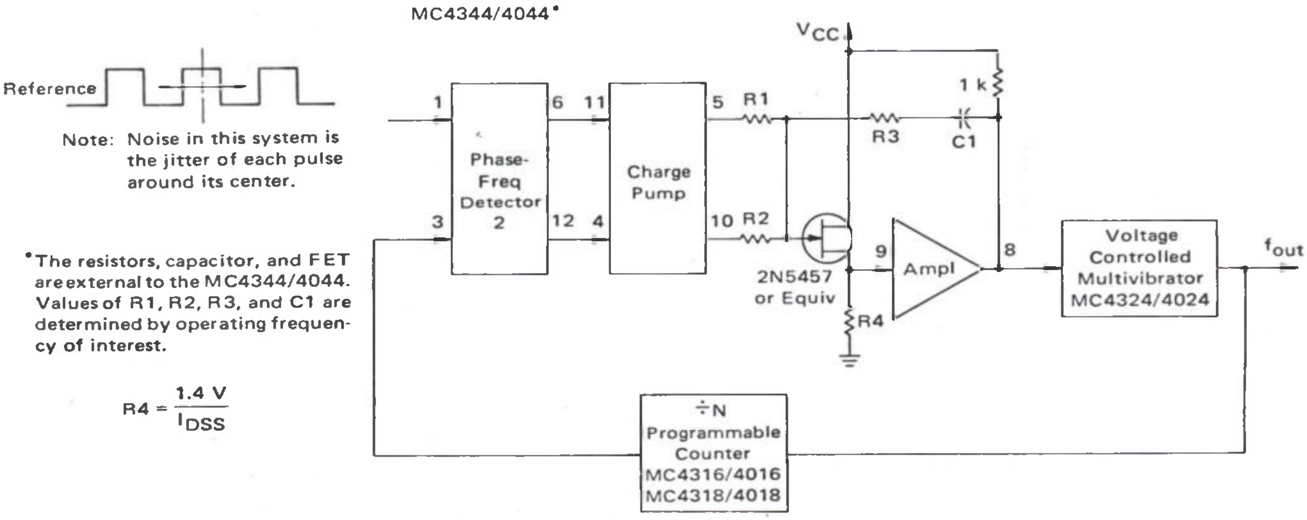


*The resistors, capacitor, and FET are external to the MC4344/4044. Values of R1, R2, R3, and C1 are determined by operating frequency of interest.

$$R4 = \frac{1.4\ V}{I_{DSS}}$$

Figure 2 shows phase detector 2 of the MC4344/4044, which operates as a correlation detector, used in a phase-locked loop. There are two differences between this system and that shown in Figure 1. First, the VCM output, when locked in, lags the reference by 90°. Second, since the correlation detector integrates the product of its two inputs over each cycle, it can handle signals in a high-noise environment. This loop is sensitive to harmonics, therefore care must be taken to limit the frequency range of the VCM.

FIGURE 2 – PHASE-LOCKED,
CORRELATION DETECTOR LOOP



Note: Noise in this system is the jitter of each pulse around its center.

*The resistors, capacitor, and FET are external to the MC4344/4044. Values of R1, R2, R3, and C1 are determined by operating frequency of interest.

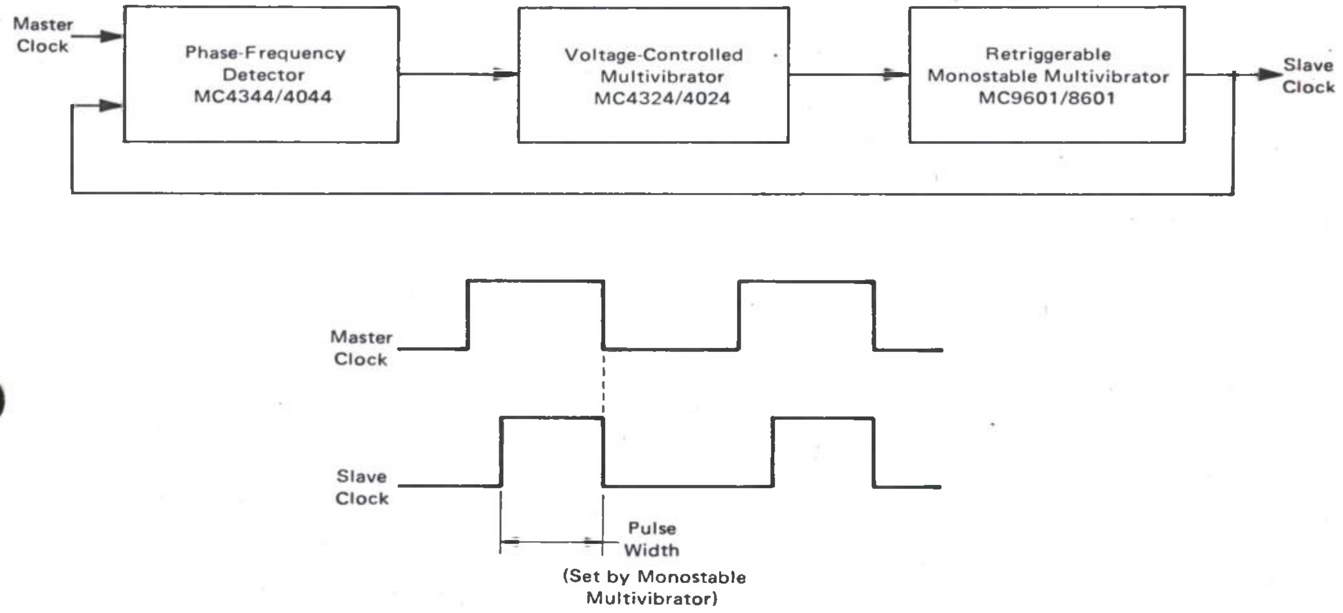
$$R4 = \frac{1.4\ V}{I_{DSS}}$$

APPLICATIONS INFORMATION (continued)

FIGURE 3 – SLAVE CLOCK PULSE GENERATOR

Figure 3 depicts the MC4344/4044 in a system used to generate a slave clock pulse with its negative edge locked to the negative edge of the master clock, but with adjustable pulse width. The pulse width of the slave clock pulse is controlled only by the monostable multivibrator, which is triggered from the negative edge of an input pulse.

The slave clock application is useful when the clock from a master computer must be slaved to that of a satellite.


Master Clock
Phase-Frequency Detector MC4344/4044
Voltage-Controlled Multivibrator MC4324/4024
Retriggerable Monostable Multivibrator MC9601/8601
Slave Clock
Master Clock
Slave Clock
Pulse Width
(Set by Monostable Multivibrator)

4211-37 PRINTED IN USA 12-70 IMPERIAL LITHO 820300 18M
DS 9108

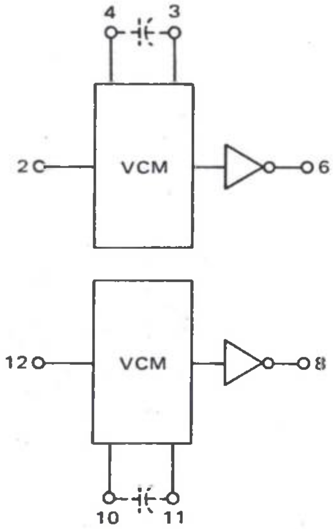
DUAL
VOLTAGE-CONTROLLED
MULTIVIBRATOR

MC4324F, L*
MC4024F, L, P*

OCTOBER 1971

The MC4324/4024 voltage-controlled multivibrator provides appropriate level shifting to produce an output compatible with MTTL logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single capacitor. Variation of the output frequency over a 3.5 to 1 range is possible with an input dc control voltage of +1.0 to +5.0 volts.

Voltage-controlled multivibrators are used in phase-locked loops for digital frequency control. They may also be used for some types of A to D converters.

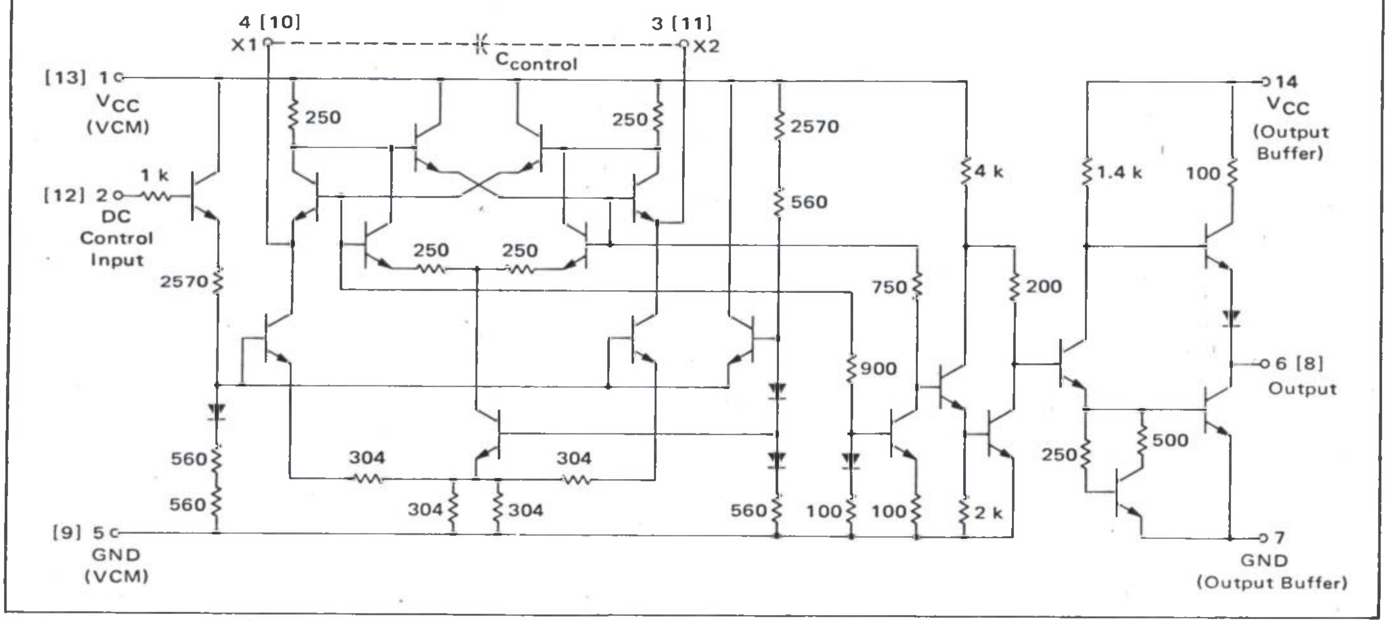


V_{CC}: VCM = 1, 13
Output Buffer = 14
GND: VCM = 5, 9
Output Buffer = 7
External Capacitor for
Frequency Range Determination
Output Loading Factor = 7
Power Dissipation = 150 mW typ/pkg
Maximum Operating Frequency = 30 MHz typ

CIRCUIT SCHEMATIC

1/2 OF CIRCUIT SHOWN

(Numbers in brackets are pin numbers for other half.)



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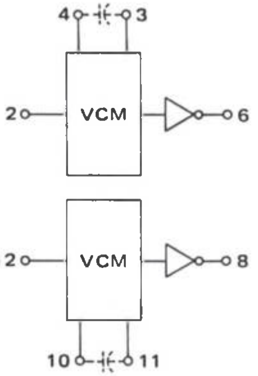
*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

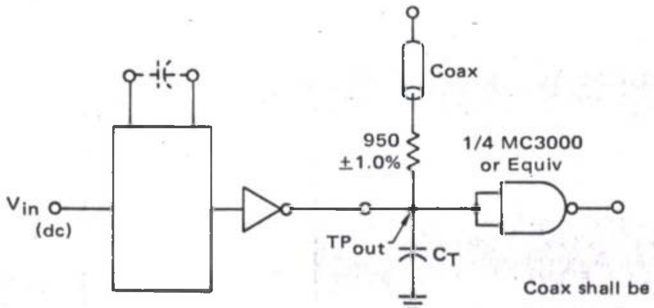


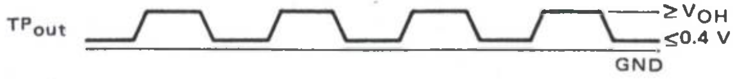
	@ Test Temperature	mA			Volts			
		I_{OL1}	I_{OL2}	I_{OH}	V_{IH}	V_{CC}	V_{CCL}	V_{CCH}
MC4324	-55°C	9.8	11.2	-1.6	5.0	5.0	4.5	5.5
	+25°C	9.8	11.2	-1.6	5.0	5.0	4.5	5.5
	+125°C	9.8	11.2	-1.6	5.0	5.0	4.5	5.5
MC4024	0°C	9.8	11.2	-1.6	5.0	5.0	4.75	5.25
	+25°C	9.8	11.2	-1.6	5.0	5.0	4.75	5.25
	+75°C	9.8	11.2	-1.6	5.0	5.0	4.75	5.25

TEST CURRENT/VOLTAGE VALUES

Characteristic	Symbol	Pin Under Test	MC4324 Test Limits						MC4024 Test Limits						Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:							
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C										
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		I_{OL1}	I_{OL2}	I_{OH}	V_{IH}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input Forward Current	I_{in}	2	–	100	–	100	–	100	–	100	–	100	–	100	µAdc	–	–	–	2	–	–	14	5,7,9
		12	–	100	–	100	–	100	–	100	–	100	–	100	µAdc	–	–	–	12	–	–	14	5,7,9
Output Output Voltage	V_{OL}	6	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	6	–	–	2	–	1,4,14	–	5,7,9
		8	–	↓	–	↓	–	↓	–	↓	–	↓	–	↓	↓	8	–	–	12	–	10,13,14	–	↓
		6	–		–		–		–		–		–			–	6	–	2	–	–	1,4,14	
		8	–		–		–		–		–		–			–	8	–	12	–	–	10,13,14	
	V_{OH}	6	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	6	2	–	1,3,14	–	5,7,9
		8	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	8	12	–	11,13,14	–	5,7,9
Short-Circuit Current	I_{SC}	6	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	2	1,3,14	–	–	5,6,7,9
		8	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	12	11,13,14	–	–	5,7,8,9
Power Requirements **(Total Device)** Power Supply Drain	I_{PD}	1,3,14	–	–	–	37	–	–	–	–	–	37	–	–	mAdc	–	–	–	2,4,10,12	1,13,14	–	–	5,7,9

AC TEST CIRCUIT AND WAVEFORMS





Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

AC TEST LIMITS

TEST	SYMBOL	CONDITIONS	LIMITS Min
Maximum Operating Frequency	f_{max}	$C_{control}$ = 10 pF, V_{in} = 5.0 Vdc Frequency Ratio = 3.5:1	25 MHz
Ratio of Frequency of Oscillation over Specified Input Voltage Range	$\frac{f_{high}}{f_{low}}$	$C_{control}$ = 100 pF, V_{in} high = 5.0 Vdc, V_{in} low = 1.0 Vdc	3.5:1.0

OPERATING CHARACTERISTICS

The operating frequency range of this multivibrator is controlled by the value of an external capacitor that is connected between X1 and X2. Either of the two equations shown below may be used to define the value of $C_{control}$:

$$C_{control} = \frac{500}{f_{max}}\ \mu F, \quad \text{or} \quad C_{control} = \frac{100}{f_{min}}\ \mu F,$$

with f given in Hz. The maximum operating frequency of this device is typically 30 MHz.

Three power supply and three ground connections are provided in this circuit. Each multivibrator has a separate power supply and ground connection. The output buffers have a common power supply and ground pin. This provides isolation between VCM's and minimizes the effect of output buffer transients on the multivibrators in critical applications. This separation of power supply and ground lines also provides the capability of disabling one VCM by disconnecting its V_{CC} pin. All grounds must always be connected to insure substrate grounding and proper isolation.

The output buffer transforms the logic levels of the VCM to MTTL logic levels.

FIGURE 1 – INPUT VOLTAGE versus OUTPUT FREQUENCY (15 pF FEEDBACK CAPACITOR)

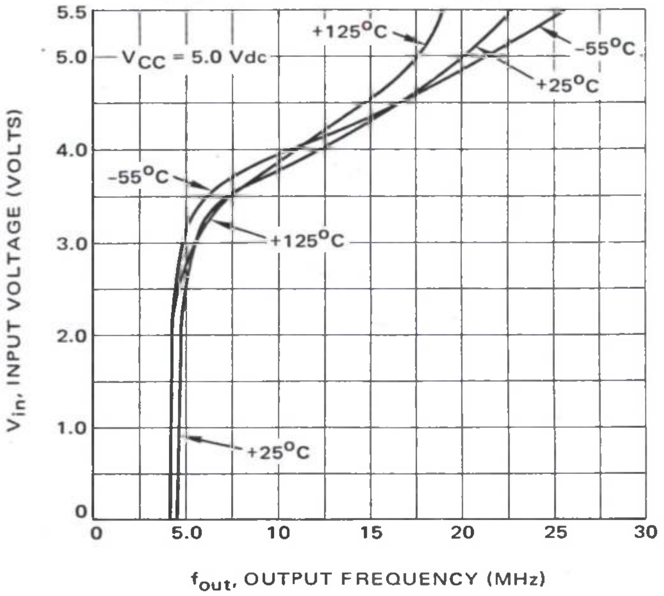


FIGURE 2 – INPUT VOLTAGE versus OUTPUT FREQUENCY (100 pF FEEDBACK CAPACITOR)

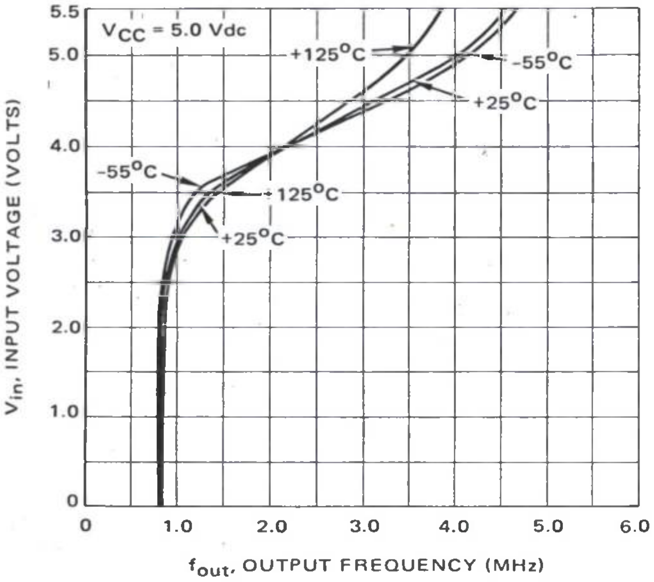
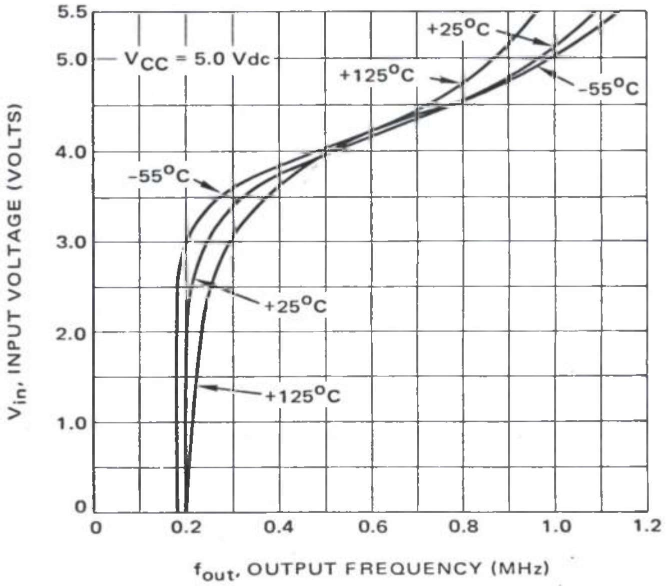


FIGURE 3 – INPUT VOLTAGE versus OUTPUT FREQUENCY (430 pF FEEDBACK CAPACITOR)



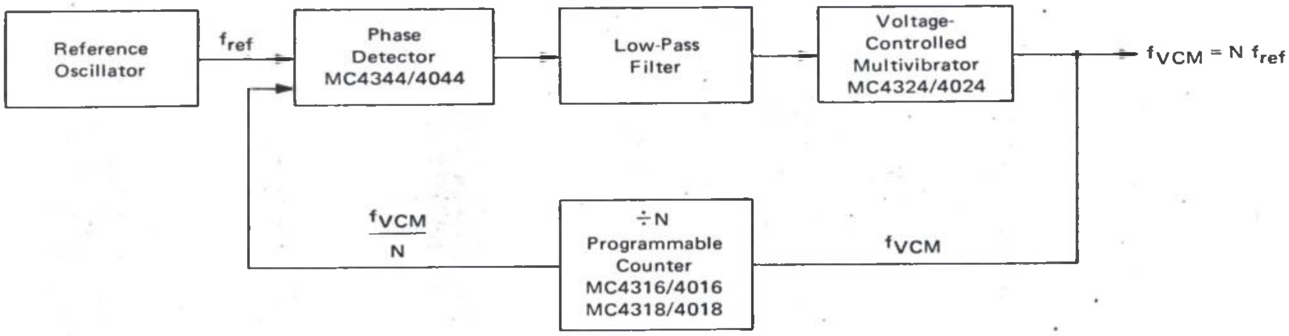
APPLICATIONS INFORMATION

The basic frequency synthesizer loop shown in Figure 4 consists of five basic components: the reference oscillator, the phase detector, the low-pass filter, the voltage controlled multivibrator/oscillator, and the divide by N counter.

This loop achieves a stable state when $f_{VCM} = N\ f_{ref}$. When this condition does not exist the VCM searches through its frequency spectrum until it finds the frequency at which the stable state occurs. At this point the loop locks. This system allows the generation of many discrete frequencies from a single, highly stable source (f_{ref}). A system such as this has many useful applications in communications (frequency control systems), computer systems (for synchronizing data tracks and clocking systems), in instruments (frequency synthesizers and counters) and filter networks.

In addition to its function in the phase-locked loop, the VCM may be used as a fixed oscillator (plug crystal into capacitor pins and ground control input), in simple A to D converter systems, and as an FM modulator.

FIGURE 4 – PHASE-LOCKED, FREQUENCY SYNTHESIZER LOOP


Reference Oscillator
fref
Phase Detector MC4344/4044
Low-Pass Filter
Voltage-Controlled Multivibrator MC4324/4024
fVCM = N fref
fVCM / N
÷N Programmable Counter MC4316/4016 MC4318/4018
fVCM

4211-46 PRINTED IN USA 10-71 IMPERIAL LITHO 825181 5M
DS 9108

HIGH-SPEED, DIFFERENTIAL COMPARATOR

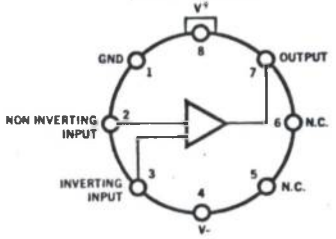
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA 710 is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar epitaxial process. The device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

ABSOLUTE MAXIMUM RATINGS

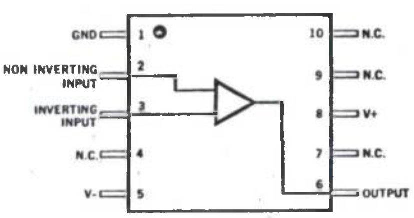
Positive Supply Voltage		+14.0 V
Negative Supply Voltage		-7.0 V
Peak Output Current		10 mA
Differential Input Voltage		±5.0 V
Input Voltage		±7.0 V
Internal Power Dissipation		
TO-5	(Note 1)	300 mW
Flat Package	(Note 2)	200 mW
Operating Temperature Range		-55°C to +125°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 60 sec.)		300°C

TO–5 CONNECTION DIAGRAM (TOP VIEW)

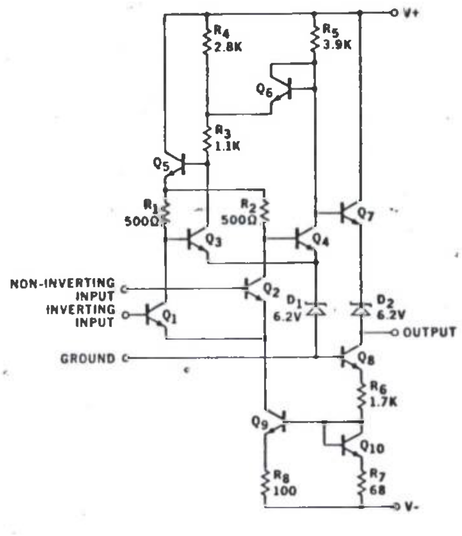


Note: Pin 4 connected to case

FLAT PACKAGE CONNECTION DIAGRAM (TOP VIEW)



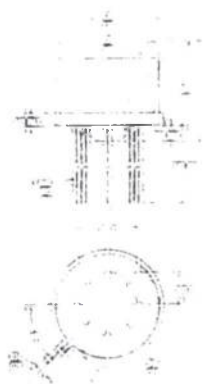
SCHEMATIC DIAGRAM



Notes on page 2

PHYSICAL DIMENSIONS

[illegible]



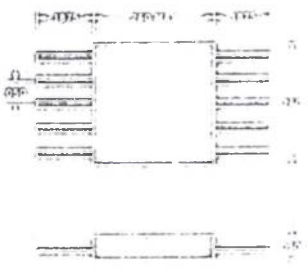
NOTES: [illegible]

ORDER PART NO

U5B771031X

PHYSICAL DIMENSIONS

(TYPICAL FLAT PACKAGE TOP VIEW)



ORDER PART NO

U3H771031X

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OTHER PATENTS PENDING

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12.0 V, V^- = -6.0 V unless otherwise specified)

Parameter (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$V_{out} = +1.4\text{ V}$, $R_S \leq 200\,\Omega$		2.0	5.0	mV
Input Offset Current	$V_{out} = +1.4\text{ V}$		1.0	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Output Resistance			200		Ω
Response Time (Note 3)			40		nsec
Input Voltage Range	$V^- = -7.0\text{ V}$	±5.0			V
Differential Input Voltage Range		±5.0			V
Positive Output Level	$V_{in} \geq 15\text{ mV}$, $0 \leq I_o \leq 0.5\text{ mA}$	+2.5	+3.2	+4.0	V
Negative Output Level	$V_{in} \geq 15\text{ mV}$	-1.0	-0.5	0	V
Output Sink Current	$V_{in} \geq 15\text{ mV}$, $V_{out} \geq 0$	1.6	2.5		mA
Positive Supply Current	$V_{out} \leq 0$		6.4		mA
Negative Supply Current			5.5		mA
Power Consumption					
TO-5 Package			110	175	mW
Flat Package			110	150	mW
The following specifications apply for $-55°\text{C} \leq T_A \leq +125°\text{C}$:					
Input Offset Voltage (Note 4)	$R_S \leq 200\,\Omega$			6.0	mV
Input Offset Current (Note 4)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage (Note 4)			5.0		μV/°C
Voltage Gain		500			

NOTES:

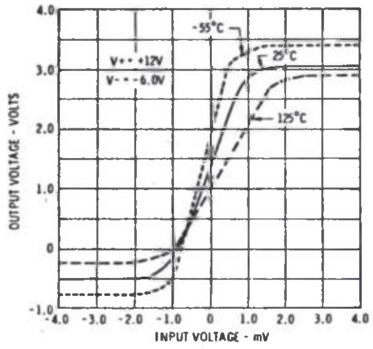
(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.

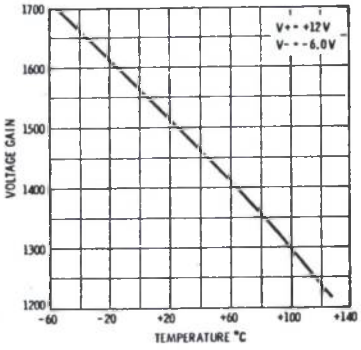
(2) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

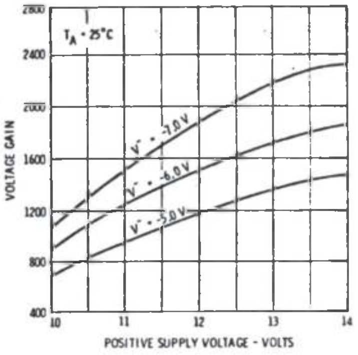
(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

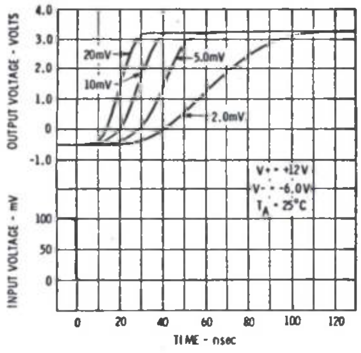
(4) The input offset voltage (see definitions) is specified for a logic threshold voltage of 1.8 V at -55°C, 1.4 V at +25°C and 1.0 V at +125°C.

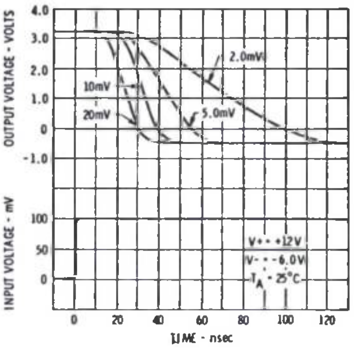
TYPICAL PERFORMANCE CURVES

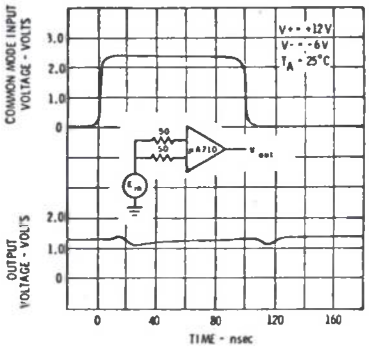

VOLTAGE TRANSFER CHARACTERISTIC

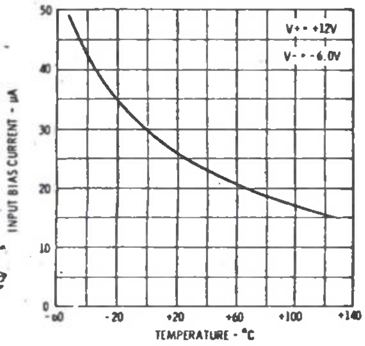

VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

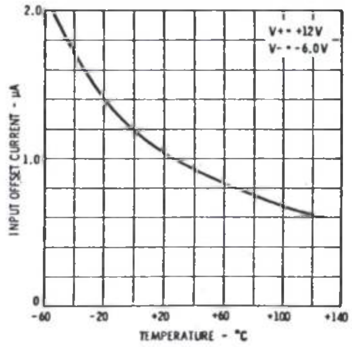

VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES

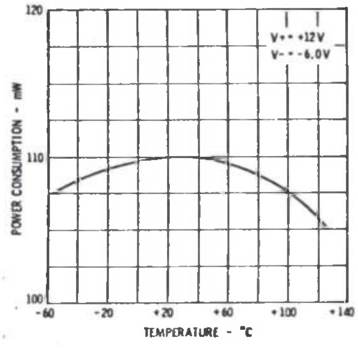

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES


COMMON MODE PULSE RESPONSE


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE


INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

DEFINITIONS

LOGIC THRESHOLD VOLTAGE - The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE - The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE - The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN - The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME - The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL - The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL - The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT - The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

DUAL COMPARATOR

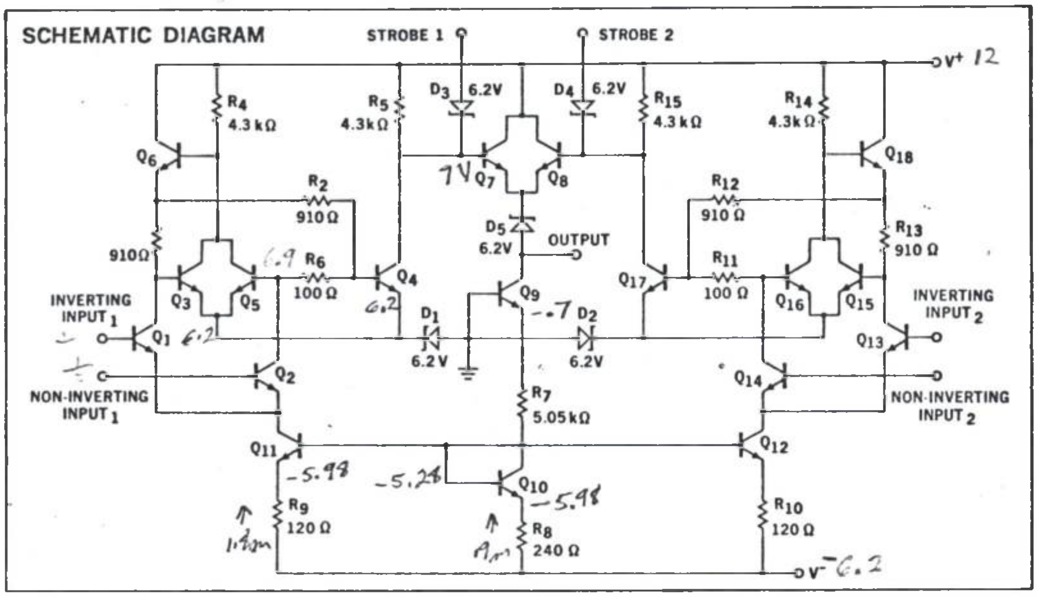
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The µA711 is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-go test equipment. The µA711, which is similar to the µA710 differential comparator, is constructed on a 40-mil square silicon chip using the Fairchild Planar* epitaxial process.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	-7.0 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Strobe Voltage	0 to +6.0 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

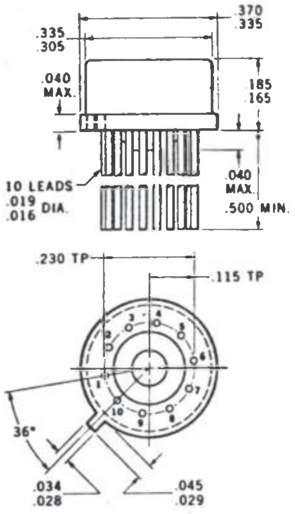
SCHEMATIC DIAGRAM



Notes on page 2

PHYSICAL DIMENSIONS

(In accordance with JEDEC TO–100)



NOTES: All dimensions in inches

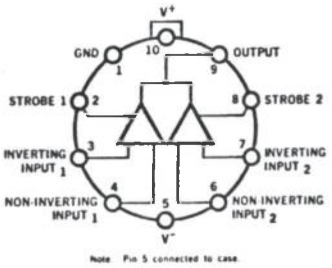
Leads are gold-plated kovar

Package weight is 1.32 grams

ORDER PART NO.

U5F771131X

TO-5 CONNECTION DIAGRAM (TOP VIEW)



Note: Pin 5 connected to case.

* Planar is a patented Fairchild process.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

SEMICONDUCTOR

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12.0 V, V^- = -6.0 V unless otherwise specified)

Parameter (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$V_{out} = +1.4$ V, $R_S \leq 200\,\Omega$, $V_{CM} = 0$		1.0	3.5	mV
	$V_{out} = +1.4$ V, $R_S \leq 200\,\Omega$		1.0	5.0	mV
Input Offset Current	$V_{out} = +1.4$ V		0.5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	$V^- = -7.0$ V	± 5.0			V
Differential Input Voltage Range		± 5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{in} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10$ mV, $I_O = 5$ mA	2.5	3.5		V
Negative Output Level	$V_{in} \geq 10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	-1.0		0	V
Output Sink Current	$V_{in} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	$V_{strobe} = 100$ mV		1.2	2.5	mA
Positive Supply Current	$V_{out} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	200	mW

The following specifications apply for -55°C $\leq T_A \leq$ +125°C:

Parameter (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage (Note 3)	$R_S \leq 200\,\Omega$, $V_{CM} = 0$			4.5	mV
	$R_S \leq 200\,\Omega$			6.0	mV
Input Offset Current (Note 3)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

NOTES:

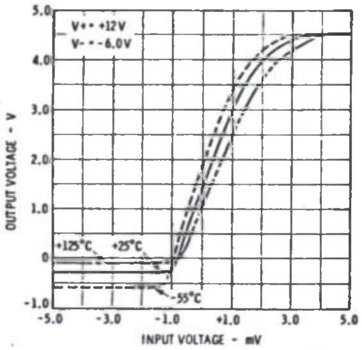
(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above 105°C.

(2) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

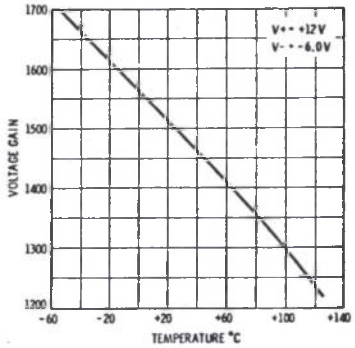
(3) The input offset voltage (see definitions) is specified for a logic threshold voltage of 1.8 V at -55°C, 1.4 V at +25°C and 1.0 V at +125°C.

TYPICAL PERFORMANCE CURVES

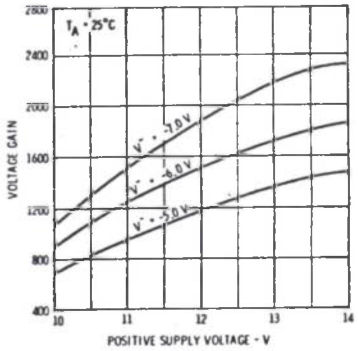
VOLTAGE TRANSFER CHARACTERISTIC



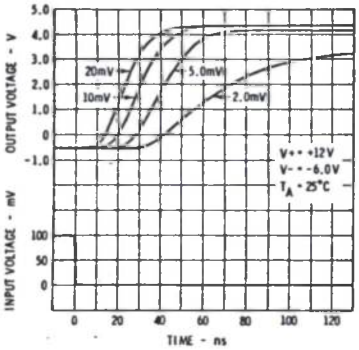
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



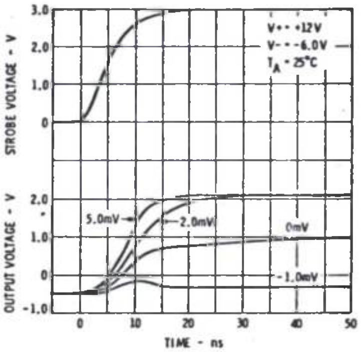
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



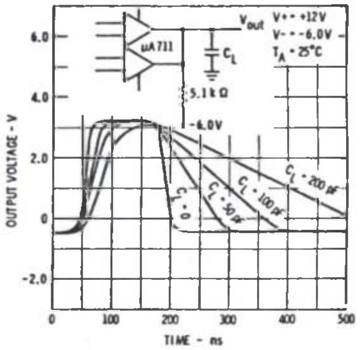
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



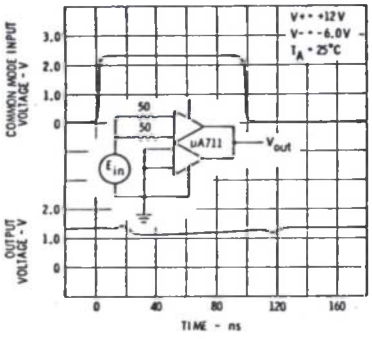
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



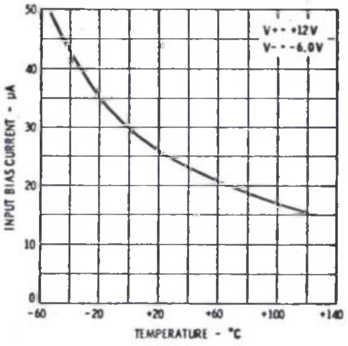
OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



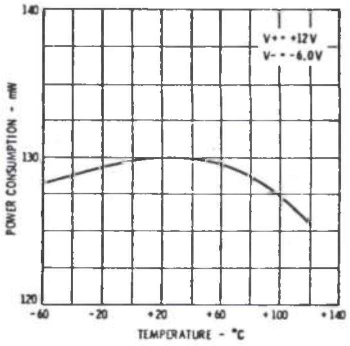
COMMON MODE PULSE RESPONSE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



DEFINITIONS

LOGIC THRESHOLD VOLTAGE - The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* - The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* - The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* - The average of the two input currents.

INPUT VOLTAGE RANGE* - The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* - The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* - The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* - The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* - The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* - The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* - The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT - The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* - The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* - The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT - The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

*These definitions apply for either side with the other disabled with the strobe.

Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product. No other circuit patent licenses are implied

Am2602/9602

Dual Retriggerable Resettable Monostable Multivibrator

Advanced Micro Devices
Complex Digital Integrated Circuits

Description: The 9602 Dual Monostable Multivibrator is functionally, electrically and pin for pin an equivalent to the Fairchild 9602. It is available in the Silicone Plastic and Hermetic Dual In-Line Package. The Am2602 is a pin for pin replacement for the 9602 with improved switching characteristics and a guaranteed pulse width change of less than 0.6% over the temperature range 0°C to +75°C.

Distinctive Characteristics: 100% Reliability Assurance Testing including high temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL STD 883.

Mixing privileges for obtaining price discounts. Refer to price list.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am 2602 and 9602 are dual DC level sensitive resettable retriggerable monostable multivibrators which provide an output pulse whose duration and accuracy depend on external timing components.

Provision is made for triggering on the rising or falling edge of an input signal. All inputs are DC coupled making triggering independent of input rise and fall times. Each time the output from the OR trigger gate goes from a FALSE (LOW) to TRUE (HIGH) condition triggering occurs independent of the state of the monostable.

The direct clear facility allows a timing cycle to be terminated at any time during the cycle. A LOW signal on the $\overline{C}_D$ input resets the monostable independent of other conditions.

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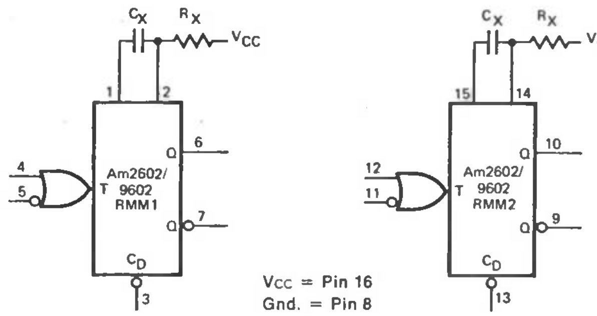
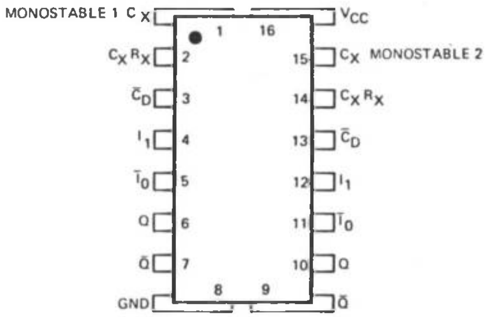
LOGIC DIAGRAM



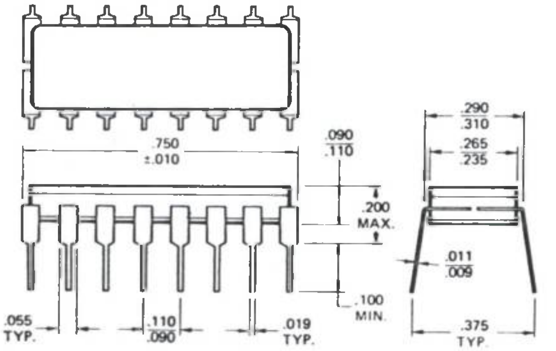
V_{CC} = Pin 16
Gnd. = Pin 8

CONNECTION DIAGRAM
Top View

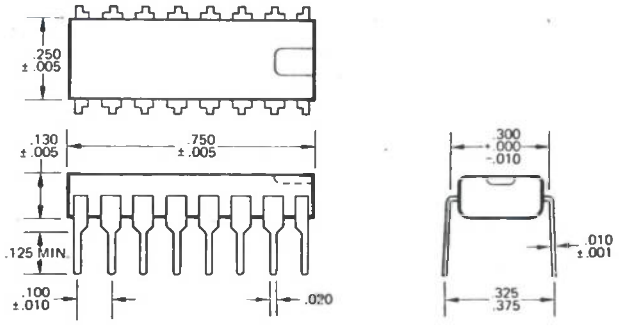


PHYSICAL DIMENSIONS
Dual In-Line

Hermetic



Silicone Plastic



NOTES: (1) All dimensions in inches.
(2) Leads are intended for insertion in hole rows on .300″ centers and are misaligned (.375) to facilitate insertion.
(3) Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to $+V_{CC}$ max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	Note 1

ELECTRICAL CHARACTERISTICS

AM2602BDEA/U7B960259X $T_A = 0°C$ to $+75°C$
AM2602AAEA/U7B960251X $T_A = -55°C$ to $+125°C$ (Note 2)

DC Characteristics (Notes 3, 4)

Parameters	Part No.	Test Conditions	−55°C Min	−55°C Max	0°C Min	0°C Max	LIMITS +25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	+125°C Min	+125°C Max	Units
V_{OH} Output HIGH Voltage	AM2602AAEA U7B960251X	$V_{CCL} = 4.5$ V, $I_{OH} = 16xI_R = -0.96$ mA	2.40				2.40	3.6				2.40		Volts
	AM2602BDEA U7B960259X	$V_{CCL} = 4.75$ V, $I_{OH} = 16xI_R = -0.96$ mA			2.40		2.40	3.8		2.40				
V_{OL} Output LOW Voltage	AM2602AAEA U7B960251X	$V_{CCH} = 5.5$ V, $I_{OL} = 8xI_F = 12.8$ mA $V_{CCL} = 4.5$ V, $I_{OL} = 8xI_F = 9.92$ mA		0.40				0.2	0.40				0.40	Volts
	AM2602BDEA U7B960259X	$V_{CCH} = 5.25$ V, $I_{OL} = 8xI_F = 12.8$ mA $V_{CCL} = 4.75$ V, $I_{OL} = 8xI_F = 11.3$ mA				0.45		0.2	0.45		0.45			
V_{IH} Input HIGH Voltage	AM2602AAEA U7B960251X	$V_{CCH} = 5.5$ V $V_{CCL} = 4.5$ V	2.00				1.70					1.40		Volts
	AM2602BDEA U7B960259X	$V_{CCH} = 5.25$ V $V_{CCL} = 4.75$ V			1.90		1.80			1.60				
V_{IL} Input LOW Voltage	AM2602AAEA U7B960251X	$V_{CCH} = 5.5$ V $V_{CCL} = 4.5$ V		0.80					0.90				0.80	Volts
	AM2602BDEA U7B960259X	$V_{CCH} = 5.25$ V $V_{CCL} = 4.75$ V				0.85			0.85		0.85			
[illegible] Input Load Current	AM2602AAEA U7B960251X	$V_{CCH} = 5.5$ V $V_F = 0.4$ V $V_{CCL} = 4.5$ V		−1.60 −1.24				−1.10 −0.97	−1.60 −1.24				−1.60 −1.24	mA
	AM2602BDEA U7B960259X	$V_{CCH} = 5.25$ V $V_F = 0.45$ V $V_{CCL} = 4.75$ V				−1.60 −1.41		−1.00 −0.90	−1.60 −1.41		−1.60 −1.41			
I_R Reverse Input Current	AM2602AAEA U7B960251X	$V_{CCH} = 5.5$ V, $V_R = 4.5$ V		60				15	60				60	μA
	AM2602BDEA U7B960259X	$V_{CCH} = 5.25$ V, $V_R = 4.5$ V				60		15	60		60			
I_{SC} Short Circuit Current	AM2602AAEA U7B960251X	$V_{CC} = 5.0$ V, $V_o = 1.0$ V					−8		−50					mA
	AM2602BDEA U7B960259X	$V_{CC} = 5.0$ V, $V_o = 1.0$ V					−8		−50					
I_{PD} Power Supply Current	AM2602AAEA U7B960251X	$V_{CC} = 5.5$ V GND Pins 5 and 11 $R_X = 10k\Omega$		56				35	56				56	mA
	AM2602BDEA U7B960259X	$V_{CC} = 5.25$ V GND Pins 5 and 11 $R_X = 10k\Omega$				56		35	56		56			

Switching Characteristics

Parameters		Test Conditions	Am2602 +25°C Min	Am2602 +25°C Typ	Am2602 +25°C Max	9602 +25°C Min	9602 +25°C Typ	9602 +25°C Max	Units
t_{pd+}	Turn Off Delay Negative Trigger Input to True Output	$V_{CC} = 5.0$ V, $C_L = 15$ pF $R_X = 5k\Omega$, $C_X = 0$ pF		25	40		27	45	ns
t_{pd-}	Turn On Delay Negative Trigger Input to False Output			25	40		27	40	ns
t_{pw}(min)	Minimum True Output Pulse Width			45	65		50	70	ns
t_{pw}	Pulse Width	$V_{CC} = 5.0$ V, $C_L = 15$ pF $R_X = 10k\Omega$, $C_X = 1000$ pF	3.08	3.42	3.76	3.08	3.42	3.76	μs
R_X	Timing Resistor over temperature range (Note 5)		5		50	5		50	kΩ

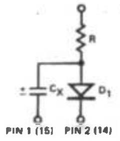
	Am2602		Min	Typ	Max	
$\Delta t_{pw}(T)$	Maximum change in Pulse Width True Output over temperature range 0°C to +75°C	$V_{CC} = 5.0$ V, $C_L = 15$ pF $R_X = 10k\Omega$, $C_X = 1000$ pF		0.3	0.6	%

Note 1. Maximum current defined by DC Input Voltage.
2. Electrical Characteristics for the Silicone Plastic DIP suffixed EB or prefixed U6M are identical to the Hermetic DIP suffixed EA or prefixed U7B.
3. Pulse tested.
4. Tests are conducted with a 10kΩ resistor placed between Pin 2 (14) and Vcc unless otherwise noted.
5. Maximum permissible Rx when used below 0°C is 25kΩ.

OPERATION RULES

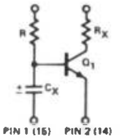
1. An external resistor R_X and an external capacitor C_X are required as shown in the logic diagram. The values of R_X may vary from 5.0 kΩ to 50 kΩ for AM 2602 BDEA/U7B960259X and 5.0 kΩ to 25 kΩ for AM 2602 AAEA/U7B960251X. C_X may vary from 0 to any value necessary and obtainable.
2. If a fixed value of R_X is used, the following values are recommended: $R_X = 30$ kΩ for AM 2602 BDEA/U7B960259X; $R_X = 10$ kΩ for AM 2602 AAEA/U7B960251X.
3. The output pulse width T is defined as follows:

   $T = 0.32\ R_X C_X\ [1 + \frac{0.7}{R_X}]$ (For C_X greater than 10^3 pF) Where: R_X is in kΩ, C_X is in pF, T is in ns. For $C_X < 10^3$ pF see Fig. 2.
4. If electrolytic type capacitors are to be used, the following two arrangements are recommended:



$R < 0.6\ R_X$ (Max)

D_1: any silicon type diode, such as FD700



This circuit also allows larger value of R to be used for longer output pulse width.

$R < R_X\ (0.7)\ (h_{FE}Q_1)$

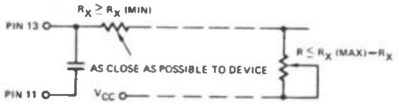
$R_X\ (\text{min}) < R_X < R_X\ (\text{max})$

Q_1: Any NPN silicon device with sufficient h_{FE} at low currents, such as 2N2511

Both circuits prevent reverse voltage across C_X. The pulse width T for the circuits is defined as follows:

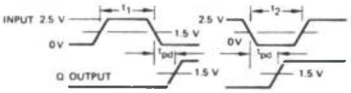
$T \approx 0.36\ RC_X\ [1 + \frac{0.7}{R}]$ Where: R is in kΩ, C_X is in pF, T is in ns.

5. To obtain variable pulse width, by remote trimming, the following circuit is recommended:

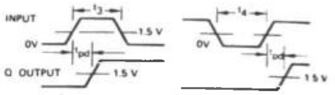


6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules. $t_1, t_2, t_3, t_4 > 40$ ns

Input to Pin 5 (11)
Pin 4 (12) = LOW
Pin 3 (13) = HIGH



Input to Pin 4 (12)
Pin 5 (11) = HIGH
Pin 3 (13) = HIGH



8. The retriggerable pulse width is calculated as shown below:

   $t_w = t_{pw} + t_{pd+} = 0.32\ R_X C_X\ (1 + \frac{0.7}{R_X}) + t_{pd+}$

   The retrigger pulse width is equal to the pulse width t_{pw} plus a delay time. For pulse widths greater than 500 ns, t_w can be approximated as t_{pw}.

   NOTE: Retriggering will not occur if the retrigger pulse comes within $.32\ R_X C_X\ (\frac{0.7}{R_X})$ ns after the initial trigger pulse.
9. Reset Operation — The Am 2600/9600 have an active LOW reset facility. By applying a low to the reset input, any timing cycle can be terminated or any new cycle inhibited until the low reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held low.

DEFINITION OF TERMS

SUBSCRIPT TERMS:

F Forward, applying to LOW inputs.

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

R Reverse, applying to HIGH inputs.

OPERATIONAL TERMS:

I_F Forward input load current, for unit input load.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_R Reverse input load current with V_R applied to input.

Negative Current Current flowing out of the device.

P_{DISS} The power dissipated within the circuit with input and output terminals open.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to figure 4.

V_{IL} Maximum logic LOW input voltage. Refer to figure 4.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

V_F Forward LOW input voltage, for forward input current (I_F) test.

V_R Input reverse HIGH voltage applied for input leakage current, (I_R) test.

FUNCTIONAL TERMS:

$\overline{C}_D$ The asynchronous direct clear input. A LOW on this input resets the monostable independent of other conditions.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

$\overline{I}_0$ The active LOW input of the monostables. With input I_1 LOW a HIGH to LOW transition on $\overline{I}_0$ will cause triggering.

I_1 The active HIGH input of the monostables. With $\overline{I}_0$ HIGH a LOW to HIGH transition on I_1 will cause triggering.

Input Unit Load One T²L gate input load. In the HIGH state it is equal to I_R and in the LOW state it is equal to I_F.

Q The TRUE output of the monostables.

$\overline{Q}$ The FALSE output of the monostables.

Triggering The switching of the monostable from the stable state to the unstable state and start of the timing cycle.

SWITCHING TERMS:

t_{pd+} The propagation delay from a HIGH to LOW transition on $\overline{I}_0$ to the true (Q) output LOW to HIGH transition.

t_{pd-} The propagation delay from a HIGH to LOW transition on $\overline{I}_0$ to the false ($\overline{Q}$) output HIGH to LOW transition.

t_{pw}(min) The minimum true (Q) output pulse width with $R_X = 5$kΩ, $C_X = 0$ pF.

t_{pw} The pulse width obtained with $R_X = 10$kΩ, $C_X = 1000$ pF.

Δt_{pw}(T) The maximum percentage change in pulse width of the true (Q) output for the Am2602 over the temperature range 0°C to +75°C.

Am 2602 Normalized Output Pulse Width Versus Ambient Temperature

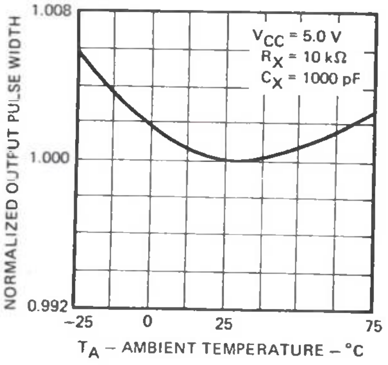


Figure 1

Output Pulse Width Versus Timing Resistance and Capacitance

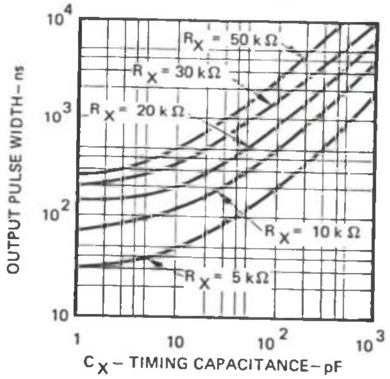
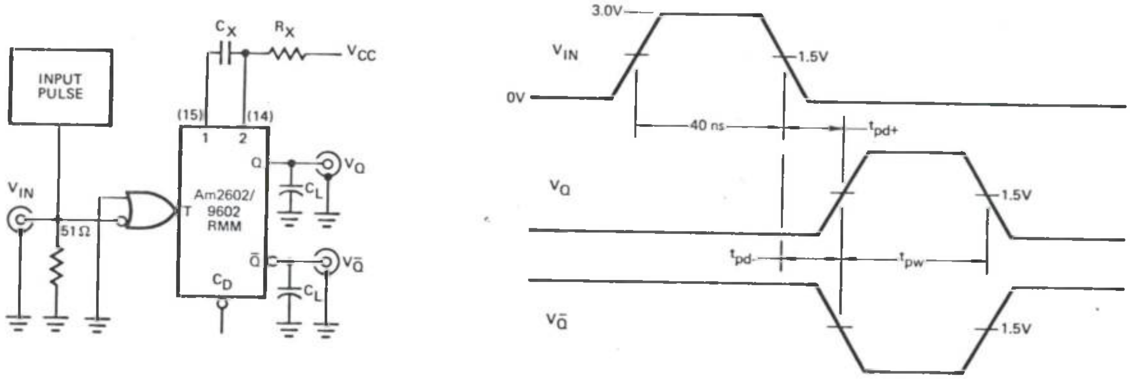


Figure 2

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



V_{CC} = Pin 16
Gnd. = Pin 8

INPUT PULSE
f ≃ 100 kHz
Amp ≃ 3.0 V
Width ≃ 40 ns
$t_r = t_f \leq 10$ ns

Figure 3

1. An extern
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2. If a fixe
   AM 260
3. The o
   T =
4. If e

TH TABLE

602/9602
ch Monostable

	$\overline{C}_D$	Operation
L	H	Trigger
L→H	H	Trigger
X	L	Reset

= HIGH Voltage Level
= LOW Voltage Level
X = Don't Care
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

Table I

Am2602/9602 LOADING RULES

Monostable 1	C_X	1	—	—	—
	$C_X\,R_X$	2	—	—	—
	$\overline{C}_D$	3	1	—	—
	I_1	4	1	—	—
	$\overline{I}_0$	5	1	—	—
	Q	6	—	16	8
	$\overline{Q}$	7	—	16	8
	GND	8	—	—	—
Monostable 2	$\overline{Q}$	9	—	16	8
	Q	10	—	16	8
	$\overline{I}_0$	11	1	—	—
	I_1	12	1	—	—
	$\overline{C}_D$	13	1	—	—
	$C_X\,R_X$	14	—	—	—
	C_X	15	—	—	—
	V_{CC}	16	—	—	—

Table II

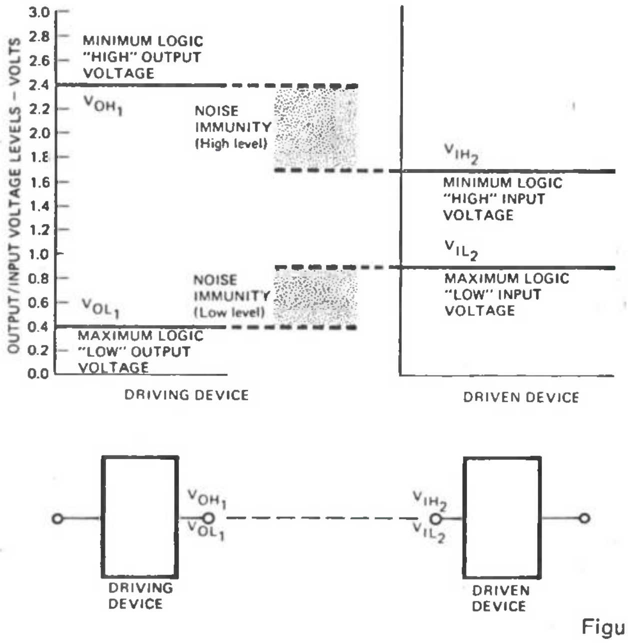
MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table III

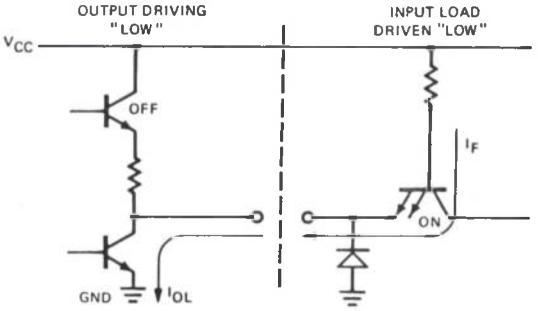
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



OUTPUT/INPUT VOLTAGE LEVELS – VOLTS
3.0
2.8
2.6
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
MINIMUM LOGIC "HIGH" OUTPUT VOLTAGE
V_{OH_1}
NOISE IMMUNITY (High level)
V_{IH_2}
MINIMUM LOGIC "HIGH" INPUT VOLTAGE
V_{IL_2}
MAXIMUM LOGIC "LOW" INPUT VOLTAGE
NOISE IMMUNITY (Low level)
V_{OL_1}
MAXIMUM LOGIC "LOW" OUTPUT VOLTAGE
DRIVING DEVICE
DRIVEN DEVICE
V_{OH_1}
V_{OL_1}
V_{IH_2}
V_{IL_2}
DRIVING DEVICE
DRIVEN DEVICE

Current Interface Conditions — LOW



Current Interface Conditions — HIGH

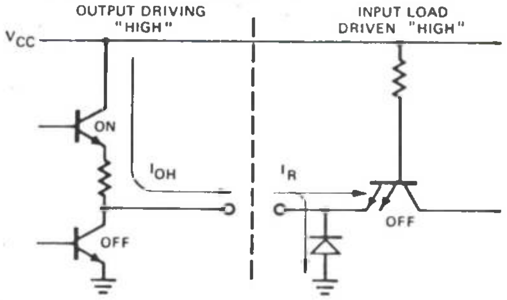
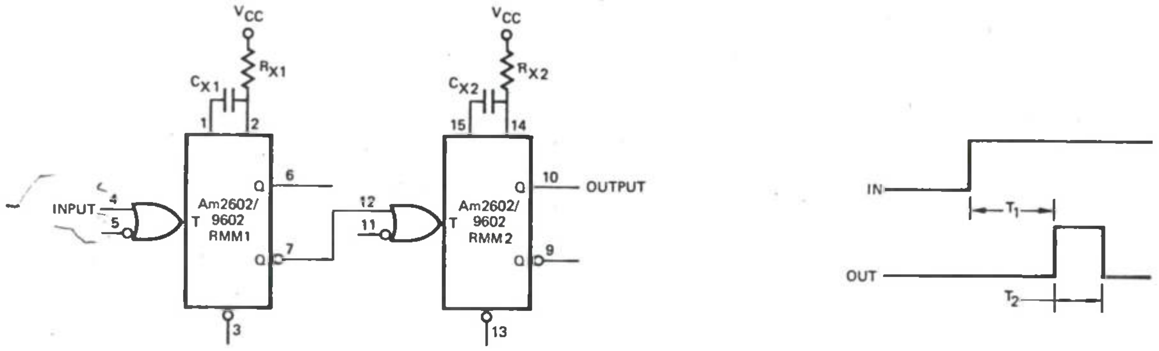


Figure 4

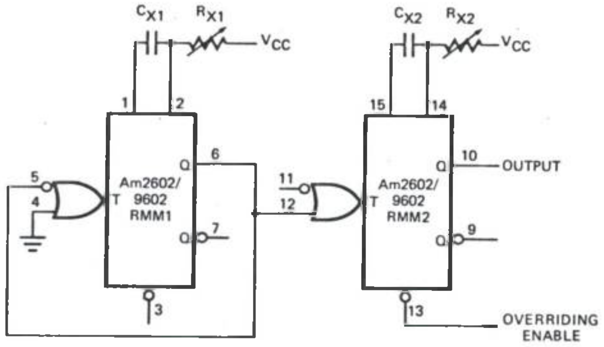
Am2602/9602 APPLICATIONS



Delayed Pulse Generation

The first monostable determines the time T_1 before the initiation of the output pulse. The second monostable determines T_2, the output pulse width.

Figure 5



Pulse Generator

The output frequency produced with the above configuration is determined by C_{X1} and R_{X1}, while the pulse width is determined by C_{X2} and R_{X2}. Monostable 1 forms an astable multivibrator with an output pulse width of approximately 25 ns, while monostable 2 extends the pulse width to the required value.

Figure 6

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am2602	Silicone Plastic DIP	0°C to +75°C	AM2602BDEB
Am2602	Hermetic DIP	0°C to +75°C	AM2602BDEA
[illegible]2602	Hermetic DIP	−55°C to +125°C	AM2602AAEA
[illegible]602	Dice	Note 6	AM2602XXXD
[illegible]602	Silicone Plastic DIP	0°C to +75°C	U6M960259X
9602	Hermetic DIP	0°C to +75°C	U7B960259X
9602	Hermetic DIP	−55°C to +125°C	U7B960251X
9602	Dice	Note 6	UXX9602XXD

Note 6: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

ADVANCED
MICRO
DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280

STEWART-WARNER COMPANIES
SYMBOL OF SW EXCELLENCE
STEWART-WARNER MICROCIRCUITS, INC.
730 EAST EVELYN AVENUE
SUNNYVALE, CALIFORNIA 94086

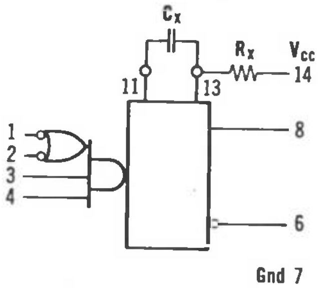
RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

TTL
SW9601

SEPTEMBER 1969

The SW9601 is a TTL Monostable Multivibrator with versatile trigger gating, rapid recovery, internally compensated reference levels, and high speed capability. It is well suited for a broad variety of applications, including pulse delay generators, square wave generators, long delay timers, pulse absence detectors, and clock pulse generators.

LOGIC SYMBOL



FEATURES

- **RETRIGGERABLE,** 0 to 100% duty cycle.
- **D. C. LEVEL TRIGGERING,** insensitive to transition times.
- **COMPLEMENTARY INPUTS,** for "leading edge" or "trailing edge" triggering.
- **COMPLEMENTARY OUTPUTS,** with active pull-ups for driving load capacitance.
- **PULSE WIDTH COMPENSATION** for Vcc and temperature variations.
- **50 nsec TO ∞ OUTPUT PULSE WIDTH RANGE.**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY.**

OPERATING NOTES

1. TRIGGERING — The SW9601 has four D.C. coupled triggering inputs; pins 1 and 2 respond to LOW state signals, while pins 3 and 4 respond to HIGH state signals. Triggering occurs as the input signal passes through the threshold region. Triggering logic is outlined in the Table. Input signals can be interchanged between pins 1 and 2, since they are logically identical; the same relationship holds for pins 3 and 4.

Pin 1	Pin 2	Pin 3	Pin 4	RESPONSE
HIGH	HIGH	↑	ϕ	NO TRIGGER
LOW	ϕ	↑	HIGH	TRIGGERS
LOW	ϕ	↑	LOW	NO TRIGGER
↓	HIGH	HIGH	HIGH	TRIGGERS
↓	HIGH	LOW	ϕ	NO TRIGGER
↓	LOW	ϕ	ϕ	NO TRIGGER

ϕ = immaterial

2. RETRIGGERING — In a normal cycle, triggering initiates a rapid discharge of the external timing capacitor, followed by a ramp voltage run-up at pin 13. The delay will time out when the ramp voltage reaches the upper trigger point of a Schmitt circuit, causing the outputs to revert to the quiescent state. If another trigger occurs before the ramp voltage reaches the Schmitt threshold, the capacitor will be discharged and the ramp will start again without having disturbed the outputs. The delay period can therefore be extended for an arbitrary length of time by insuring that the interval between triggers is less than the delay time, as determined by the external capacitor and resistor.

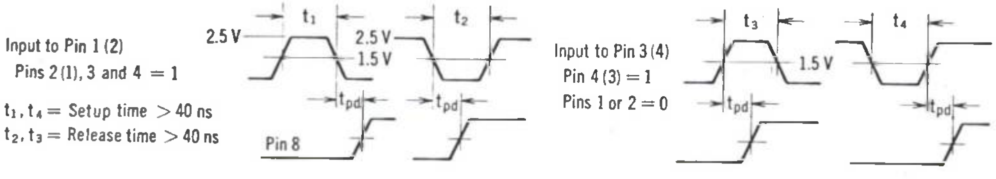
3. NON-RETRIGGERABLE OPERATION — Retriggering can be inhibited logically, by connecting pin 6 back to pin 3 or 4, or by connecting pin 8 back to **both** pins 1 and 2.

4. OUTPUT PULSE WIDTH — An external resistor R_X and an external capacitor C_X are required, as shown in the logic diagram; to minimize stray capacitance and noise pickup, R_X and C_X should be located as close as possible to the circuit. In applications which require remote trimming of the pulse width, as with a variable resistor, R_X should consist of a fixed resistor in series with the variable resistor; the fixed resistor should be located as close as possible to the circuit.
The output pulse width T is defined as follows, where R_X is in KΩ, C_X is in pf and T is in nanoseconds.

$$T = 0.32\,R_X C_X \left(1 + \frac{0.7}{R_X}\right) \qquad (\text{for } C_X > 10^3 \text{ pf})$$

The values of R_X may vary from 5.0KΩ to 50KΩ for 0° to +75°C operation, and 5.0KΩ to 25KΩ for −55° to +125°C operation. C_X may vary from 0 to any value.

5. SETUP AND RELEASE TIMES



t_1, t_4 = Setup time > 40 ns
t_2, t_3 = Release time > 40 ns

MAXIMUM RATINGS (beyond which device life may be impaired)

Vcc Pin Potential to Ground*	−0.5V to +8.0V
Input Voltage (D.C.)	−0.5V to +5.5V
Input Current	−30 mA to +5.0 mA
Voltage Applied to Output when Output is High	0V to +Vcc value
Current Into Output when Output is Low	50 mA

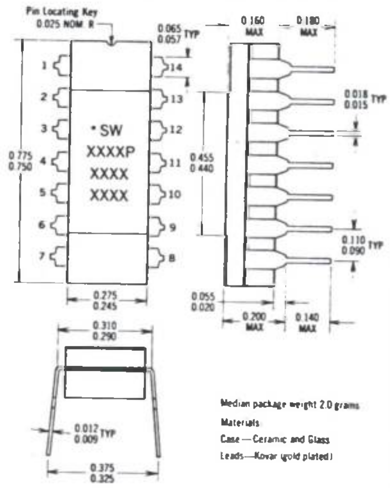
Operating Temperature Range (Military-1)	−55°C to +125°C
Operating Temperature Range (Industrial-2)	0°C to +75°C
Storage Temperature	−65°C to +150°C

---

* In a system, Vcc should not exceed 7.0 volts, in order to limit the reverse current forced into the input of a driven load.

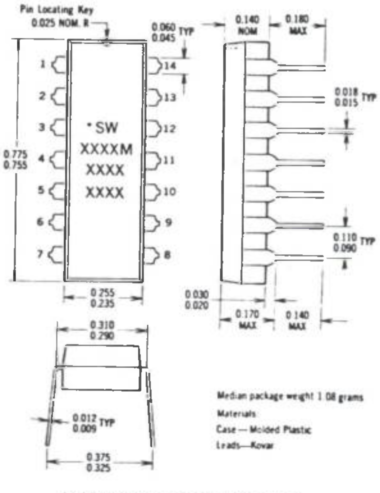
PACKAGE DIMENSIONS
(IN INCHES)

14 LEAD CERAMIC DUAL IN LINE PLUG-IN "P"



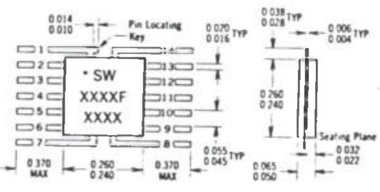
Median package weight 2.0 grams
Materials
Case — Ceramic and Glass
Leads — Kovar (gold plated)

14 LEAD PLASTIC DUAL IN LINE PLUG-IN "M"



Median package weight 1.08 grams
Materials
Case — Molded Plastic
Leads — Kovar

14 LEAD .250 × .250 FLAT PACK "F"



Median package weight 0.40 gram
Materials: Case — Ceramic and Glass, Leads — Kovar (gold plated)

Printed in U.S.A.

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5\ V \pm 10\%$)

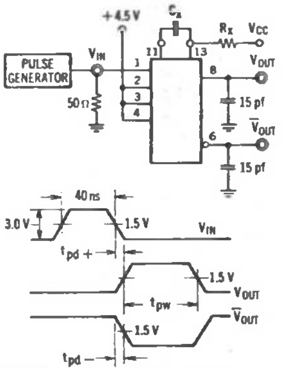
CHARACTERISTIC	SYMBOL	CONDITIONS ①	−55°C		+25°C			+125°C		UNIT
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
Output High Voltage	V_{OH}	$V_{CC} = 4.5\ V$; $I_{OH} = -1.0\ mA$ ②	2.4		2.4	3.3		2.4		V
Output Low Voltage	V_{OL}	$V_{CC} = 4.5\ V$; $I_{OL} = 10\ mA$ ②		0.4		0.2	0.4		0.4	V
Input High Voltage	V_{IH}	$V_{CC} = 4.5\ V$ ③	2.0		1.7			1.4		V
Input Low Voltage	V_{IL}	$V_{CC} = 5.5\ V$ ③		0.85			0.90		0.85	V
Input Load Current	I_F	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$		−1.6		−1.1	−1.6		−1.6	mA
Input Leakage Current	I_R	$V_{CC} = 5.5\ V$; $V_R = 4.5\ V$				15	60		60	μA
Short Circuit Current	I_{SC}	$V_{CC} = 5.0\ V$; $V_{OUT} = 0\ V$ ②			−10		−40			mA
Quiescent Power Supply Drain	I_{pd}	$V_{CC} = 5.5\ V$; Ground pins 1 and 2		24			24		24	mA
Max. Allowable Wiring Cap. (Pin 13)	C_{STRAY}	Pin 13 to Ground		50			50		50	pf
Timing Resistor	R_X		5	25	5		25	5	25	KΩ

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5\ V \pm 5\%$)

CHARACTERISTIC	SYMBOL	CONDITIONS ①	0°C		+25°C			+75°C		UNIT
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
Output High Voltage	V_{OH}	$V_{CC} = 4.75\ V$; $I_{OH} = -1.0\ mA$ ②	2.4		2.4	3.4		2.4		V
Output Low Voltage	V_{OL}	$V_{CC} = 4.75\ V$; $I_{OL} = 12.8\ mA$ ②		0.45		0.2	0.45		0.45	V
Input High Voltage	V_{IH}	$V_{CC} = 4.75\ V$ ③	1.9		1.8			1.6		V
Input Low Voltage	V_{IL}	$V_{CC} = 5.25\ V$ ③		0.85			0.85		0.85	V
Input Load Current	I_F	$V_{CC} = 5.25\ V$; $V_F = 0.45\ V$		−1.6		−1.0	−1.6		−1.6	mA
Input Leakage Current	I_R	$V_{CC} = 5.25\ V$; $V_R = 4.5\ V$				15	60		60	μA
Short Circuit Current	I_{SC}	$V_{CC} = 5.0\ V$; $V_{OUT} = 0\ V$ ②			−10		−40			mA
Quiescent Power Supply Drain	I_{pd}	$V_{CC} = 5.25\ V$; Ground pins 1 and 2		24			24		24	mA
Max. Allowable Wiring Cap. (Pin 13)	C_{STRAY}	Pin 13 to Ground		50			50		50	pf
Timing Resistor	R_X		5	50	5		50	5	50	KΩ

NOTES: ① Unless otherwise noted, 10KΩ resistor placed between Pin 13 and V_{CC}, for all tests. (R_X).
② Ground Pin 11 for V_{OL} @ Pin 6 or V_{OH} @ Pin 8 or I_{SC} @ Pin 8. Open Pin 11 for V_{OL} @ Pin 8 or V_{OH} @ Pin 6 or I_{SC} @ Pin 6.
③ Pulse test to determine V_{IH} and V_{IL} (minimum P.W. 40 ns).

DYNAMIC TEST SPECIFICATIONS

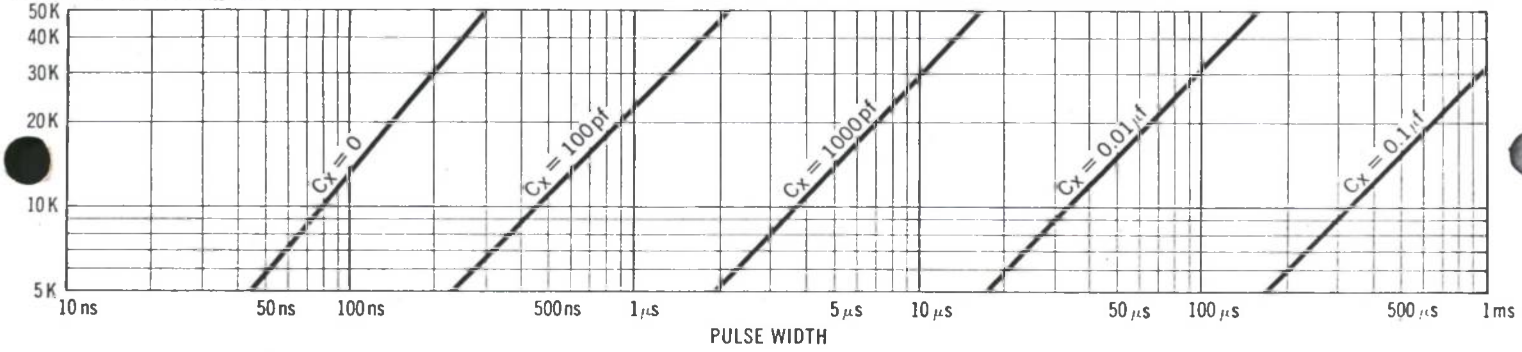


NOTE: Capacitance includes probe and jig.

$V_{CC} = 5\ V$, $T_A = +25°C$

CHARACTERISTIC	SYMBOL	LIMITS		UNIT	R_X KΩ	C_X pf
		MIN	MAX			
Negative Trigger Input to True Output	$t_{pd}+$		40	ns	5.0	0
Negative Trigger Input to Complement Output	$t_{pd}-$		30	ns	5.0	0
Minimum True Output Pulse Width	t_{pw}(min)		60	ns	5.0	0
Pulse Width Variation	Δt_{pw}	3.08	3.76	ns	10	1000

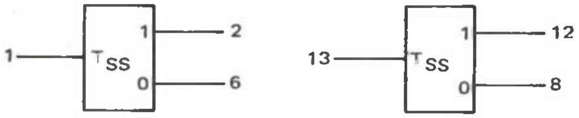
PULSE WIDTH VS. R_X AND C_X



DUAL MONOSTABLE MULTIVIBRATOR

MC667

NOVEMBER 1970



Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 240 mW typ

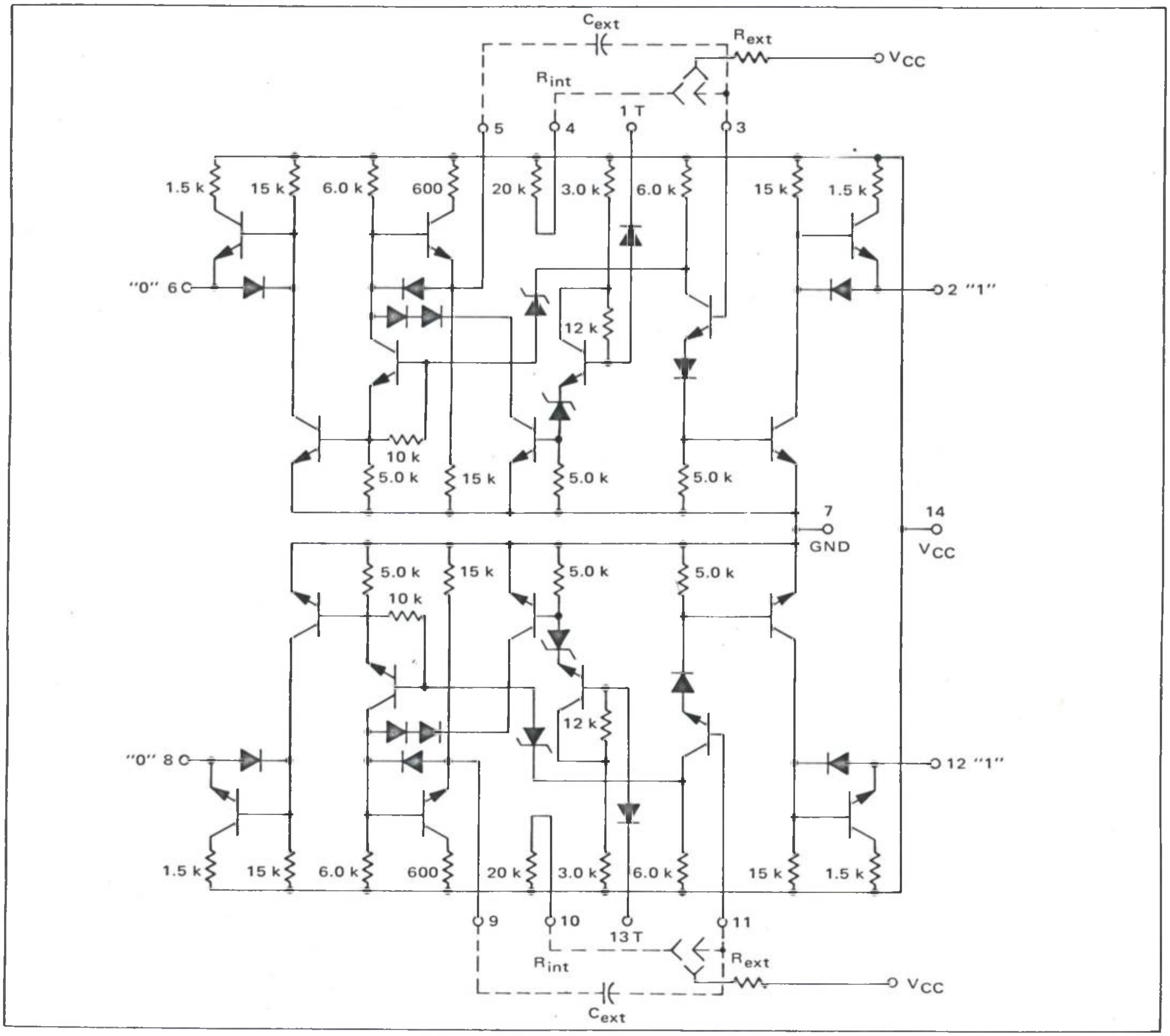
An internal timing resistor is provided at pin 4(10).

An external timing resistor may be connected between V_{CC} and pin 3(11) instead of using pin 4(10).

A timing capacitor is connected between pins 3(11) and 5(9). (See circuit schematic.)

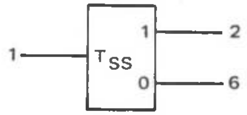
The MC667 is a dual monostable multivibrator whose output pulse width is independent of input pulse width. The device is triggered on the rising edge of a pulse to the toggle input, and the output pulse width is determined by the R-C timing network. Circuit operation is described on Page 7 of Application Note 467.

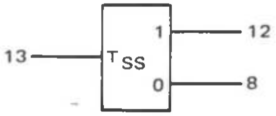
Each multivibrator in the package has both true logic "1" and complement logic "0" outputs available. A positive-going pulse is available at the logic "1" output, and the inverted pulse is available at the logic "0" output. Outputs utilize active pullup circuits to minimize output impedance.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one monostable multivibrator. The other monostable multivibrator is tested in the same manner.

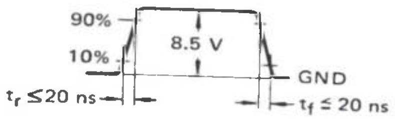




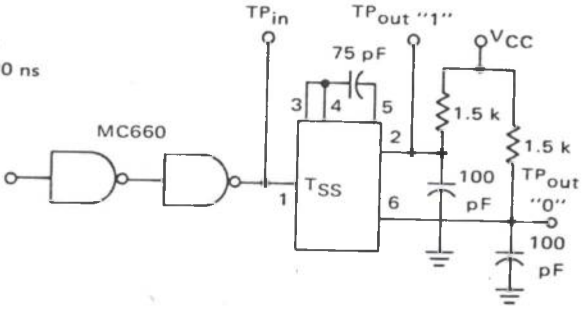
			MC667 Test Limits							TEST CURRENT / VOLTAGE VALUES (All Temperatures)											
										mA			Volts								
										I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{RX}	V_{CC}	V_{CCL}	V_{CCH}	
										12.0	-0.03	0.2	6.50	8.50	1.5	16.0	-13	15.0	14.0	16.0	
			−30°C		+25°C		+75°C			TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:											
Characteristic	Symbol	Pin Under Test	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{RX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	2	-	1.5	-	1.5	-	1.5	Vdc	2	-	3	-	-	-	-	-	-	14	-	7
		5†	-	2.8	-	2.8	-	2.8	↓	-	-	3	-	1	-	-	-	-	↓	-	7
		5†	-	2.1	-	2.1	-	2.1	↓	-	-	-	-	-	-	-	-	-	↓	-	1,3,7
		6	-	1.5	-	1.5	-	1.5	↓	6	-	-	1	-	-	-	-	-	↓	-	3,7
	V_{OH}	2	12.5	-	12.5	-	12.5	-	↓	-	2	-	-	-	-	-	-	-	↓	-	1,3,7
		5*	12.8	-	12.8	-	12.8	-	↓	-	-	-	1	-	-	-	-	-	↓	-	7
		6	12.5	-	12.5	-	12.5	-	↓	-	6	3	-	-	-	-	-	-	↓	-	1,7
Short-Circuit Current	I_{SC}	2	-6.5	-15	-6.5	-15	-6.5	-15	mAdc	-	-	-	-	-	-	-	-	-	-	14	2,3,7
		4	-0.64	-1.07	-0.64	-1.07	-0.64	-1.07	↓	-	-	-	-	-	-	-	-	-	-	↓	4,7
		5*	-19	-40	-19	-40	-19	-40	↓	-	-	-	-	-	-	-	-	-	-	↓	1,5,7
		6	-6.5	-15	-6.5	-15	-6.5	-15	↓	-	-	3	-	-	-	-	-	-	-	↓	6,7
Reverse Current	I_{R1}	1	-	2.0	-	2.0	-	2.0	µAdc	-	-	-	-	-	-	1	-	-	-	14	7
	I_{R2}	3	-	-2.0	-	-2.0	-	-2.0	µAdc	-	-	-	-	-	-	-	3	-	-	14	7
Output Leakage Current	I_{CEX}	2	-	100	-	100	-	100	µAdc	-	-	-	-	-	-	-	-	-	-	2,14	3,7
		6*	-	100	-	100	-	100	µAdc	-	-	-	-	-	-	-	-	-	-	6,14	7
Forward Current	I_F	1	-	1.2	-	1.2	-	1.2	mAdc	-	-	-	-	-	1	-	-	-	-	14	7
Power Drain Current (Both Units)	I_{CCL}	14	-	-	-	17.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1,3,7,11,13
	I_{CCH}	14*‡	-	-	-	23	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	1,13,14	7
										Pulse In	Pulse Out										
Switching Times	t_{1+2+}	2	-	-	-	275	-	-	ns	1	2	-	-	-	-	-	-	14	-	-	7
	t_{1+6-}	6	-	-	-	75	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7

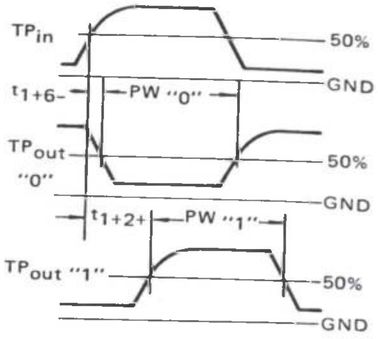
Pins not listed are left open.
*Pin 4 connected to pin 3
†Pin 4 connected to pin 5
‡Pin 11 connected to pin 10

SWITCHING TIME TEST CIRCUIT, WAVEFORMS AND DEFINITIONS



f = 500 kHz
DUTY CYCLE = 50%





Pulse Width: $PW_{"1"} \approx 0.7\ R_T\ C_T - 125 \times 10^{-9}$ } R_T in ohms

$PW_{"0"} \approx 0.7\ R_T\ C_T + 125 \times 10^{-9}$ } C_T in farads

C_T and R_T are timing resistor and capacitor.

Recovery Time: $t_R = 3\ C_T \times 10^3$ — t_R in seconds, C_T in farads

Duty Cycle: $DC \approx \dfrac{PW \times (100)}{PW + t_R} \approx \dfrac{R_T \times (100)}{R_T + 4.5}$

R_T in ohms

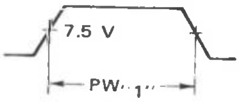
External Timing Resistor: $5.0\ k\Omega \leq R_{ext} \leq 56\ k\Omega$

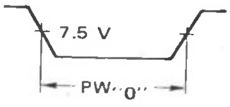
APPLICATION INFORMATION

Circuit Operation

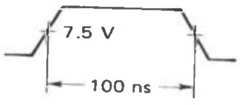
1. Any value of external capacitor (C_{ext}) may be used for the timing circuit. If an external resistor is used (20 kΩ internal is provided), $5.0\ k\Omega \leqslant R_{ext} \leqslant 56\ k\Omega$.
2. The generated pulse width (PW) is calculated as follows:

$$\left.\begin{aligned} PW_{"1"} &\approx 0.7\ R_T\ C_T - 125 \times 10^{-9} \\ PW_{"0"} &\approx 0.7\ R_T\ C_T + 125 \times 10^{-9} \end{aligned}\right\} \begin{aligned} &R_T \text{ in ohms} \\ &C_T \text{ in farads} \end{aligned}$$





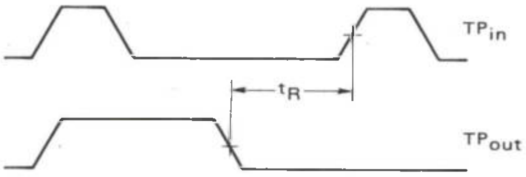
3. Input pulse width may be as narrow as 100 ns.



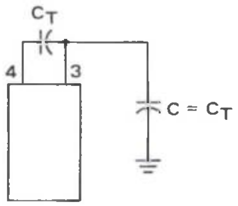
4. Sufficient recovery time must be allowed between input and output pulses. Recovery time is that period of time which the multivibrator requires for the capacitor to reach its quiescent state after triggering. Recovery time begins after the end of the output

pulse or the return of the input to the zero state, depending upon which occurs later.

$t_R = 3\,C_T \times 10^3$ t_R in seconds
C_T in farads

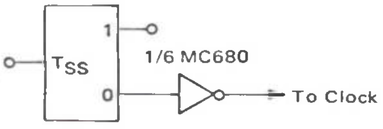


5. Although the toggle input displays the 5.0 volt noise margins of MHTL, the MC667 is susceptible to negative-going noise on the R-C timing network. False triggering may be caused by a negative-going spike of 1.5 volts or greater. V_{CC} should be bypassed at the package by a capacitor if false triggering occurs. Also, a capacitor equal to C_T connected from pin 3 (pin 11 for second multivibrator) to ground will improve noise immunity. The output pulse width will not be significantly affected.

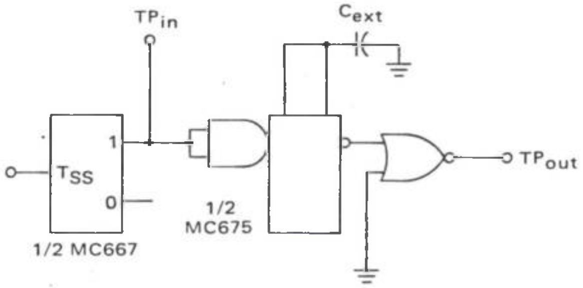


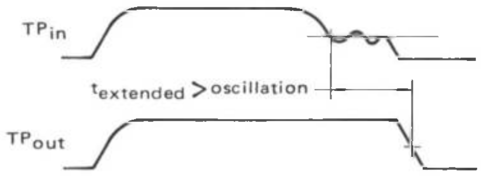
6. If the output pulse width is approximately 0.25 ms or greater, the logic "1" output fall time will be greater than 1.0 μs. If the logic "1" output is used to clock a flip-flop, this long fall time may cause improper toggling due to noise or oscillation on the clock line. Several solutions to this problem are shown.

   A. Use of the logic "0" output inverted. Rise and fall times of the logic "0" output are typically less than 0.5 μs.

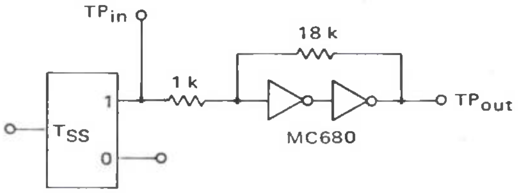


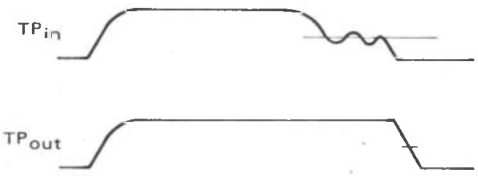
B. Let the output of the MC667 drive 1/2 MC675 pulse stretcher. The pulse stretcher extends the pulse width beyond the oscillation and gives a sharp fall time to the pulse. A typical value of C_{ext} (for the pulse stretcher) is 50 pF.





C. Let the output of the MC667 drive two active pullup inverters (MC680) or gates connected as a Schmitt Trigger. The trigger goes from the high to the low state at a threshold of approximately 6.5 volts. The oscillation then appears at a voltage level above the threshold of the Schmitt Trigger. Also, the hysteresis action of the network helps prevent oscillation from retriggering the Schmitt Trigger and gives sharp rise and fall time at TP_{out}.





TYPICAL APPLICATIONS (continued)

Application Ideas

The configuration shown in Figure 1 is a gated astable multivibrator. Pulse widths may be varied by changing time constants "t_1" and "t_2".

A sequential pulse train may be generated as shown in Figure 2. The timing diagram shows an approximate delay of 250 ns between pulses. Any pulse width in the train must be of sufficient length to allow proper recovery time of the multivibrator following that pulse.

FIGURE 1 – GATED ASTABLE MULTIVIBRATOR

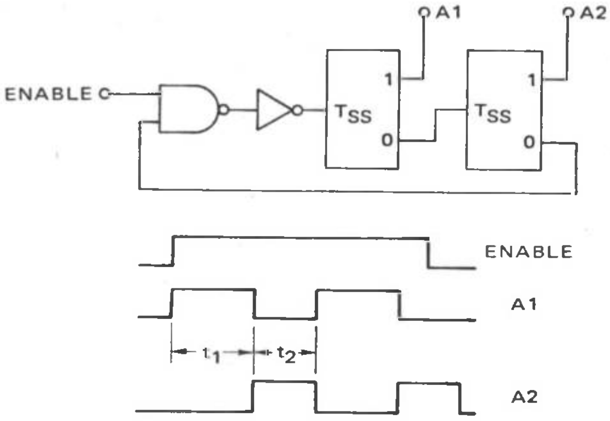
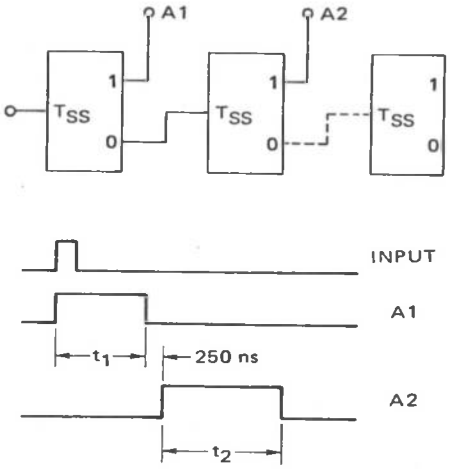


FIGURE 2 – GENERATION OF A SEQUENTIAL PULSE TRAIN



TYPICAL CHARACTERISTICS

FIGURE 3 – OUTPUT PULSE WIDTH versus CAPACITANCE

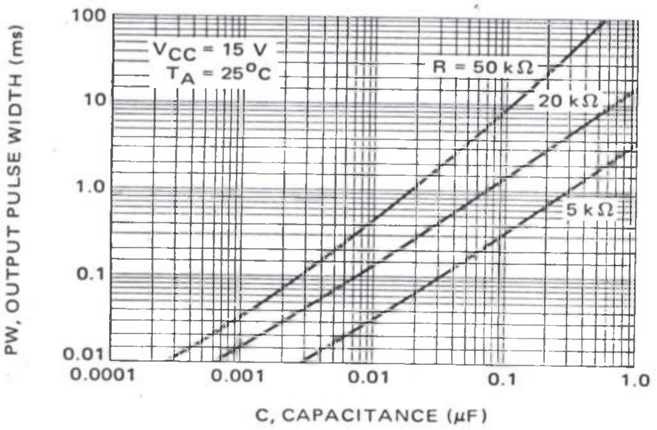
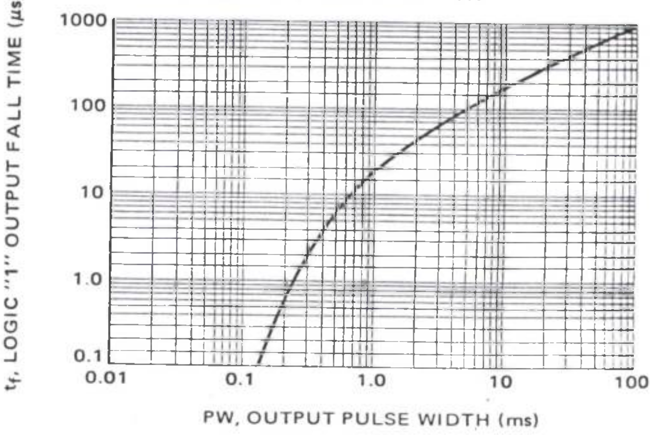
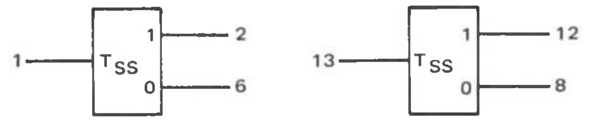


FIGURE 4 – LOGIC "1" OUTPUT FALL TIME versus OUTPUT PULSE WIDTH



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one monostable multivibrator. The other monostable multivibrator is tested in the same manner.



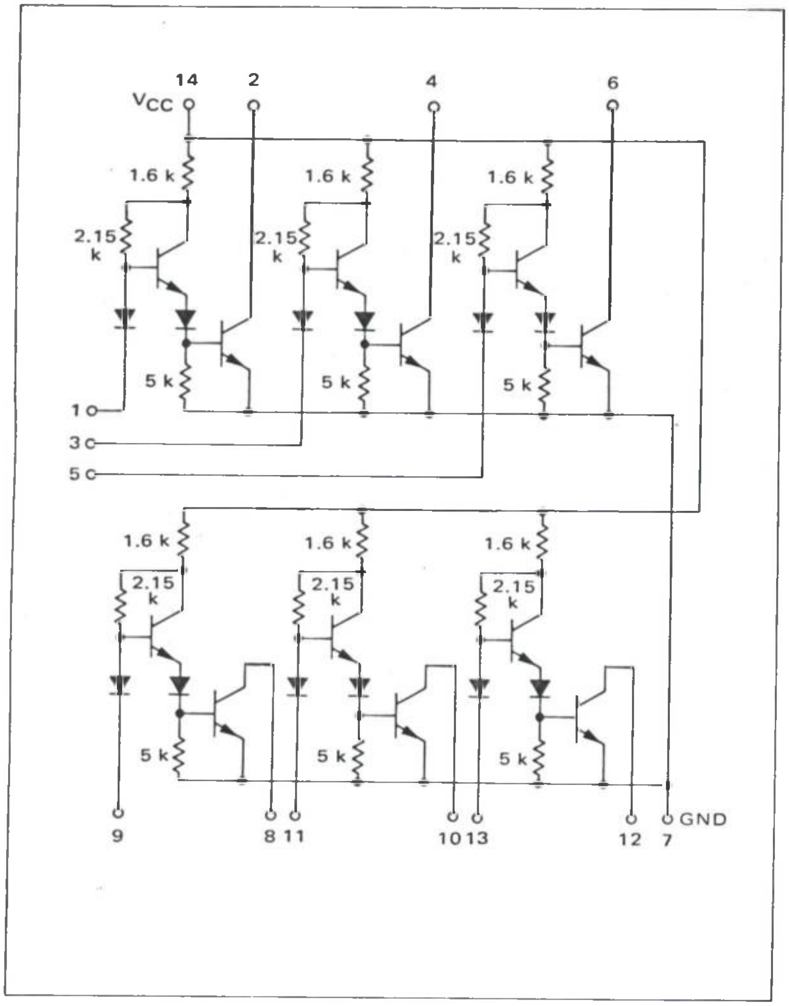
Characteristic	Symbol	Pin Under Test	MC667 Test Limits						Unit	TEST CURRENT / VOLTAGE VALUES (All Temperatures)											Gnd
			−30°C		+25°C		+75°C			mA			Volts								
			Min	Max	Min	Max	Min	Max		I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{RX}	V_{CC}	V_{CCL}	V_{CCH}	
										12.0	-0.03	0.2	6.50	8.50	1.5	16.0	-13	15.0	14.0	16.0	
										TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:											
										I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_F	V_R	V_{RX}	V_{CC}	V_{CCL}	V_{CCH}	
Output Voltage	V_{OL}	2	-	1.5	-	1.5	-	1.5	Vdc	2	-	3	-	-	-	-	-	-	14	-	7
		5†	-	2.8	-	2.8	-	2.8		-	-	3	-	1	-	-	-	-		-	7
		5†	-	2.1	-	2.1	-	2.1		-	-	-	-	-	-	-	-	-		-	1,3,7
		6	-	1.5	-	1.5	-	1.5		6	-	-	1	-	-	-	-	-		-	3,7
	V_{OH}	2	12.5	-	12.5	-	12.5	-		-	2	-	-	-	-	-	-	-		-	1,3,7
		5*	12.8	-	12.8	-	12.8	-		-	-	-	1	-	-	-	-	-		-	7
		6	12.5	-	12.5	-	12.5	-		-	6	3	-	-	-	-	-	-		-	1,7
Short-Circuit Current	I_{SC}	2	-6.5	-15	-6.5	-15	-6.5	-15	mAdc	-	-	-	-	-	-	-	-	-	-	14	2,3,7
		4	-0.64	-1.07	-0.64	-1.07	-0.64	-1.07		-	-	-	-	-	-	-	-	-	-		4,7
		5*	-19	-40	-19	-40	-19	-40		-	-	-	-	-	-	-	-	-	-		1,5,7
		6	-6.5	-15	-6.5	-15	-6.5	-15		-	-	3	-	-	-	-	-	-	-		6,7
Reverse Current	I_{R1}	1	-	2.0	-	2.0	-	2.0	μAdc	-	-	-	-	-	-	1	-	-	-	14	7
	I_{R2}	3	-	-2.0	-	-2.0	-	-2.0	μAdc	-	-	-	-	-	-	-	3	-	-	14	7
Output Leakage Current	I_{CEX}	2	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	-	-	-	2,14	3,7
		6*	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	-	-	-	6,14	7
Forward Current	I_F	1	-	1.2	-	1.2	-	1.2	mAdc	-	-	-	-	-	1	-	-	-	-	14	7
Power Drain Current (Both Units)	I_{CCL}	14	-	-	-	17.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1,3,7,11,13
	I_{CCH}	14*‡	-	-	-	23	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	1,13,14	7
Switching Times										Pulse In	Pulse Out										
	t_{1+2+}	2	-	-	-	275	-	-	ns	1	2	-	-	-	-	-	-	14	-	-	7
	t_{1+6-}	6	-	-	-	75	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.
*Pin 4 connected to pin 3
†Pin 4 connected to pin 5
‡Pin 11 connected to pin 10

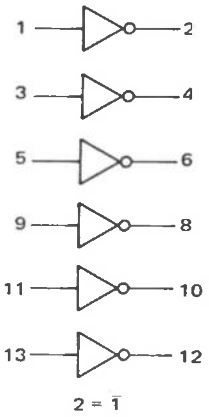
HEX INVERTER
(Open Collector)

MC935F · MC835F,P

JULY 1968



This hex inverter with no output pullup resistors, is useful in low-voltage applications such as lamp and/or relay drivers and interfacing with discrete component systems. It is convenient for obtaining wired-collector functions with little sacrifice in power dissipation or available fan-out.



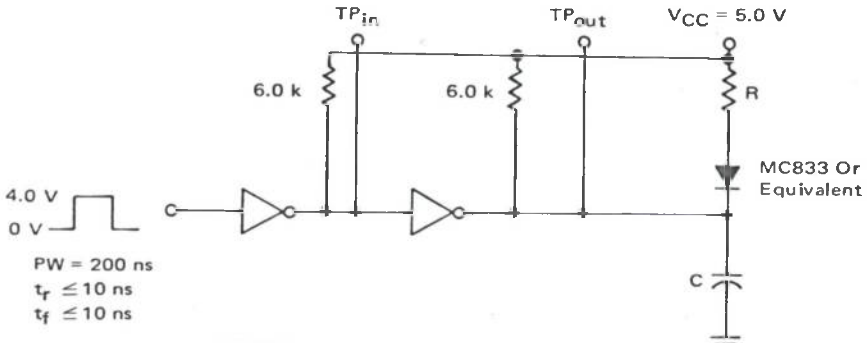
Input Loading Factor = 1

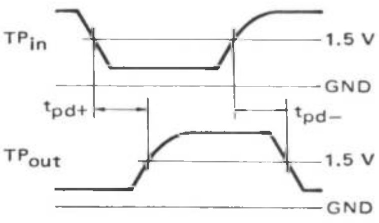
Output Loading Factor = 8

Total Power Dissipation = 42 mW typ/pkg

Propagation Delay Time = 30 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

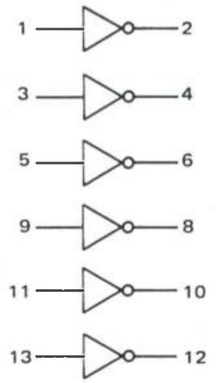




TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.



	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES										
		mA		Volts								
		I_{OL}	I_{CE}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
MC935	−55°C	11.4	-	1.40	2.10	0	4.00	-	-	4.50	5.50	-
	+25°C	12.0	5.00	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	8.00
	+125°C	10.8	-	0.80	2.00	0	4.00	-	-	4.50	5.50	-
MC835	0°C	12.0	-	1.20	2.00	0.45	4.00	-	-	5.00	5.00	-
	+25°C	12.0	5.00	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	8.00
	+75°C	11.4	-	0.95	1.80	0.50	4.00	-	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC935 Test Limits							MC835 Test Limits							TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:											Gnd
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C														
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{CE}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	
Output Voltage	V_{OL}	2	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	2	-	-	1	-	-	-	-	14	-	-	7
Output Breakdown Voltage	LV_{CE}	2	-	-	6.0	-	-	-	Vdc	-	-	6.0	-	-	-	Vdc	-	2	-	-	-	-	-	-	-	14	-	1,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	µAdc	-	5.0	-	5.0	-	10	µAdc	-	-	-	-	-	1	-	-	-	14	-	7
Output Leakage Current	I_{CEX}	2	-	-	-	50	-	-	µAdc	-	-	-	100	-	-	µAdc	-	-	1	-	-	-	2,14	-	-	-	-	7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	1	-	-	-	-	14	-	7
Power Drain Current (Total Device)	I_{PDH}	14	-	-	-	13.5	-	-	mAdc	-	-	-	17.5	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	-	7
	I_{max}	14	-	-	-	16.5	-	-	mAdc	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1,3,5,7, 9,11,13
Switching Times																	Pulse In	Pulse Out										
	t_{pd+}	1,2	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	2	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,2	-	-	10	30	-	-	ns	-	-	10	30	-	-	ns	1	2	-	-	-	-	-	14	-	-	-	7

Pins not listed are left open.

DUAL J-K FLIP-FLOP

MDTL MC930/830 series **MOTOROLA**

MAY 1971

MC952F · MC852F, P
MC953F · MC853F, P
MC955F · MC855F, P
MC956F · MC856F, P

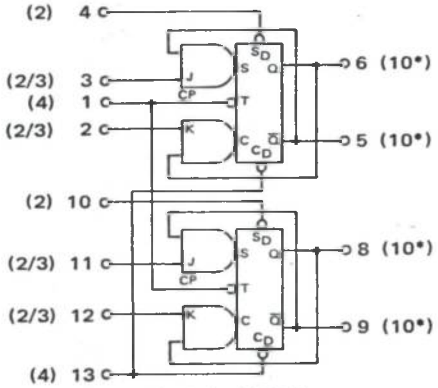
Each section of the monolithic MC952/MC852 and MC953/MC853 dual J-K clocked flip-flops consists of two directly-coupled flip-flops operating on the "master-slave" principle. Operation depends only on voltage levels, so the rise and fall times of the input clock are unimportant in determining the state of the flip-flop. Input information is stored in the "master" flip-flop when the clock voltage is high and is transferred to the "slave" when the clock voltage goes low.

The MC952/MC852 has a common clock input which makes this device suitable for clocked counters and shift register applications. A common direct clear (C_D) and separate direct sets (S_D) are available. The direct inputs override all synchronous inputs.

The MC953/MC853 has separate clock inputs to each flip-flop, which makes the device suitable for ripple counter applications. Separate direct set inputs which override the synchronous inputs are also provided.

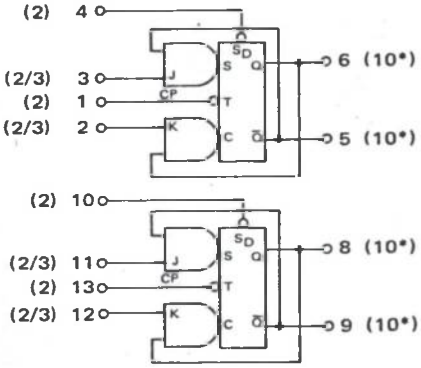
The outputs of the flip-flops are buffered, thereby reducing the possibility of circuit disturbance from external line noise.

MC952/MC852



* 12 for MC852

MC953/MC853



* 12 for MC853

Number in parenthesis indicates loading.

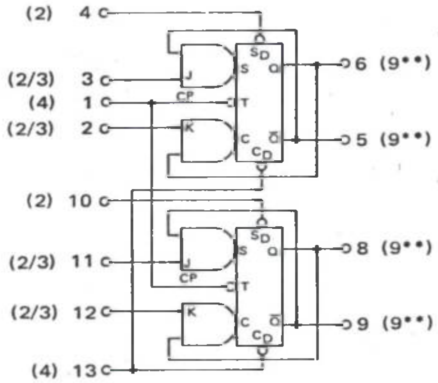
Each section of the monolithic MC955/MC855 and MC956/MC856 dual J-K clocked flip-flops consists of two directly-coupled flip-flops operating on the "master-slave" principle. Input information is stored in the "master" flip-flop when the clock voltage is high and is transferred to the "slave" when the clock voltage goes low.

The MC955/MC855 has a common clock input which makes this device suitable for clocked counters and shift register applications. A common direct clear (C_D) and separate direct sets (S_D) are available. The direct inputs override all synchronous inputs.

The MC956/MC856 has separate clock inputs to each flip-flop, which makes the device suitable for ripple counter applications. Separate direct set inputs which override the synchronous inputs are also provided.

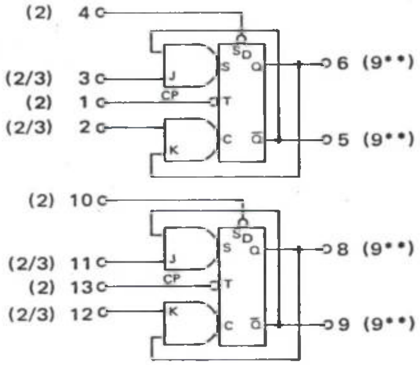
The outputs of the flip-flops are buffered, thereby reducing the possibility of circuit disturbance from external line noise. The output pull-up resistor has been changed from that utilized in the MC952/MC852 and MC953/MC853 in order to improve the propagation delay versus capacitance characteristics.

MC955/MC855



** 11 for MC855

MC956/MC856



** 11 for MC856

Number in parenthesis indicates loading.

Total Power Dissipation
MC952/MC852, MC953/MC853
= 120 mW typ/pkg
MC955/MC855, MC956/MC856
= 140 mW typ/pkg

Propagation Delay Time = 40 ns typ

ASYNCHRONOUS TRUTH TABLE MC952/MC852 and MC955/MC855

S_D	C_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

ASYNCHRONOUS TRUTH TABLE MC953/MC853 and MC956/MC856

S_D	Q	$\overline{Q}$
1	NC	NC
0	1	0

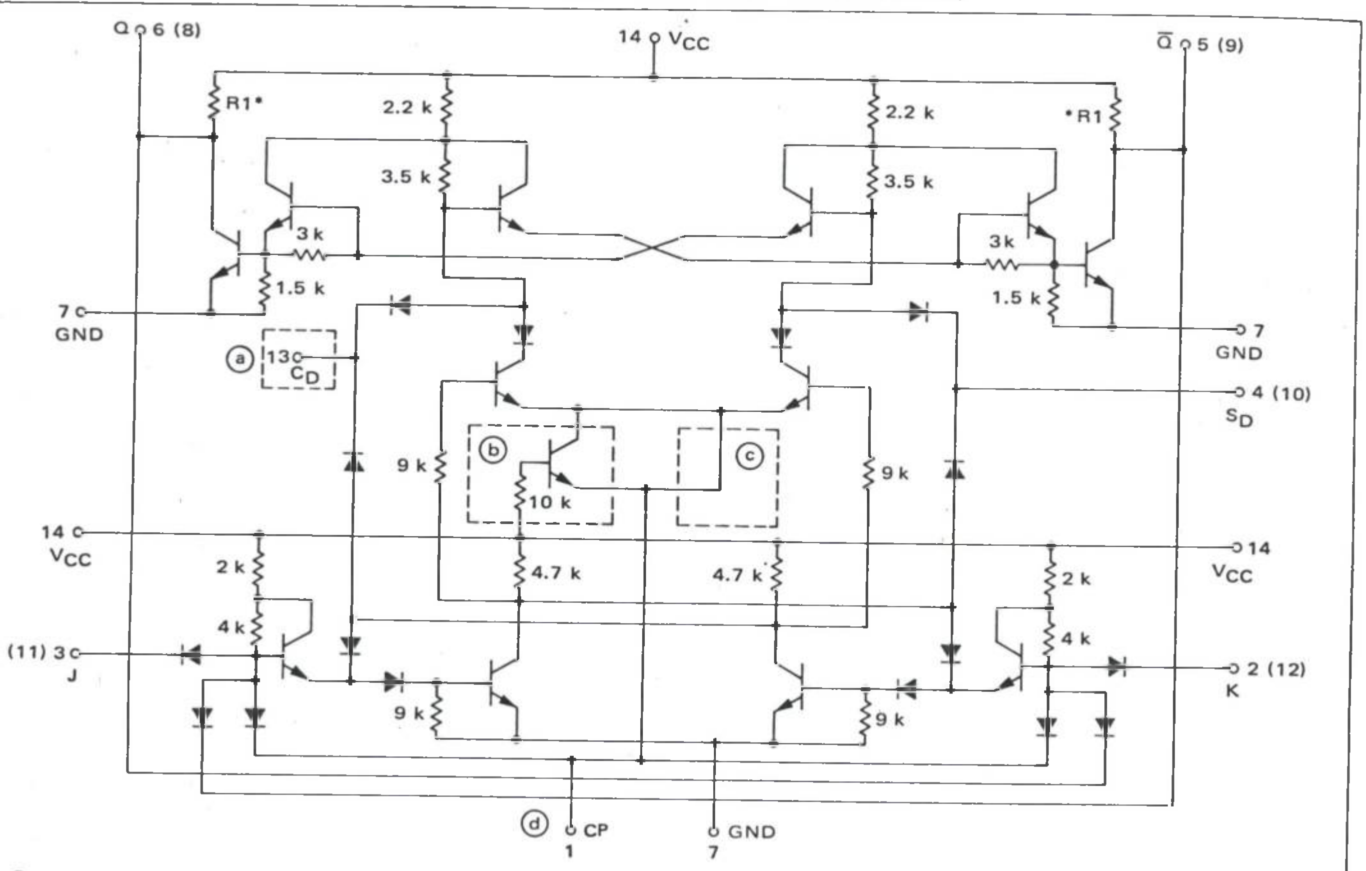
J-K TRUTH TABLE — All Types †

t_n		t_{n+1}
J	K	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs; they are independent of all other inputs.

† Valid only when J and K inputs remain unchanged during period while CP is high.

CIRCUIT SCHEMATIC (1/2 OF CIRCUIT SHOWN)

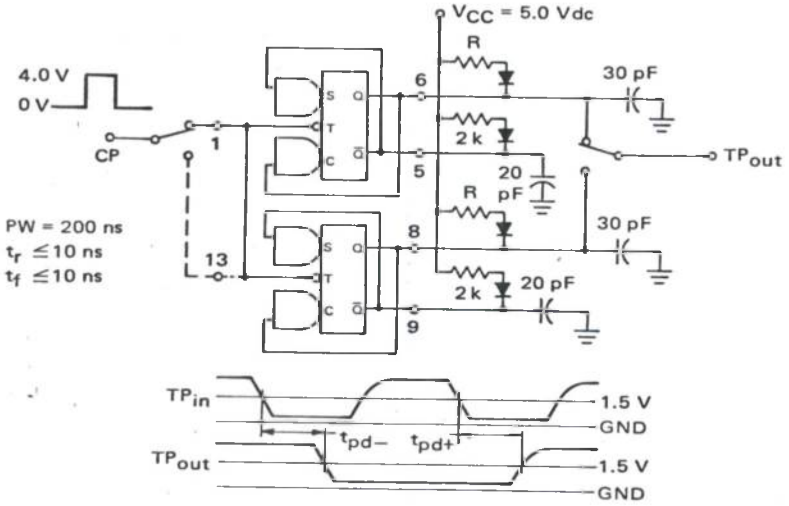


ⓐ Used only on MC952/MC852 and MC955/MC855
ⓑ Used only on MC952/MC852 and MC953/MC853
ⓒ Used only on MC955/MC855 and MC956/MC856
ⓓ Pin 13 used for other side of MC953/MC853 and MC956/MC856

NOTE: Number in parenthesis indicates pin number for other half of the schematic. Ground and V_{CC} pins are common to both sides.

* MC952/MC852 and MC953/MC853 – 6 k
MC955/MC855 and MC956/MC856 – 2 k

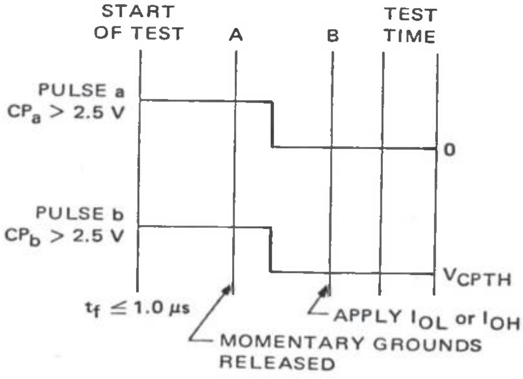
PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS



Test circuit shown for MC952/MC852 and MC955/MC855.
Use dotted-line connection for MC953/MC853 and MC956/MC856, which have separate toggle inputs.
Ground pin 7. Only connected inputs are shown. All others are open.
MC833 or equivalent used for diodes.

TEST	R
t_{pd+}	3.9 k ohms
t_{pd-}	400 ohms

CLOCK PULSE WAVEFORMS

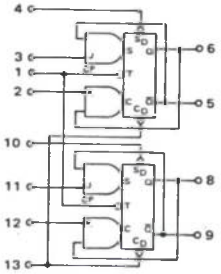


TEST CONDITIONS

T_A	V_{CPTH}	
	MC952, MC953	MC955, MC956
–55°C +25°C +125°C	1.15 V 0.95 V 0.65 V	1.30 V 1.15 V 0.85 V
	MC852, MC853	MC855, MC856
0°C +25°C +75°C	1.00 V 0.95 V 0.65 V	1.20 V 1.15 V 0.85 V

MC952/MC852
MC955/MC855

ELECTRICAL CHARACTERISTICS



		TEST CURRENT/VOLTAGE VALUES											
		mA				Volts							
	@ Test Temperature	I_{OL}		I_{OH}		V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
		MC952	MC955	MC952	MC955								
MC952, MC955	−55°C	14.6	13.0	-0.12	-0.5	1.40	2.10	0	4.00	-	4.50	5.50	-
	+25°C	15.2	13.6	-0.12	-0.5	1.10	2.00	0	4.00	5.00	4.50	5.50	8.00
	+125°C	13.8	12.3	-0.12	-0.5	0.80	2.00	0	4.00	-	4.50	5.50	-
		MC852	MC855	MC852	MC855								
MC852, MC855	0°C	16.8	15.4	-0.12	-0.5	1.20	2.00	0.45	4.00	-	5.00	5.00	-
	+25°C	16.8	15.4	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	16.0	14.6	-0.12	-0.5	0.95	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC952, MC955 TEST LIMITS							MC852, MC855 TEST LIMITS							TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:												
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C															
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	CP_a§	CP_b§	Gnd
Output Voltage	V_{OL}	5	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	5†	-	2	-	-	-	-	14	-	-	-	1	7,13‡
		6	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	6†	-	3	-	-	-	-	↓	-	-	-	↓	4‡,7
		8	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	8†	-	11	-	-	-	-	↓	-	-	-	↓	7,10‡
		9	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	9†	-	12	-	-	-	-	↓	-	-	-	↓	7,13‡
	V_{OH}	5	2.50	-	2.60	-	2.50	-	↓	2.60	-	2.60	-	2.50	-	↓	↓	5†	3	2	-	-	-	↓	-	-	1	-	4‡,7
		5	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	5	2,13	4	-	-	-	↓	-	-	↓	-	7
		6	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	6†	2	3	-	-	-	↓	-	-	↓	-	7,13‡
		6	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	6	3,4	13	-	-	-	↓	-	-	↓	-	7
		8	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	8†	12	11	-	-	-	↓	-	-	↓	-	7,13‡
		8	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	8	10,11	13	-	-	-	↓	-	-	↓	-	7
		9	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	9†	11	12	-	-	-	↓	-	-	↓	-	7,10‡
		9	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	9	12,13	10	-	-	-	↓	-	-	↓	-	7
Short-Circuit Current MC952/MC852	I_{SC}	5	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	mAdc	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	mAdc	-	-	-	-	-	-	-	-	14	-	-	1	5,7
		6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	-	-	-	-	↓	-	-	↓	6,7
		8	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	-	-	-	-	↓	-	-	↓	7,8
		9	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	-	-	-	-	↓	-	-	↓	7,9
MC955/MC855		5	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10	↓	-2.60	-5.20	-2.35	-4.75	-2.20	-4.40	↓	-	-	-	-	-	-	-	-	↓	-	-	↓	5,7
		6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	-	-	-	-	↓	-	-	↓	6,7
		8	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	-	-	-	-	↓	-	-	↓	7,8
		9	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	-	-	-	-	↓	-	-	↓	7,9
Reverse Current All Types	I_R	2	-	2.0	-	2.0	-	5.0	µAdc	-	5.0	-	5.0	-	10	µAdc	-	-	-	-	-	2	-	-	14	-	-	-	1,7,13
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	3	-	-	↓	-	-	-	1,4,7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	4	-	-	↓	-	1	-	2,6,7
		10	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	10	-	-	↓	-	1	-	7,8,12
		11	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	11	-	-	↓	-	-	-	1,7,10
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	12	-	-	↓	-	-	-	1,7,13
All Types	$2\,I_R$	13	-	4.0	-	4.0	-	10	↓	-	10	-	10	-	20	↓	-	-	-	-	-	13	-	-	↓	-	1	-	3,5,7,9,11
MC952/MC852	$2\,I_{RCP}$	1	-	20	-	20	-	40	↓	-	40	-	40	-	60	↓	-	-	-	-	-	1,14	-	-	-	-	-	-	2,3,5,6,7,8,9,11,12
MC955/MC855	$2\,I_{RCP}$	1	-	20	-	20	-	40	↓	-	40	-	40	-	60	↓	-	-	-	-	-	1	-	-	14	-	-	-	2,3,5,6,7,8,9,11,12
Forward Current	$2/3\,I_F$	2	-	-1.07	-	-1.07	-	-1.00	mAdc	-	-0.95	-	-0.95	-	-0.90	mAdc	-	-	-	-	2	-	-	-	14	-	-	1	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	3	-	-	-	↓	-	-	↓	↓
		11	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	11	-	-	-	↓	-	-	↓	↓
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	12	-	-	-	↓	-	-	↓	↓
	$2\,I_{FCP}$	1	-	-6.40	-	-6.40	-	-6.00	↓	-	-5.60	-	-5.60	-	-5.34	↓	-	-	4,10	-	1	-	-	-	↓	-	-	-	↓
		1	-	-6.40	-	-6.40	-	-6.00	↓	-	-5.60	-	-5.60	-	-5.34	↓	-	-	13	-	1	-	-	-	↓	-	-	-	↓
	I_{FS}	4	-	-3.20	-	-3.20	-	-3.00	↓	-	-2.80	-	-2.80	-	-2.67	↓	-	-	-	-	4	-	-	-	↓	-	-	-	2,3,7,13
		10	-	-3.20	-	-3.20	-	-3.00	↓	-	-2.80	-	-2.80	-	-2.67	↓	-	-	-	-	10	-	-	-	↓	-	-	-	7,11,12,13
	$2\,I_{FS}$	13	-	-6.40	-	-6.40	-	-6.00	↓	-	-5.60	-	-5.60	-	-5.34	↓	-	-	-	-	13	-	-	-	↓	-	-	-	2,3,4,7,10,11,12
Power Drain Current MC952/MC852	I_{PDH}	14	-	-	-	22	-	-	mAdc	-	-	-	28	-	-	mAdc	-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	32	-	-	↓	-	-	-	36	-	-	↓	-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,7,10,11,12
MC955/MC855	I_{PDH}	14	-	-	-	27	-	-	↓	-	-	-	34	-	-	↓	-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	38	-	-	↓	-	-	-	45	-	-	↓	-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,7,10,11,12
Switching Times																	Pulse In	Pulse Out											
MC952/MC852	t_{pd+}	1,6	-	-	25	100	-	-	ns	-	-	25	100	-	-	ns	1	6	-	-	-	-	14	-	-	-	-	-	7
	t_{pd-}	1,6	-	-	15	55	-	-	↓	-	-	15	55	-	-	↓	↓	6	-	-	-	-	↓	-	-	-	-	-	↓
	t_{pd+}	1,8	-	-	25	100	-	-	↓	-	-	25	100	-	-	↓	↓	8	-	-	-	-	↓	-	-	-	-	-	↓
	t_{pd-}	1,8	-	-	15	55	-	-	↓	-	-	15	55	-	-	↓	↓	8	-	-	-	-	↓	-	-	-	-	-	↓
MC955/MC855	t_{pd+}	1,6	-	-	25	75	-	-	↓	-	-	25	75	-	-	↓	↓	6	-	-	-	-	↓	-	-	-	-	-	↓
	t_{pd-}	1,6	-	-	15	55	-	-	↓	-	-	15	55	-	-	↓	↓	6	-	-	-	-	↓	-	-	-	-	-	↓
	t_{pd+}	1,8	-	-	25	75	-	-	↓	-	-	25	75	-	-	↓	↓	8	-	-	-	-	↓	-	-	-	-	-	↓
	t_{pd-}	1,8	-	-	15	55	-	-	↓	-	-	15	55	-	-	↓	↓	8	-	-	-	-	↓	-	-	-	-	-	↓

Pins not listed are left open.

§ CP_a = Clock Pulse a; CP_b = Clock Pulse b } See Clock Pulse Waveforms.

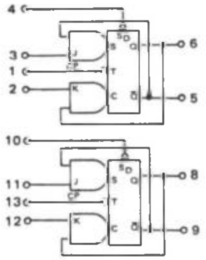
† Applied after Clock Pulse.

‡ Momentary Ground.

MC953/MC853
MC956/MC856

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



@ Test Temperature		I_{OL} (mA) MC953	I_{OL} (mA) MC956	I_{OH} (mA) MC953	I_{OH} (mA) MC956	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
MC953, MC956	−55°C	14.6	13.0	-0.12	-0.5	1.40	2.10	0	4.00	-	4.50	5.50	-
	+25°C	15.2	13.6	-0.12	-0.5	1.10	2.00	0	4.00	5.00	4.50	5.50	8.00
	+125°C	13.8	12.3	-0.12	-0.5	0.80	2.00	0	4.00	-	4.50	5.50	-
		MC853	MC856	MC853	MC856								
MC853, MC856	0°C	16.8	15.4	-0.12	-0.5	1.20	2.00	0.45	4.00	-	5.00	5.00	-
	+25°C	16.8	15.4	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	16.0	14.6	-0.12	-0.5	0.95	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC953, MC956 −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC853, MC856 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	CP_a§	CP_b§	Gnd
Output Voltage	V_{OL}	5	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	5	-	4	-	-	-	-	14	-	-	-	-	7
		6	-	0.40	-	0.40	-	0.45	↓	-	0.45	-	0.45	-	0.50	↓	6†	-	3	-	-	-	-	↓	-	-	-	1	4‡,7
	V_{OH}	5	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	5†	3	2	-	-	-		-	-	1	-	4‡,7
		6	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	6	3,4	-	-	-	-		-	-	1	-	7
Short-Circuit Current MC953/MC853	I_{SC}	5	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	mAdc	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	mAdc	-	-	-	-	-	-	-	-	14	-	-	1	5,7
		6	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	↓	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	↓	-	-	-	-	-	-	-	-	↓	-	-	↓	6,7
MC956/MC856		5	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10		-2.60	-5.20	-2.35	-4.75	-2.20	-4.40		-	-	-	-	-	-	-	-		-	-		5,7
		6	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10		-2.60	-5.20	-2.35	-4.75	-2.20	-4.40		-	-	-	-	-	-	-	-		-	-		6,7
Reverse Current All Types	I_R	2	-	2.0	-	2.0	-	5.0	µAdc	-	5.0	-	5.0	-	10	µAdc	-	-	-	-	-	2	-	-	14	-	-	-	1,7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	3	-	-	↓	-	-	-	1,7
		4	-		-		-			-		-		-			-	-	-	-	-	4	-	-		-	-	-	2,6,7
MC953/MC853	I_{RCP}	1	-	10	-	10	-	20		-	20	-	20	-	30		-	-	-	-	-	1,14	-	-	-	-	-	-	2,3,5,6,7
MC956/MC856	I_{RCP}	1	-	10	-	10	-	20		-	20	-	20	-	30		-	-	-	-	-	1	-	-	14	-	-	-	2,3,5,6,7
Forward Current	$2/3\ I_F$	2	-	-1.07	-	-1.07	-	-1.00	mAdc	-	-0.95	-	-0.95	-	-0.90	mAdc	-	-	-	-	2	-	-	-	14	-	-	1	7
	$2/3\ I_F$	3	-	-1.07	-	-1.07	-	-1.00	↓	-	-0.95	-	-0.95	-	-0.90	↓	-	-	-	-	3	-	-	-	↓	-	-	1	↓
	I_{FCP}	1	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67		-	-	4	-	1	-	-	-		-	-	-	
	I_{FS}	4	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67		-	-	-	-	4	-	-	-		-	-	-	3,7
Power Drain Current (Total Device) MC953/MC853	I_{PDH}	14	-	-	-	22	-	-	mAdc	-	-	-	28	-	-	mAdc	-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	32	-	-	↓	-	-	-	36	-	-	↓	-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,7,10, 11,12,13
MC956/MC856	I_{PDH}	14	-	-	-	27	-	-		-	-	-	34	-	-		-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	38	-	-		-	-	-	45	-	-		-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,7,10, 11,12,13
Switching Times																	Pulse In	Pulse Out											
MC953/MC853	t_{pd+}	1,6	-	-	25	100	-	-	ns	-	-	25	100	-	-	ns	1	6	-	-	-	-	14	-	-	-	-	-	7
	t_{pd-}	1,6	-	-	15	55	-	-	↓	-	-	15	55	-	-	↓	↓	↓	-	-	-	-	↓	-	-	-	-	-	↓
MC956/MC856	t_{pd+}	1,6	-	-	25	75	-	-		-	-	25	75	-	-				-	-	-	-		-	-	-	-	-	
	t_{pd-}	1,6	-	-	15	55	-	-		-	-	15	55	-	-				-	-	-	-		-	-	-	-	-	

Pins not listed are left open.

§ CP_a = Clock Pulse a, CP_b = Clock Pulse b } See Clock Pulse Waveforms.

† Applied after Clock Pulse.

‡ Momentary ground.

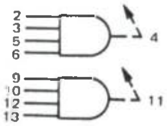
3517-14 PRINTED IN USA 5-71 IMPERIAL LITHO B22598 5M

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	–	2	3	4	5	6	7	–	9	10	11	12	13	–
Metal Can	–	10	1	2	3	4	5	–	6	7	8	9	–	–



TEST CURRENT / VOLTAGE VALUES (All Temperatures)	
mA	Volts
I_{FD}	V_R
2.00	4.00

Characteristic	Symbol	Pin Under Test	MC933 Test Limits							MC833 Test Limits							TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:		
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C					
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit	I_{FD}	V_R	Gnd
Forward Voltage	V_{FD}	4	-	0.98	-	0.82	-	0.65	Vdc	-	0.90	-	0.82	-	0.75	Vdc	4	-	2,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	↓	-	3,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	↓	-	5,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	↓	-	6,7
		↓	0.85	-	0.70	-	0.50	-	↓	0.75	-	0.68	-	0.60	-	↓	↓	-	2,3,5,6,7
Reverse Current	I_R	2	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	2	3,5,6,7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	2,5,6,7
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	5	2,3,6,7
		6	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	6	2,3,5,7
	$5\,I_R$	4	-	10	-	10	-	25	↓	-	-	-	-	-	-	↓	-	4	7
	$2\,I_R$	4	-	-	-	-	-	-	↓	-	-	-	10	-	-	↓	-	4	7

Pins not listed are left open.

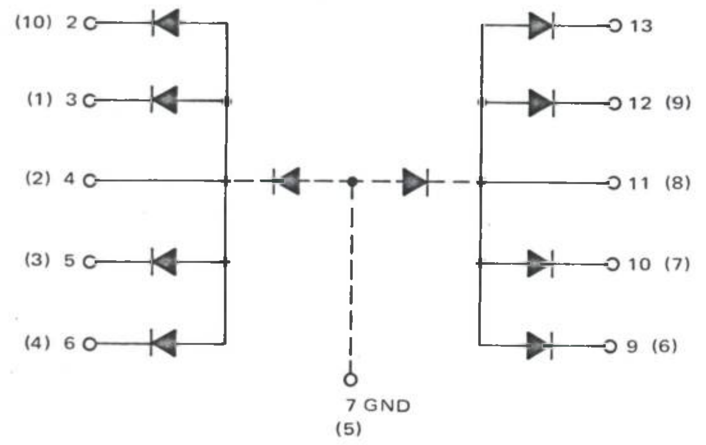
MARCH 1968

DUAL 4-INPUT EXPANDER

MC933F • MC833F, P

DUAL 4-3 INPUT EXPANDER

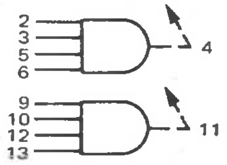
MC933G • MC833G



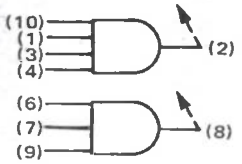
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.

This dual expander consists of two independent diode networks with characteristics matched to the input diodes of the gate and buffer elements in this logic family. Its use increases the fan-in capability of other MDTL devices to a maximum of 20 while only slightly affecting performance.

MC933F/MC833F, P



MC933G/MC833G



MARCH 1968

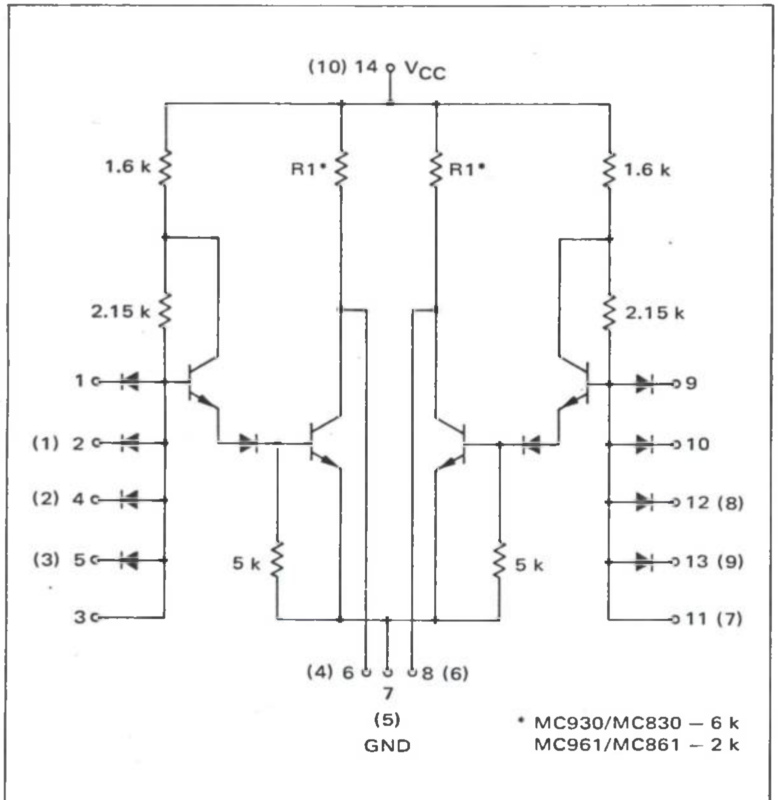
EXPANDABLE DUAL 4-INPUT "NAND" GATE

MC930F · MC830F, P
MC961F · MC861F, P

EXPANDABLE DUAL 3-2 INPUT "NAND" GATE

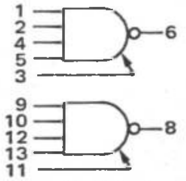
MC930G · MC830G
MC961G · MC861G

This gate element, in the 14-pin flat and dual in-line packages, consists of two expandable 4-input NAND gate circuits. Since the metal can (G suffix) has only 10 pins, that circuit consists of one 3-input and one 2-input expandable gate. The elements may be cross-coupled to form a bistable multivibrator, or the outputs may be connected in parallel to perform the logic "OR" function.



* MC930/MC830 – 6 k
MC961/MC861 – 2 k

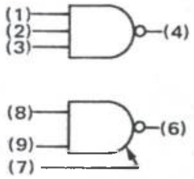
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.



MC930F/MC830F, P
MC961F/MC861F, P

Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

Negative Logic: $6 = \overline{1 + 2 + 4 + 5 + [3]}$



MC930G/MC830G
MC961G/MC861G

Positive Logic: $4 = \overline{1 \cdot 2 \cdot 3}$

Negative Logic: $4 = \overline{1 + 2 + 3}$

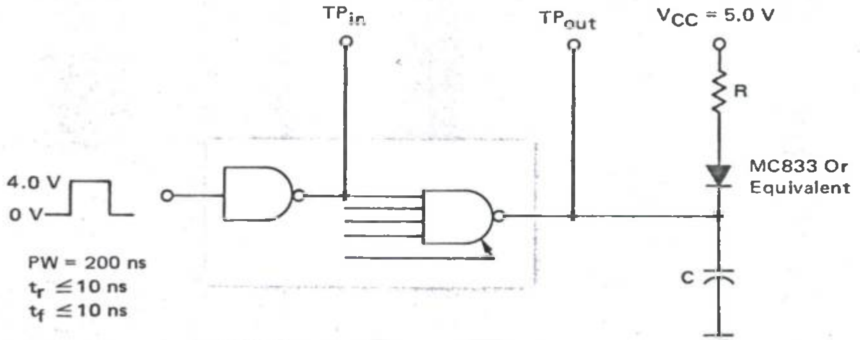
Input Loading Factor = 1

Output Loading Factor:
MC930/MC830 = 8
MC961/MC861 = 7

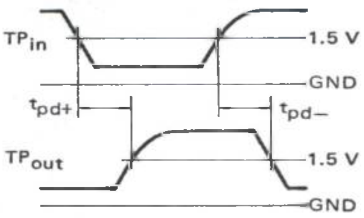
Total Power Dissipation:	MC930 MC830	MC961 MC861
Inputs Low	12 mW	12 mW
Inputs High	26 mW	42 mW
50% duty Cycle	19 mW	27 mW

Propagation Delay Time
MC930/MC830 = 30 ns typ
MC961/MC861 = 25 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



PW = 200 ns
$t_r \leq 10$ ns
$t_f \leq 10$ ns



TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF

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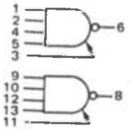
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.



PACKAGE	PIN NUMBER													
Flat/Dual In-Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Metal Can	–	1	–	2	3	4	5	6	–	–	7	8	9	10

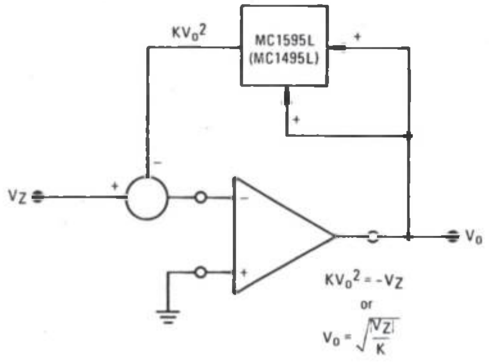
	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES													
		mA				Volts									
		I_{OL}		I_{OH}		V_{IL}	V_{IH}	V_X	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
		MC930	MC961	MC930	MC961										
MC930, MC961	−55°C	11.4	10.4	-0.12	-0.5	1.40	2.10	-	0	4.00	-	-	4.50	5.50	-
	+25°C	12.0	11.0	-0.12	-0.5	1.10	2.00	1.80	0	4.00	4.50	5.00	4.50	5.50	8.00
	+125°C	10.8	9.8	-0.12	-0.5	0.80	2.00	-	0	4.00	-	-	4.50	5.50	-
		MC830	MC861	MC830	MC861										
MC830, MC861	0°C	12.0	11.0	-0.12	-0.5	1.20	2.00	-	0.45	4.00	-	-	5.00	5.00	-
	+25°C	12.0	11.0	-0.12	-0.5	1.10	1.90	1.80	0.45	4.00	5.00	5.00	5.00	5.00	8.00
	+75°C	11.4	10.4	-0.12	-0.5	0.95	1.80	-	0.50	4.00	-	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC930, MC961 TEST LIMITS							MC830, MC861 TEST LIMITS							TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:												
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C															
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_X	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	1,2, 4,5	-	-	-	-	-	14	-	-	7
	V_{OH}	6	2.50	-	2.60	-	2.50	-	↓	2.60	-	2.60	-	2.50	-	↓	-	6	1	-	-	-	-	-	-	↓	-	-	↓
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	↓	2	-	-	-	-	-	-	↓	-	-	↓
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	↓	4	-	-	-	-	-	-	↓	-	-	↓
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	↓	5	-	-	-	-	-	-	↓	-	-	↓
		↓	-	-	↓	-	-	-	↓	-	-	↓	-	-	-	↓	-	↓	-	-	3	-	-	-	-	↓	-	-	↓
Short-Circuit Current																													
MC930/MC830	I_{SC}	6	-	-1.34	-	-1.34	-	-1.30	mAdc	-	-1.30	-	-1.30	-	-1.25	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	1, 6, 7
MC961/MC861		6	-	-4.00	-	-4.00	-	-3.90	mAdc	-	-3.90	-	-3.90	-	-3.75	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	1, 6, 7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	-	1	-	-	-	14	-	2, 4, 5, 7
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	2	-	-	-	↓	-	1, 4, 5, 7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	4	-	-	-	↓	-	1, 2, 5, 7
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	5	-	-	-	↓	-	1, 2, 4, 7
Output Leakage Current	I_{CEX}	6	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	-	6,14	-	-	-	-	1, 7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	-	1	2,4,5	-	-	-	14	-	7
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	2	1,4,5	-	-	-	↓	-	↓
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	4	1,2,5	-	-	-	↓	-	↓
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	5	1,2,4	-	-	-	↓	-	↓
Power Drain Current (Total Device)																													
MC930/MC830	I_{PDH}	14	-	-	-	6.5	-	-	mAdc	-	-	-	8.0	-	-	mAdc	-	-	-	-	-	-	-	-	14	-	-	-	7
MC961/MC861	I_{PDH}	14	-	-	-	10.7	-	-	↓	-	-	-	13.1	-	-	↓	-	-	-	-	-	-	-	-	14	-	-	-	7
All Types	I_{max}	14	-	-	-	5.5	-	-	↓	-	-	-	8.0	-	-	↓	-	-	-	-	-	-	-	-	-	-	-	14	1, 7, 9
Switching Times																	Pulse In	Pulse Out											
MC930/MC830	t_{pd+}	1, 6	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1, 6	-	-	10	30	-	-	↓	-	-	10	30	-	-	↓	↓	↓	-	-	-	-	-	-	↓	-	-	-	↓
MC961/MC861	t_{pd+}	1, 6	-	-	15	60	-	-	↓	-	-	15	60	-	-	↓	↓	↓	-	-	-	-	-	-	↓	-	-	-	↓
	t_{pd-}	1, 6	-	-	10	30	-	-	↓	-	-	10	30	-	-	↓	↓	↓	-	-	-	-	-	-	↓	-	-	-	↓

Pins not listed are left open.

OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 26 – BASIC SQUARE ROOT CIRCUIT



as indicated in Figure 26. This circuit may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 27) protects against accidental latch-up.

This circuit also may be adjusted in the closed-loop mode as follows:

1. Set V_Z to −0.01 volts and adjust P_4 (output offset) for V_o = +0.316 volts, being careful to approach the output from the positive side to preclude the effect of the output diode clamping.
2. Set V_Z to −0.9 volts and adjust P_2 (X adjust) for V_o = +3.0 volts.
3. Set V_Z to −10 volts and adjust P_3 (scale factor adjust) for V_o = +10 volts.
4. Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

6. AC Applications

The applications that follow demonstrate the versatility of the monolithic multiplier. If a potted multiplier is used for these cases, the results generally would not be as good because the potted units have circuits that, although they optimize dc multiplication operation, can hinder ac applications.

6.1 Frequency doubling often is done with a diode where the fundamental plus a series of harmonics are generated. However, extensive filtering is required to obtain the desired harmonic, and the second harmonic obtained under this technique usually is small in magnitude and requires amplification.

When a multiplier is used to double frequency the second harmonic is obtained directly, except for a dc term, which can be removed with ac coupling.

$$e_o = KE^2 \cos^2 \omega t$$

$$e_o = \frac{KE^2}{2} (1 + \cos 2\omega t).$$

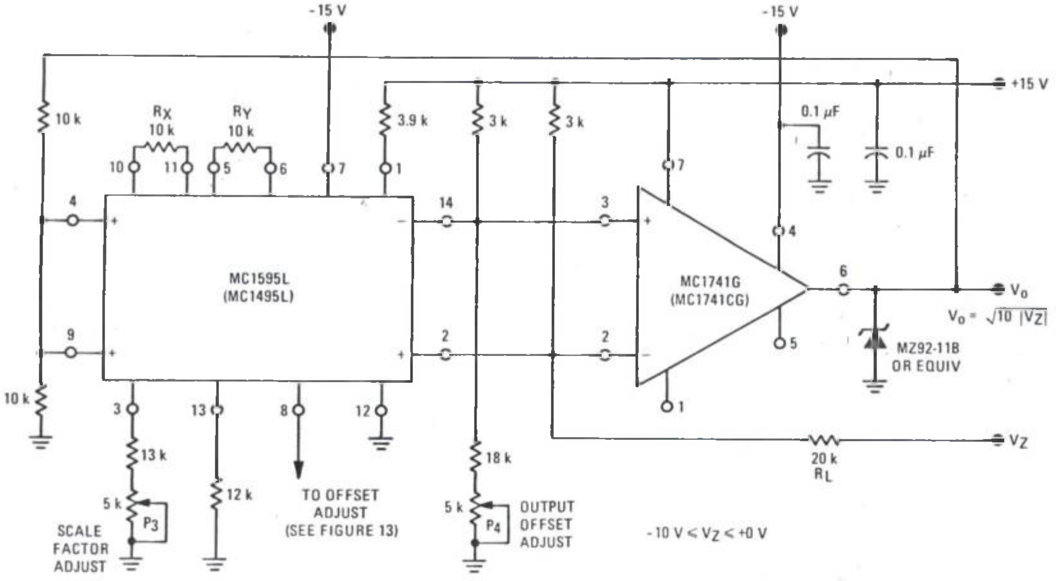
A potted multiplier can be used to obtain the double frequency component, but frequency would be limited by its internal level-shift amplifier. In the monolithic units, the amplifier is omitted.

In a typical doubler circuit, conventional ± 15-volt supplies are used. An input dynamic range of 5.0 volts peak-to-peak is allowed. The circuit generates wave-forms that are double frequency; less than 1% distortion is encountered without filtering. The configuration has been successfully used in excess of 200 kHz; reducing the scale factor by decreasing the load resistors can further expand the bandwidth.

A slightly modified version of the MC1595 (MC1495) – the MC1596 (MC1496) – has been successfully used as a doubler to obtain 400 MHz. (See Figure 28.)

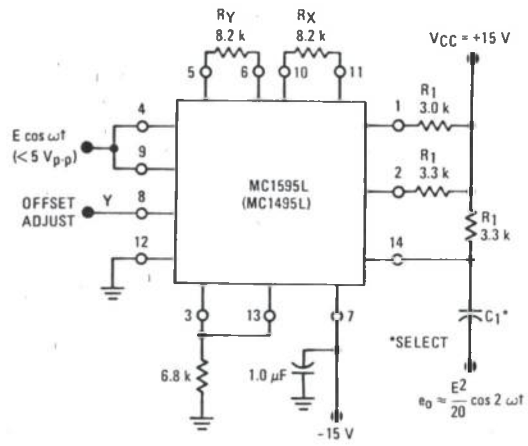
6.2 Figure 29 represents an application for the monolithic multiplier as a balanced modulator. Here, the audio input signal is 1.6 kHz and the carrier is 40 kHz.

FIGURE 27 – SQUARE ROOT CIRCUIT



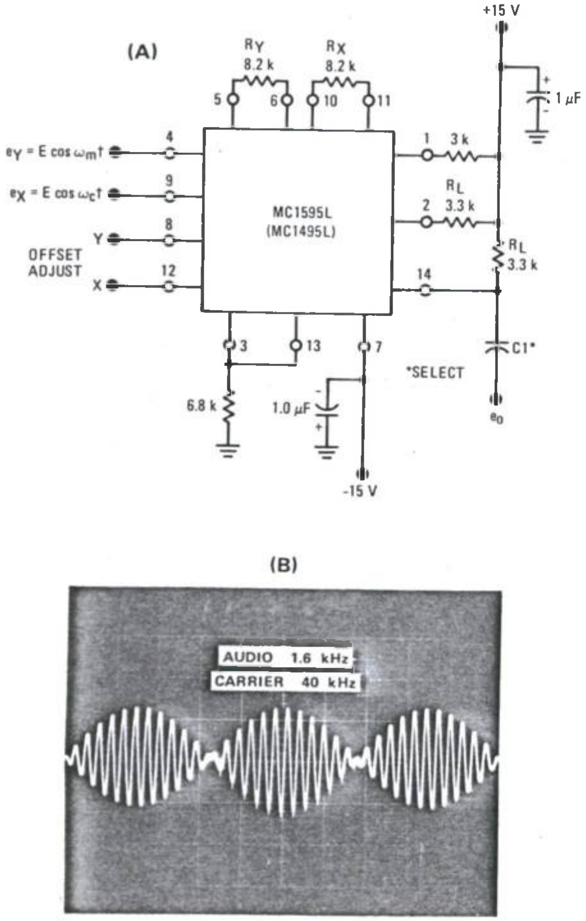
OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 28 – FREQUENCY DOUBLER



When two equal cosine waves are applied to X and Y, the result is a wave shape of twice the input frequency. For this example the input was a 10 kHz signal, output was 20 kHz.

FIGURE 29 – BALANCED MODULATOR



The defining equation for balanced modulation is

$$K(E_m \cos \omega_m t)(E_c \cos \omega_c t) =$$

$$\frac{KE_cE_m}{2}[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

where ω_c is the carrier frequency, ω_m is the modulator frequency and K is the multiplier gain constant.

AC coupling at the output eliminates the need for level translation or an operational amplifier; a higher operating frequency results.

A problem common to communications is to extract the intelligence from single-sideband received signal. The ssb signal is of the form

$$e_{ssb} = A \cos(\omega_c + \omega_m)t$$

and if multiplied by the appropriate carrier waveform, cos $\omega_c t$,

$$e_{ssb}e_{carrier} = \frac{AK}{2}[\cos(2\omega_c + \omega_m)t + \cos(\omega_c)t].$$

If the frequency of the band-limited carrier signal, ω_c, is ascertained in advance the designer can insert a low-pass filter and obtain the (AK/2) (cos $\omega_c t$) term with ease. He also can use an operational amplifier for a combination level shift-active filter, as an external component. But in potted multipliers, even if the frequency range can be covered, the operational amplifier is inside and not accessible, so the user must accept the level shifting provided, and still add a low-pass filter.

6.3 Amplitude Modulation

The multiplier performs amplitude modulation, similar to balanced modulation, when a dc term is added to the modulating signal with the Y offset adjust potentiometer. (See Figure 30.)

Here, the identity is

$$E_m(1 + m \cos \omega_m t) E_c \cos \omega_c t = KE_mE_c \cos \omega_c t +$$

$$\frac{KE_mE_cm}{2}[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

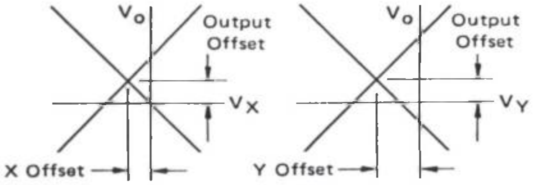
where m indicates the degree of modulation. Since m is adjustable, via potentiometer P_1, 100% modulation is possible. Without extensive tweaking, 96% modulation may be obtained where ω_c and ω_m are the same as in the balanced-modulator example.

6.4 Linear Gain Control

To obtain linear gain control, the designer can feed to one of the two MC1595 (MC1495) inputs a signal that will vary the unit's gain. The following example demonstrates the feasibility of this application. Suppose a 200 kHz sine wave, 1.0 volt peak-to-peak, is the signal to which a gain control will be added. The dynamic range of the control voltage V_C is 0 to +1.0 volt. These must be ascertained and the proper values of R_X and R_Y can be selected for optimum performance. For the 200-kHz operating frequency, load resistors of 100 ohms were chosen to broaden the operating bandwidth of the multiplier, but gain was sacrificed. It may be made up with an amplifier operating at the appropriate frequency. (See Figure 31.)

OPERATION AND APPLICATIONS INFORMATION (continued)

X, Y and Output Offset Voltages



For most dc applications, all three offset adjust potentiometers (P_1, P_2, P_4) will be necessary. One or more offset adjust potentiometers can be eliminated for ac applications (See Figures 28, 29, 30, 31).

If well regulated supply voltages are available, the offset adjust circuit of Figure 13 is recommended. Otherwise, the circuit of Figure 14 will greatly reduce the sensitivity to power supply changes.

4.2 Scale Factor

The scale factor, K, is set by P_3(Figure 21). P_3 varies I_3 which inversely controls the scale factor K. It should be noted that current I_3 is one-half the current through R_1. R_1 sets the bias level for Q_5, Q_6, Q_7, and Q_8 (See Figure 3). Therefore, to be sure that these devices remain active under all conditions of input and output swing, care should be exercised in adjusting P_3 over wide voltage ranges (see Section 3, General Design Procedure).

4.3 Adjustment Procedures

The following adjustment procedure should be used to null the offsets and set the scale factor for the multiply mode of operation. (See Figure 21)

1. X Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 4)
   (b) Connect "X" input (pin 9) to ground
   (c) Adjust X offset potentiometer, P_2, for an ac null at the output
2. Y Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 9)
   (b) Connect "Y" input (pin 4) to ground
   (c) Adjust "Y" offset potentiometer, P_1, for an ac null at the output
3. Output Offset
   (a) Connect both "X" and "Y" inputs to ground
   (b) Adjust output offset potentiometer, P_4, until the output voltage V_o is zero volts dc
4. Scale Factor
   (a) Apply +10 Vdc to both the "X" and "Y" inputs
   (b) Adjust P_3 to achieve + 10.00 V at the output.
5. Repeat steps 1 through 4 as necessary.

The ability to accurately adjust the MC1595 (MC1495) depends upon the characteristics of potentiometers P_1 through P_4. Multi-turn, infinite resolution potentiometers with low-temperature coefficients are recommended.

5. DC Applications

5.1 Multiply

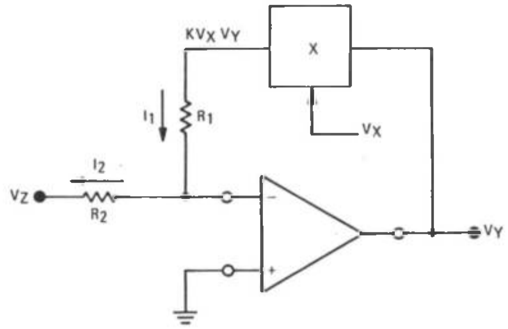
The circuit shown in Figure 21 may be used to multiply signals from dc to 100 kHz. Input levels to the actual multiplier are 5.0 V (max). With resistive voltage dividers the maximum could be very large – however, for this application two-to-one dividers have been used so that the maximum input level is 10 V. The maximum output level has also been designed for 10 V (max).

5.2 Squaring Circuit

If the two inputs are tied together, the resultant function is squaring; that is $V_o = KV^2$ where K is the scale factor. Note that all error terms can be eliminated with only three adjustment potentiometers, thus eliminating one of the input offset adjustments. Procedures for nulling with adjustments are given as follows:

1. AC Procedure:
   (a) Connect oscillator (1 kHz, 15 Vpp) to input
   (b) Monitor output at 2 kHz with tuned voltmeter and adjust P_3 for desired gain (be sure to peak response of the voltmeter)
   (c) Tune voltmeter to 1 kHz and adjust P_1 for a minimum output voltage
   (d) Ground input and adjust P_4 (output offset) for zero volts dc output
   (e) Repeat steps a through d as necessary.
2. DC Procedure:
   (a) Set $V_X = V_Y = 0$ V and adjust P_4 (output offset potentiometer) such that $V_o = 0.0$ Vdc
   (b) Set $V_X = V_Y = 1.0$ V and adjust P_1 (Y input offset potentiometer) such that the output voltage is +0.100 volts
   (c) Set $V_X = V_Y = 10$ Vdc and adjust P_3 such that the output voltage is +10.00 volts
   (d) Set $V_X = V_Y = -10$ Vdc. Repeat steps a through d as necessary.

FIGURE 24 – BASIC DIVIDE CIRCUIT



5.3 Divide Circuit

Consider the circuit shown in Figure 24 in which the multiplier is placed in the feedback path of an operational amplifier. For this configuration, the operational amplifier will maintain a "virtual ground" at the inverting (–) input. Assuming that the bias current of the operational amplifier is negligible, then $I_1 = I_2$ and

$$\frac{KV_XV_Y}{R1} = \frac{-V_Z}{R2} \tag{1}$$

Solving for V_Y,

$$V_Y = \frac{-R1}{R2\,K}\,\frac{V_Z}{V_X}. \tag{2}$$

If R1 = R2

$$V_Y = \frac{-V_Z}{KV_X} \tag{3}$$

If R1 = KR2

$$V_Y = \frac{-V_Z}{V_X}. \tag{4}$$

OPERATION AND APPLICATIONS INFORMATION (continued)

Hence, the output voltage is the ratio of V_Z to V_X and provides a divide function. This analysis is, of course, the ideal condition. If the multiplier error is taken into account, the output voltage is found to be

$$V_Y = -\left[\frac{R1}{R2\,K}\right]\frac{V_Z}{V_X} + \frac{\Delta E}{KV_X}, \qquad (5)$$

where ΔE is the error voltage at the output of the multiplier. From this equation, it is seen that divide accuracy is strongly dependent upon the accuracy at which the multiplier can be set, particularly at small values of V_Y. For example, assume that $R1 = R2$, and $K = 1/10$. For these conditions the output of the divide circuit is given by:

$$V_Y = \frac{-10\,V_Z}{V_X} + \frac{10\,\Delta E}{V_X}. \qquad (6)$$

From equation 6, it is seen that only when $V_X = 10$ V is the error voltage of the divide circuit as low as the error of the multiply circuit. For example, when V_X is small, (0.1 volt) the error voltage of the divide circuit can be expected to be a hundred times the error of the basic multiplier circuit.

In terms of percentage error,

$$\text{percentage error} = \frac{\text{error}}{\text{actual}} \times 100\%$$

or from equation (5),

$$\text{P.E.}_D = \frac{\dfrac{\Delta E}{KV_X}}{\left[\dfrac{R1}{R2\,K}\right]\dfrac{V_Z}{V_X}} = \left[\frac{R2}{R1}\right]\frac{\Delta E}{V_Z}. \qquad (7)$$

From equation 7, the percentage error is inversely related to voltage V_Z (i.e., for increasing values of V_Z, the percentage error decreases).

A circuit that performs the divide function is shown in Figure 25.

Two things should be emphasized concerning Figure 25.

1. The input voltage (V'_X) must be greater than zero and must be positive. This insures that the current out of pin 2 of the multiplier will always be in a direction compatible with the polarity of V_Z.
2. Pins 2 and 14 of the multiplier have been interchanged in respect to the operational amplifiers input terminals. In this instance, Figure 25 differs from the circuit connection shown in Figure 21; necessitated to insure negative feedback around the loop.

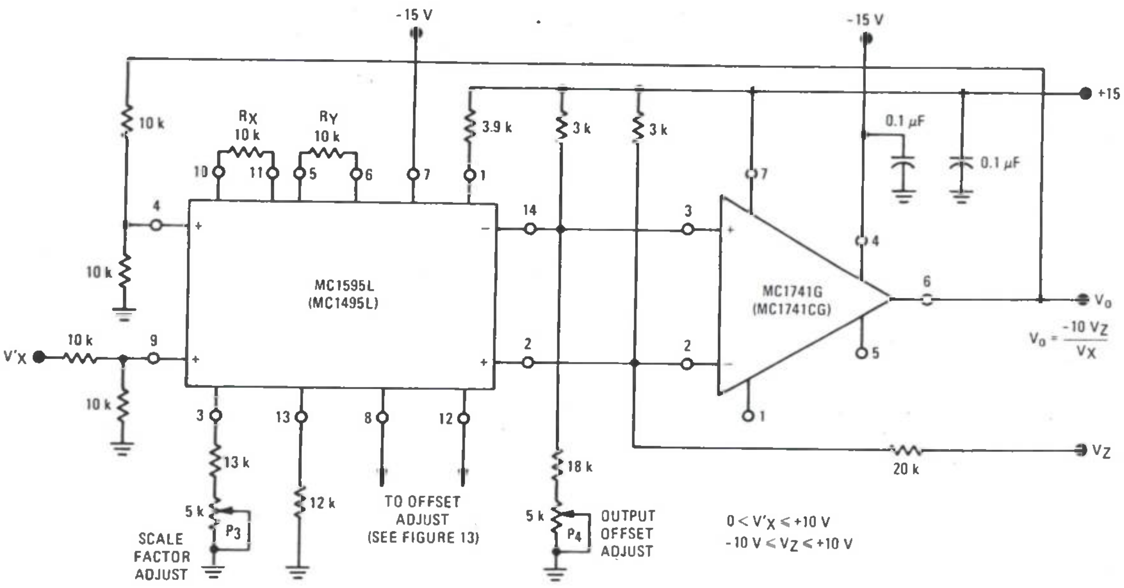
A Suggested Adjustment Procedure for the Divide Circuit

1. Set $V_Z = 0$ volts and adjust the output offset potentiometer (P_4) until the output voltage (V_o) remains at some (not necessarily zero) constant value as V_X' is varied between +1.0 volt and +10 volts.
2. Keep V_Z at 0 volts, set V_X' at +10 volts and adjust the Y input offset potentiometer (P_1) until $V_o = 0$ volts.
3. Let $V_X' = V_Z$ and adjust the X input offset potentiometer (P_2) until the output voltage remains at some (not necessarily − 10 volts) constant value as $V_Z = V_X'$ is varied between +1.0 and +10 volts.
4. Keep $V_X' = V_Z$ and adjust the scale factor potentiometer (P_3) until the average value of V_o is − 10 volts as $V_Z = V_X'$ is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

5.4 Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together is the square root function

FIGURE 25 – DIVIDE CIRCUIT



OPERATION AND APPLICATIONS INFORMATION (continued)

it can be seen that the resistor values necessary are given by:

$$R_{13} + 500\ \Omega = \frac{|V^{-}| - 0.7\ V}{I_{13}}$$

$$R_3 + 500\ \Omega = \frac{|V^{-}| - 0.7\ V}{I_3}$$

Let $V^{-} = -15\ V$

Then $R_{13} + 500 = \frac{14.3\ V}{1\ mA}$ or $R_{13} = 13.8\ k\Omega$

Let $R_{13} = 12\ k\Omega$

Similarly, $R_3 = 13.8\ k\Omega$

Let $R_3 = 15\ k\Omega$

However, for applications which require an accurate scale factor, the adjustment of R_3 and consequently, I_3, offers a convenient method of making a final trim of the scale factor. For this reason, as shown in Figure 21, resistor R_3 is shown as a fixed resistor in series with a potentiometer.

For applications not requiring an exact scale factor (balanced modulator, frequency doubler, AGC amplifier, etc.), pins 3 and 13 can be connected together and a single resistor from pin 3 to ground can be used. In this case, the single resistor would have a value of one-half the above calculated value for R_{13}.

Step 2. The next step is to select R_X and R_Y. To insure that the input transistors will always be active, the following conditions should be met:

$$\frac{V_X}{R_X} < I_{13} \qquad \frac{V_Y}{R_Y} < I_3.$$

A good rule of thumb is to make $I_3R_Y \geqslant 1.5\ V_{Y(max)}$ and $I_{13}\ R_X \geqslant 1.5\ V_{X(max)}$.

The larger the I_3R_Y and $I_{13}R_X$ product in relation to V_Y and V_X respectively, the more accurate the multiplier will be (see Figures 17 and 18).

Let $R_X = R_Y = 10\ k\Omega$

Then $I_3R_Y = 10\ V$

$I_{13}R_X = 10\ V$

since $V_{X(max)} = V_{Y(max)} = 5.0$ volts the value of $R_X = R_Y = 10\ k\Omega$ is sufficient.

Step 3. Now that R_X, R_Y and I_3 have been chosen, R_L can be determined:

$$K = \frac{2R_L}{R_XR_YI_3} = \frac{4}{10}$$

or $$\frac{(2)\ (R_L)}{(10\ k)\ (10\ k)\ (1\ mA)} = \frac{4}{10}$$

Thus $R_L = 20\ k\Omega$.

Step 4. To determine what power-supply voltage is necessary for this application, attention must be given to the circuit schematic shown in Figure 3. From the circuit schematic it can be seen that in order to maintain transistors Q_1, Q_2, Q_3 and Q_4 in an active region when the maximum input voltages are applied ($V_X' = V_Y' = 10$ V or $V_X = 5.0$ V, $V_Y = 5.0$ V), their respective collector voltage should be at least a few tenths of a volt higher than the maximum input voltage. It should also be noticed that the collector voltage of transistors Q_3 and Q_4 are at a potential which is two diode-drops below the voltage at pin 1. Thus, the voltage at pin 1 should be about two volts higher than the maximum input voltage. Therefore, to handle +5.0 volts at the inputs, the voltage at pin 1 must be at least +7.0 volts. Let $V_1 = 9.0$ Vdc.

Since the current following into pin 1 is always equal to $2I_3$, the voltage at pin 1 can be set by placing a resistor, R_1 from pin 1 to the positive supply:

$$R_1 = \frac{V^{+} - V_1}{2I_3}$$

Let $V^{+} = +15\ V$

Then $R_1 = \frac{15\ V - 9\ V}{(2)\ (1\ mA)}$

$R_1 = 3\ k\Omega$.

Note that the voltage at the base of transistors Q_5, Q_6, Q_7 and Q_8 is one diode-drop below the voltage at pin 1. Thus, in order that these transistors stay active, the voltage at pins 2 and 14 should be approximately halfway between the voltage at pin 1 and the positive-supply voltage. For this example, the voltage at pins 2 and 14 should be approximately 11 volts.

Step 5. Level Shifting

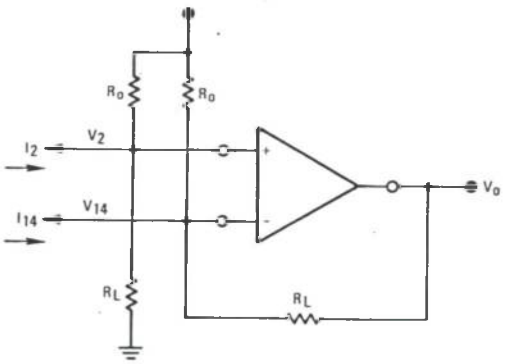
For dc applications, such as the multiply, divide and square-root functions, it is usually desirable to convert the differential output to a single-ended output voltage referenced to ground. The circuit shown in Figure 22 performs this function. It can be shown that the output voltage of this circuit is given by:

$$V_o = (I_2 - I_{14})\ R_L$$

And since $I_A - I_B = I_2 - I_{14} = \frac{2I_XI_Y}{I_3} = \frac{2\ V_XV_Y}{I_3R_XR_Y}$

Then $V_o = \frac{2R_LV_X'V_Y'}{4R_XR_XI_3}$ where $V_X'V_Y'$ is the voltage at the input to the voltage dividers.

FIGURE 22 – LEVEL SHIFT CIRCUIT



OPERATION AND APPLICATIONS INFORMATION (continued)

The choice of an operational amplifier for this application should have low bias currents, low offset current, and a high common-mode input voltage range as well as a high common-mode rejection ratio. The MC1556, and MC1741 operational amplifiers meet these requirements.

Referring to Figure 21, the level shift components will be determined. When $V_X = V_Y = 0$, the currents I_2 and I_{14} will be equal to I_{13}. In Step 3, R_L was found to be 20 kΩ and in Step 4, V_2 and V_{14} were found to be approximately 11 volts. From this information, R_o can be found easily from the following equation (neglecting the operational amplifiers bias current):

$$\frac{V_2}{R_L} + I_{13} = \frac{V^+ - V_2}{R_o}$$

And for this example, $\frac{11\ \text{V}}{20\ \text{k}\Omega} + 1\ \text{mA} = \frac{15\ \text{V} - 11\ \text{V}}{R_o}$

Solving for R_o, $R_o = 2.6\ \text{k}\Omega$

Thus, select $R_o = 3.0\ \text{k}\Omega$

For $R_o = 3.0\ \text{k}\Omega$, the voltage at pins 2 and 14 is calculated to be

$$V_2 = V_{14} = 10.4\ \text{volts.}$$

The linearity of this circuit (Figure 21) is likely to be as good or better than the circuit of Figure 5. Further improvements are possible as shown in Figure 23 where R_Y has been increased substantially to improve the Y linearity, and R_X decreased somewhat so as not to materially affect the X linearity, this avoids increasing R_L significantly in order to maintain a K of 0.1.

The versatility of the MC1595 (MC1495) allows the user to to optimize its performance for various input and output signal levels.

4. Offset and Scale Factor Adjustment

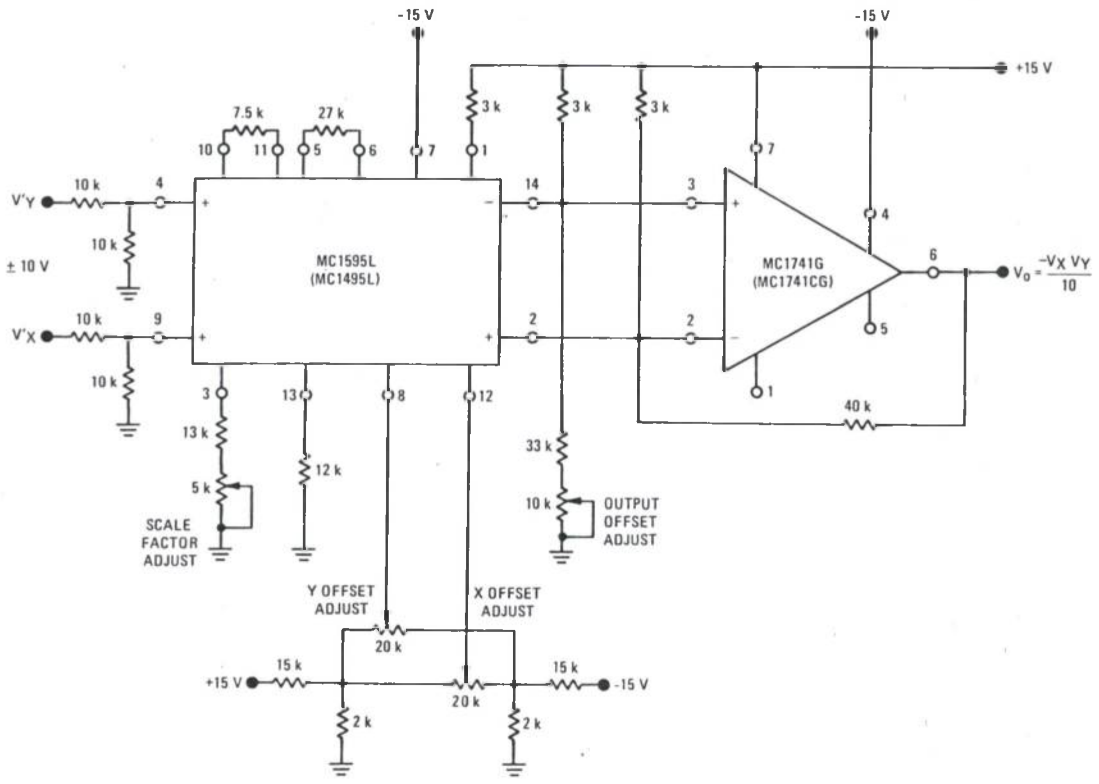
4.1 Offset Voltages

Within the monolithic multiplier (Figure 3) transistor base-emitter junctions are typically matched within 1 mV and resistors are typically matched within 2%. Even with this careful matching, an output error can occur. This output error is comprised of X-input offset voltage, Y-input offset voltage, and output-offset voltage. These errors can be adjusted to zero with the techniques shown in Figure 21. Offset terms can be shown analytically by the transfer function:

$$V_o = K(V_X \pm V_{IOX} \pm V_{X\,off})(V_Y \pm V_{IOY} \pm V_{Y\,off}) \pm V_{oo} \qquad (1)$$

Where K = scale factor
V_X = X input voltage
V_Y = Y input voltage
V_{IOX} = X input offset voltage
V_{IOY} = Y input offset voltage
$V_{X\,off}$ = X input offset adjust voltage
$V_{Y\,off}$ = Y input offset adjust voltage
V_{oo} = output offset voltage.

FIGURE 23 — MULTIPLIER WITH IMPROVED LINEARITY



OPERATION AND APPLICATIONS INFORMATION

1. Theory of Operation

The MC1595 (MC1495) is a monolithic, four-quadrant multiplier which operates on the principle of variable transconductance. The detailed theory of operation is covered in Application Note AN-489, Analysis and Basic Operation of the MC1595. The result of this analysis is that the differential output current of the multiplier is given by

$$I_A - I_B = \Delta I = \frac{2V_XV_Y}{R_XR_YI_3}$$

where I_A and I_B are the currents into pins 14 and 2, respectively, and V_X and V_Y are the X and Y input voltages at the multiplier input terminals.

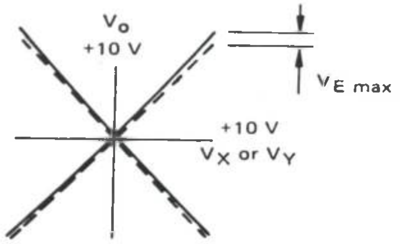
2. Design Considerations

2.1 General

The MC1595 (MC1495) permits the designer to tailor the multiplier to a specific application by proper selection of external components. External components may be selected to optimize a given parameter (e.g. bandwidth) which may in turn restrict another parameter (e.g. maximum output voltage swing). Each important parameter is discussed in detail in the following paragraphs.

2.1.1 Linearity, Output Error, E_{RX} or E_{RY}

Linearity error is defined as the maximum deviation of output voltage from a straight line transfer function. It is expressed as error in percent of full scale (see figure below).



For example, if the maximum deviation, $V_{E(max)}$, is ±100 mV and the full scale output is 10 volts, then the percentage error is

$$E_R = \frac{V_{E(max)}}{V_{o(max)}} \times 100 = \frac{100 \times 10^{-3}}{10} \times 100 = \pm 1.0\%.$$

Linearity error may be measured by either of the following methods:

1. Using an X — Y plotter with the circuit shown in Figure 5, obtain plots for X and Y similar to the one shown above.
2. Use the circuit of Figure 4. This method nulls the level shifted output of the multiplier with the original input. The peak output of the null operational amplifier will be equal to the error voltage, $V_{E(max)}$.

One source of linearity error can arise from large signal nonlinearity in the X and Y-input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that nonlinear base-emitter voltage variation can be ignored. Figures 17 and 18 show the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_3 = I_{13} = 1.0$ mA).

2.1.2 3 dB-Bandwidth and Phase Shift

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband operational amplifier should be used. Stray output capacitance will depend to a large extent on circuit layout.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector error of 5%.

2.1.3 Maximum Input Voltage

$V_{X(max)}$, $V_{Y(max)}$ maximum input voltages must be such that:

$$V_{X(max)} < I_{13} R_Y$$

$$V_{Y(max)} < I_3 R_Y.$$

Exceeding this value will drive one side of the input amplifier to "cutoff" and cause non-linear operation.

Currents I_3 and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then R_X and R_Y can be determined by considering the input signal handling requirements.

For $V_{X(max)} = V_{Y(max)} = 10$ volts;

$$R_X = R_Y > \frac{10\ \text{V}}{1.0\ \text{mA}} = 10\ \text{k}\Omega.$$

The equation $I_A - I_B = \dfrac{2V_XV_Y}{R_XR_YI_3}$

is derived from $I_A - I_B = \dfrac{2V_XV_Y}{\left(R_X + \dfrac{2kT}{qI_{13}}\right)\left(R_Y + \dfrac{2kT}{qI_3}\right) I_3}$

with the assumption $R_X \gg \dfrac{2kT}{qI_{13}}$ and $R_Y \gg \dfrac{2kT}{qI_3}$.

At $T_A = +25^\circ$C and $I_{13} = I_3 = 1$ mA,

$$\frac{2kT}{qI_{13}} = \frac{2kT}{qI_3} = 52\ \Omega.$$

Therefore, with $R_X = R_Y = 10\ \text{k}\Omega$ the above assumption is valid. Reference to Figure 19 will indicate limitations of $V_{X(max)}$ or $V_{Y(max)}$ due to V_1 and V_7. Exceeding these limits will cause saturation or "cutoff" of the input transistors. See Step 4 of Section 3 (General Design Procedure) for further details.

2.1.4 Maximum Output Voltage Swing

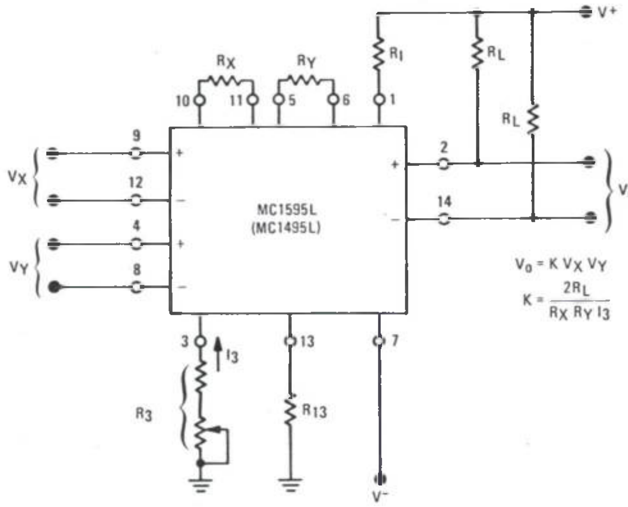
The maximum output voltage swing is dependent upon the factors mentioned below and upon the particular circuit being considered.

For Figure 20 the maximum output swing is dependent upon V^+ for positive swing and upon the voltage at pin 1 for negative swing. The potential at pin 1 determines the quiescent level for transistors Q_5, Q_6, Q_7, and Q_8. This potential

OPERATION AND APPLICATIONS INFORMATION (continued)

should be related so that negative swing at pins 2 or 14 does not saturate those transistors. See Section 3 for further information regarding selection of these potentials.

FIGURE 20 – BASIC MULTIPLIER



If an operational amplifier is used for level shift, as shown in Figure 21, the output swing (of the multiplier) is greatly reduced. See Section 3 for further details.

3. General Design Procedure

Selection of component values is best demonstrated by the following example: assume resistive dividers are used at the X and Y inputs to limit the maximum multiplier input to ±5.0 volts ($V_X = V_{Y[max]}$) for a ±10-volt input ($V_X' = V_Y'_{[max]}$). (See Figure 21). If an overall scale factor of 1/10 is desired, then

$$V_o = \frac{V_X' \, V_Y'}{10} = \frac{(2V_X)\,(2V_Y)}{10} = 4/10 \, V_X V_Y .$$

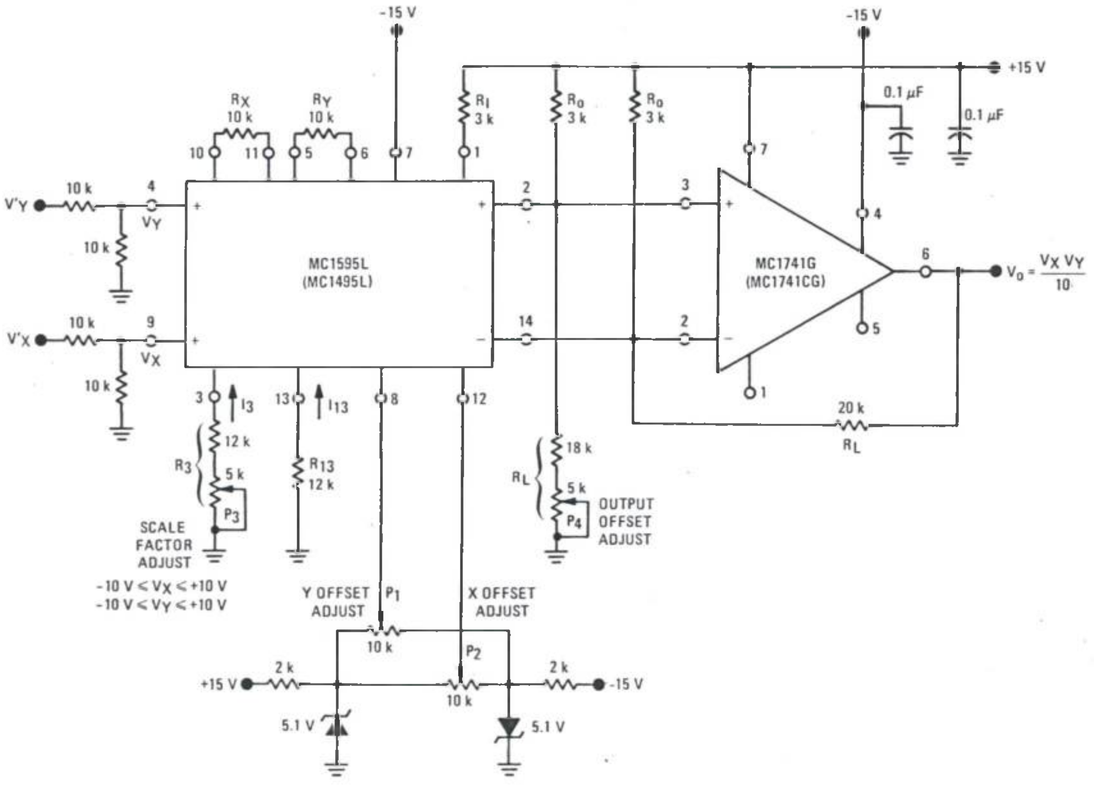
Therefore, K = 4/10 for the multiplier (excluding the divider network).

Step 1. The first step is to select current I_3 and current I_{13}. There are no restrictions on the selection of either of these currents except the power dissipation of the device. I_3 and I_{13} will normally be one or two milliamperes. Further, I_3 does not have to be equal to I_{13}, and there is normally no need to make them different. For this example, let

$$I_3 = I_{13} = 1 \text{ mA}.$$

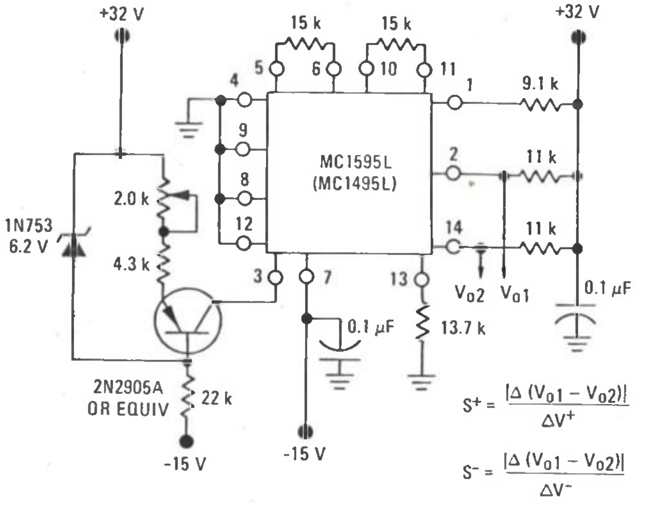
To set currents I_3 and I_{13} to the desired value, it is only necessary to connect a resistor between pin 13 and ground, and between pin 3 and ground. From the schematic shown in Figure 3,

FIGURE 21 – MULTIPLIER WITH OP-AMPL. LEVEL SHIFT



TEST CIRCUITS (continued)

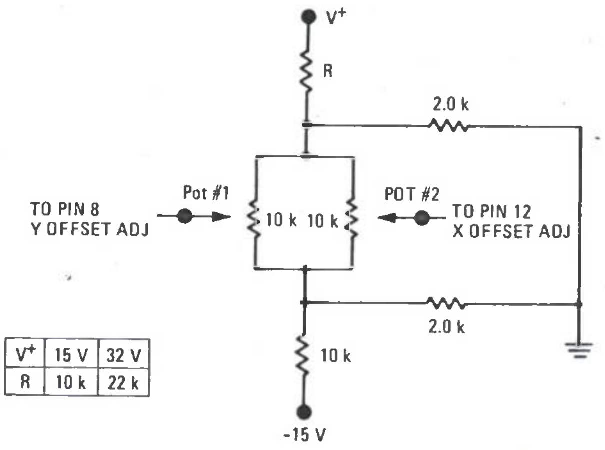
FIGURE 12 – POWER SUPPLY SENSITIVITY



$$S^{+} = \frac{|\Delta (V_{o1} - V_{o2})|}{\Delta V^{+}}$$

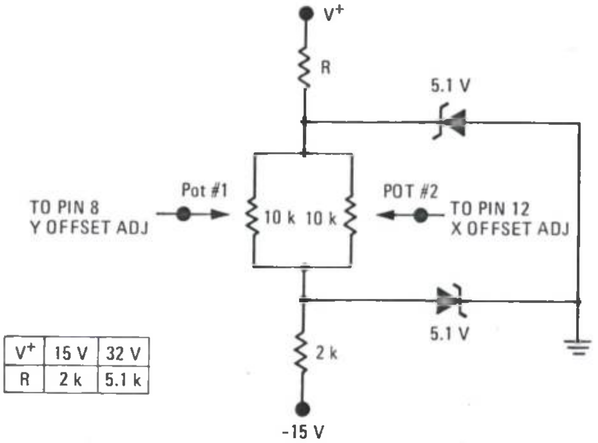
$$S^{-} = \frac{|\Delta (V_{o1} - V_{o2})|}{\Delta V^{-}}$$

FIGURE 13 – OFFSET ADJUST CIRCUIT

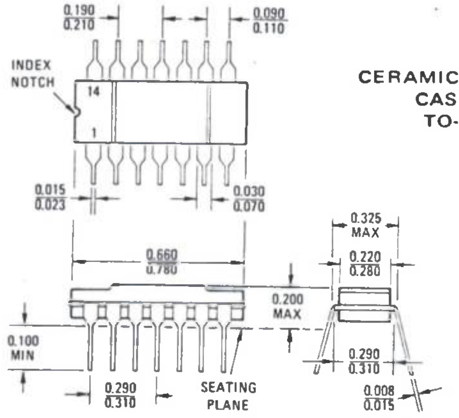


V^{+}	15 V	32 V
R	10 k	22 k

FIGURE 14 – OFFSET ADJUST CIRCUIT (ALTERNATE)



V^{+}	15 V	32 V
R	2 k	5.1 k



Weight ≈ 1.954 grams

CERAMIC PACKAGE
CASE 632
TO-116

OUTLINE DIMENSIONS

All JEDEC TO-116 dimensions and notes apply.

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

TYPICAL CHARACTERISTICS

FIGURE 15 – LINEARITY versus TEMPERATURE

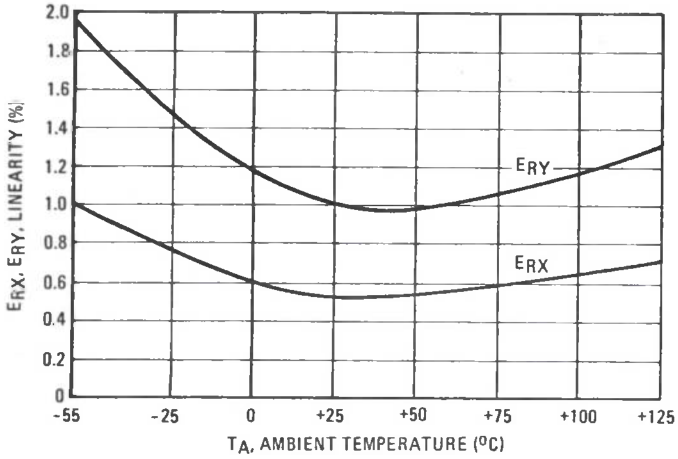


FIGURE 16 – SCALE FACTOR versus TEMPERATURE

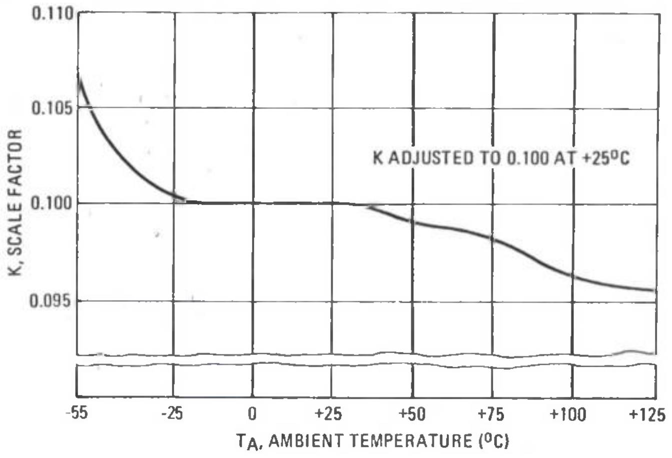


FIGURE 17 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

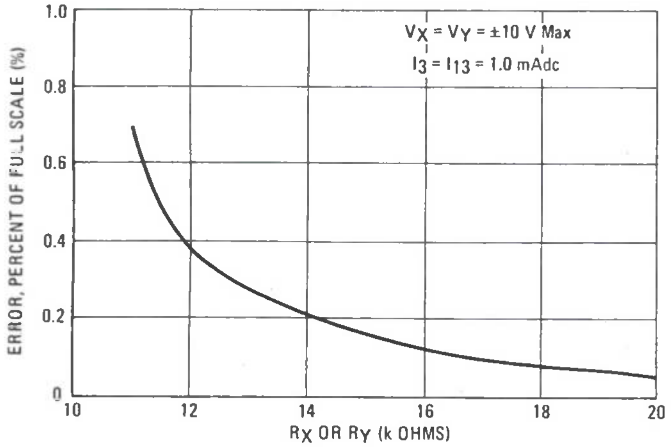


FIGURE 18 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

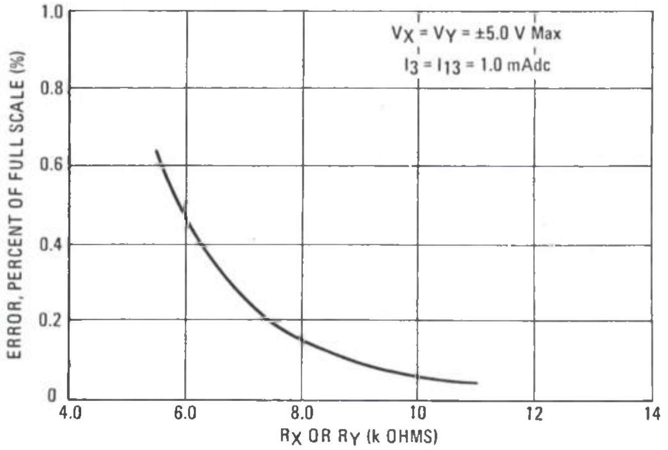
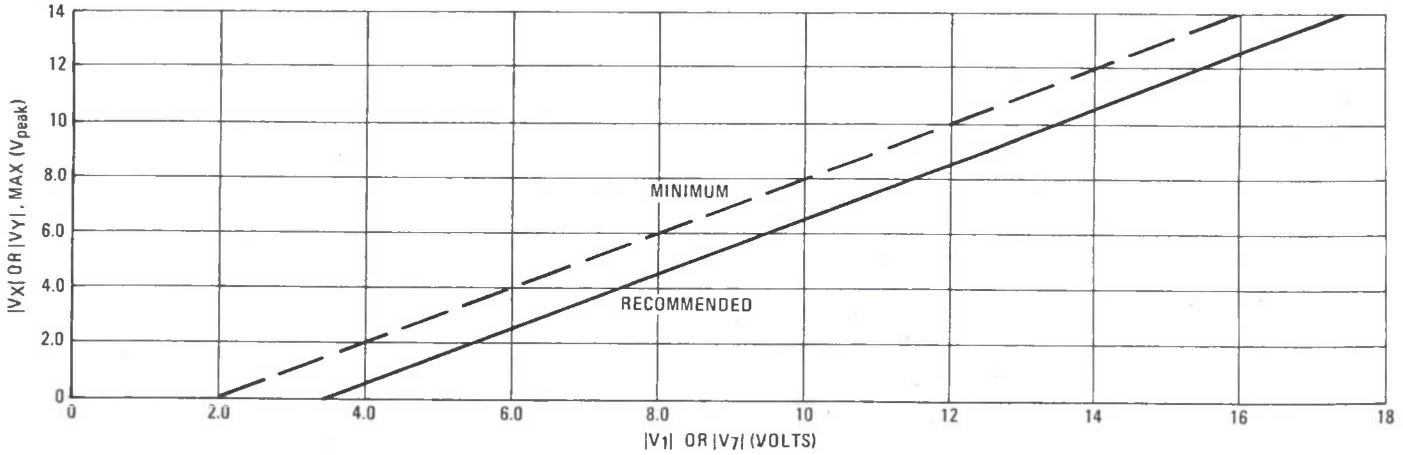


FIGURE 19 – MAXIMUM ALLOWABLE INPUT VOLTAGE versus VOLTAGE AT PIN 1 OR PIN 7

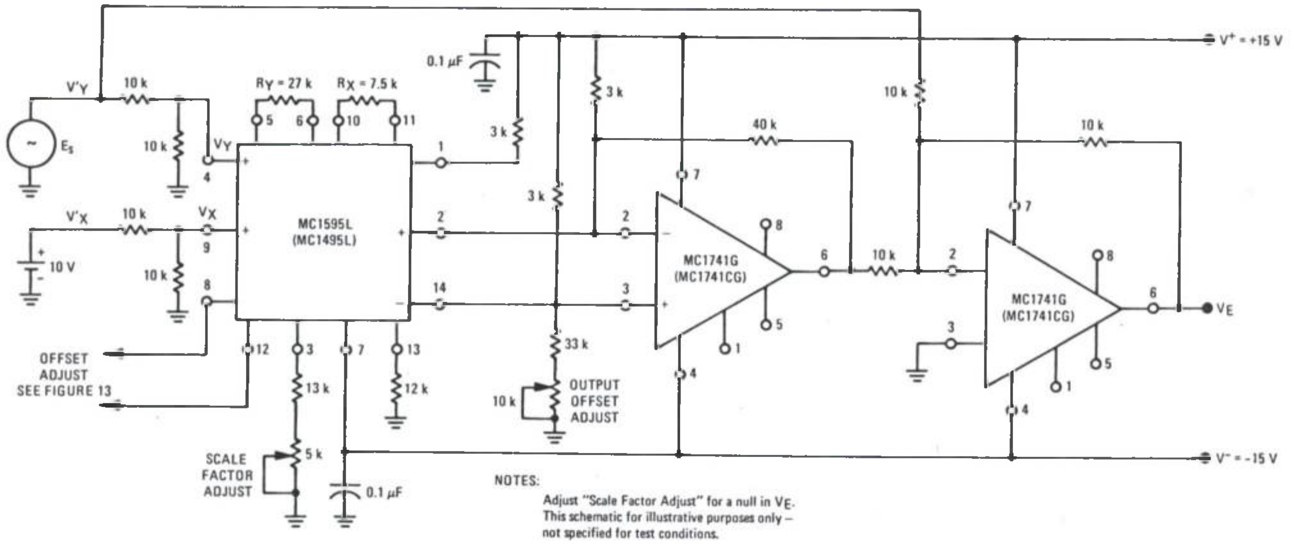


MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage (V_2-V_1, $V_{14}-V_1$, V_1-V_9, V_1-V_{12}, V_1-V_4, V_1-V_8, $V_{12}-V_7$, V_9-V_7, V_8-V_7, V_4-V_7)	ΔV	30	Vdc
Differential Input Signal	$V_{12}-V_9$ V_4-V_8	$\pm(6+I_{13}R_X)$ $\pm(6+I_3R_Y)$	Vdc Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	 750 5.0	 mW mW/°C
Operating Temperature Range MC1495 MC1595	T_A	 0 to +70 -55 to +125	°C °C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TEST CIRCUITS

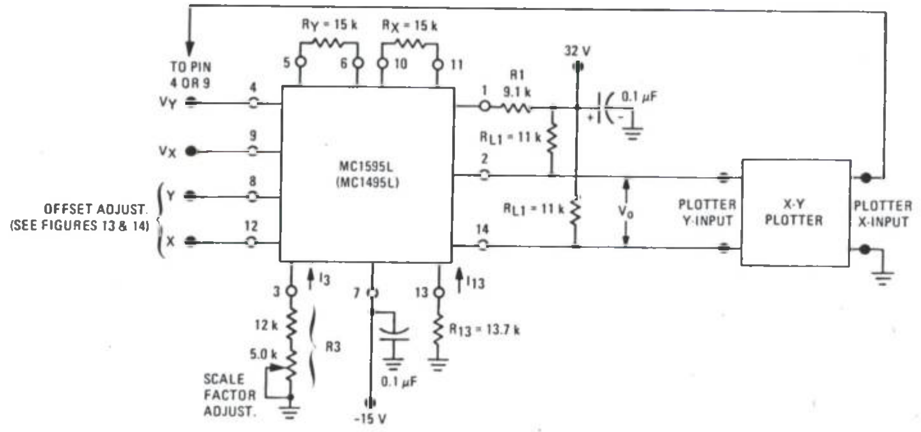
FIGURE 4 – LINEARITY (USING NULL TECHNIQUE)



NOTES:

Adjust "Scale Factor Adjust" for a null in V_E.
This schematic for illustrative purposes only – not specified for test conditions.

FIGURE 5 – LINEARITY (USING X-Y PLOTTER TECHNIQUE)



TEST CIRCUITS (continued)

FIGURE 6 – INPUT AND OUTPUT CURRENT

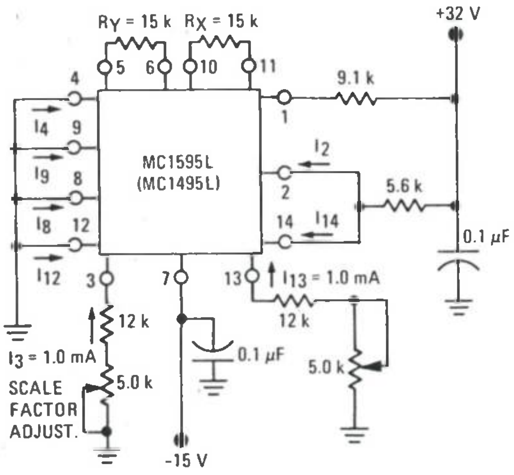


FIGURE 7 – INPUT RESISTANCE

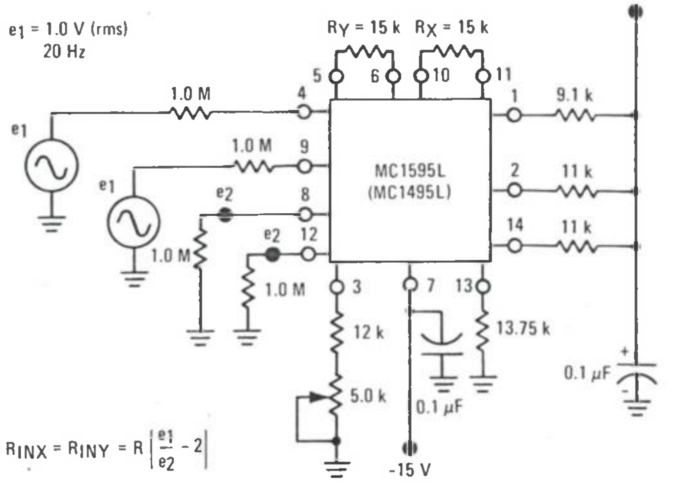


FIGURE 8 – OUTPUT RESISTANCE

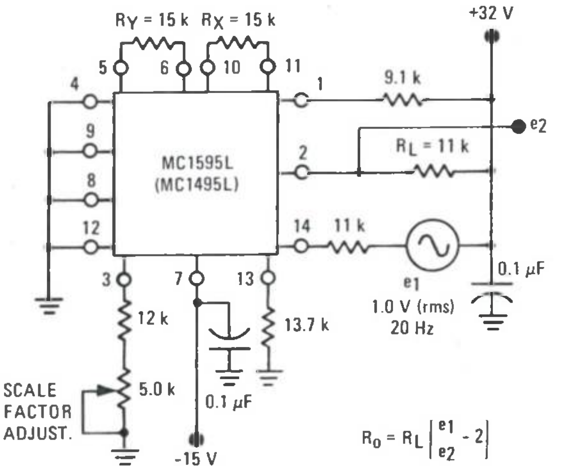


FIGURE 9 – BANDWIDTH (R_L = 11 kΩ)

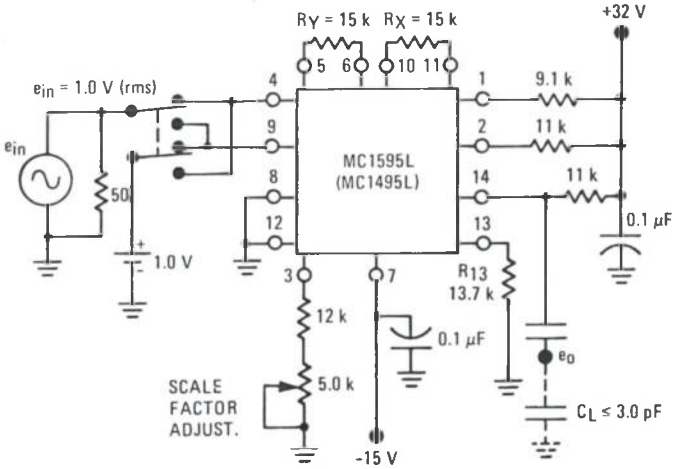


FIGURE 10 – BANDWIDTH (R_L = 50 Ω)

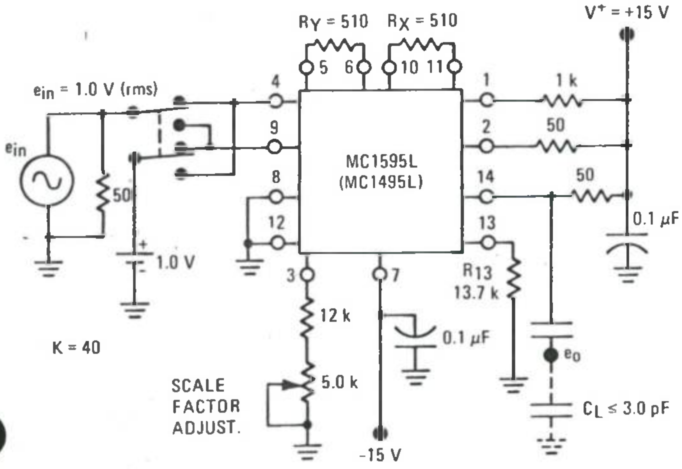
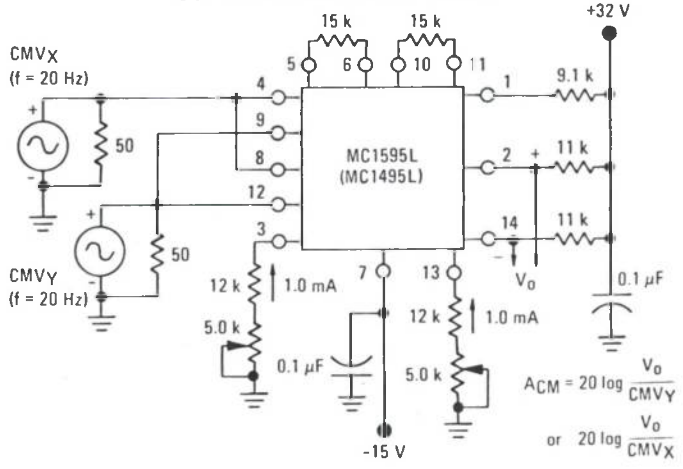
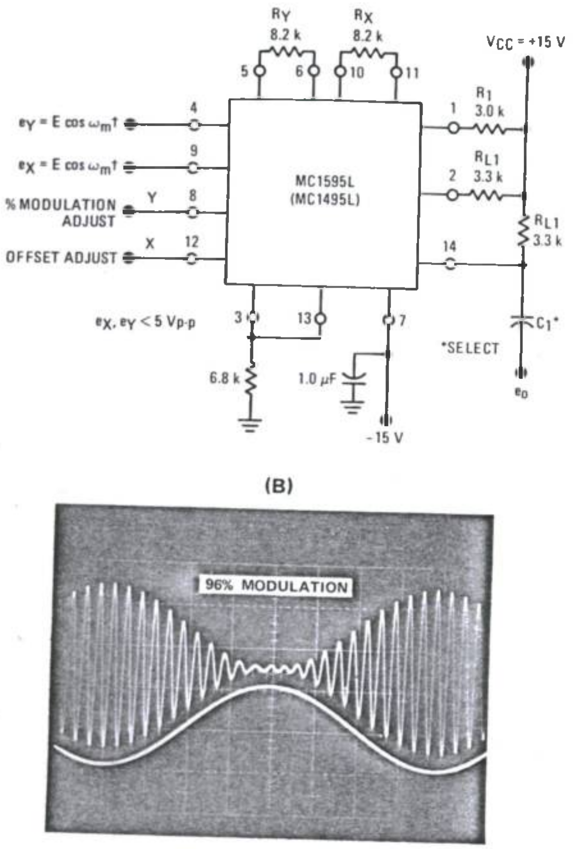


FIGURE 11 – COMMON-MODE GAIN and COMMON-MODE INPUT SWING



OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 30 – AMPLITUDE MODULATION



(B)

The signal is applied to the unit's Y input. Since the total input range is limited to 1.0 volt p-p, a 2.0-volt swing, a current source of 2.0 mA and an R_Y value of 1.0 kilohm is chosen. This takes best advantage of the dynamic range and insures linear operation in the Y-channel.

Since the X input varies between 0 and +1.0 volt, the current source selected was 1.0 mA and the R_X value chosen was 2.0 kilohms. This also insures linear operation over the X input dynamic range.

Choosing R_L = 100 assures wide-bandwidth operation. Hence, the scale factor for this configuration is

$$K = \frac{R_L}{R_X R_Y I_3}$$

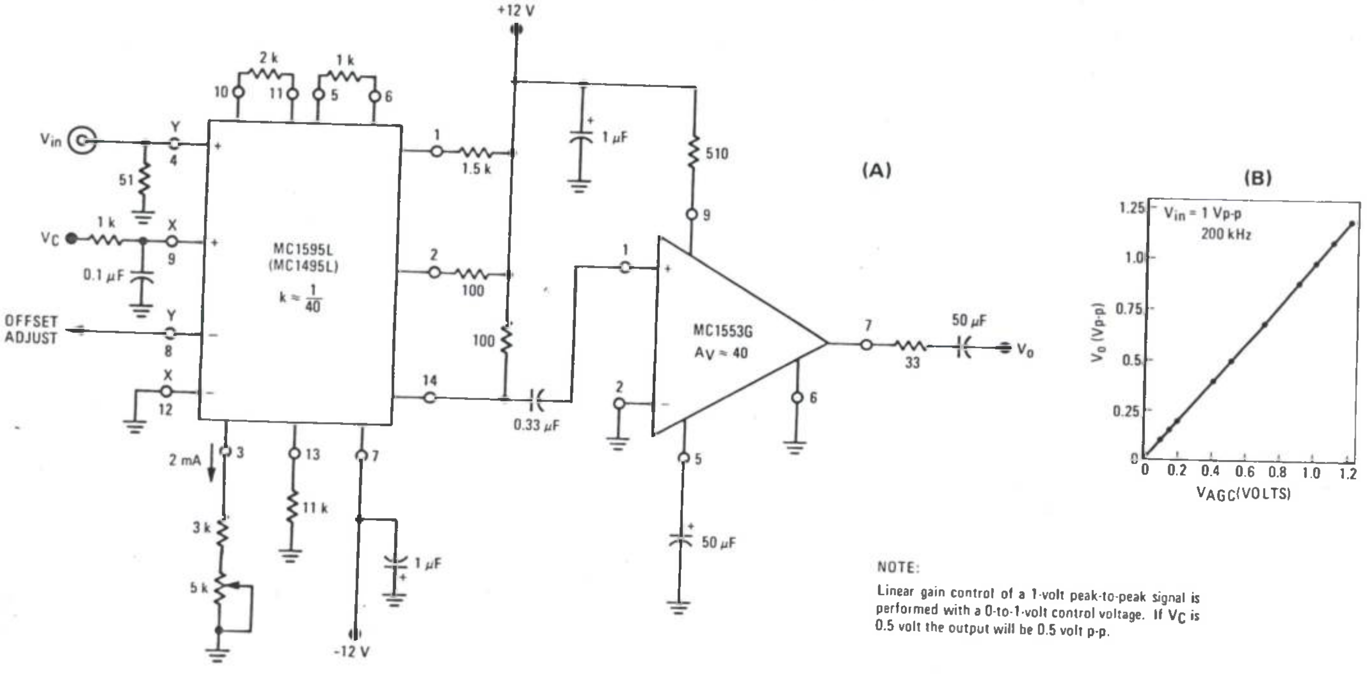
$$= \frac{100}{(2\ \text{k})(1\ \text{k})(2 \times 10^{+3})}\ V^{-1}$$

$$= \frac{1}{40}\ V^{-1}.$$

The 2 in the numerator of the equation is missing in this scale-factor expression because the output is single-ended and ac coupled.

To recover the gain, an MC1552 video amplifier with a gain of 40 is used. An operational amplifier also could have been used with frequency compensation to allow a gain of 40 at 200 kHz. The MC1539 operational amplifier can be tailored for this use; and the MC1520 operational amplifier does it directly.

FIGURE 31 – LINEAR GAIN CONTROL



NOTE:

Linear gain control of a 1-volt peak-to-peak signal is performed with a 0-to-1-volt control voltage. If V_C is 0.5 volt the output will be 0.5 volt p-p.

OPERATIONS AND APPLICATIONS INFORMATION INDEX

1. THEORY OF OPERATION

2. DESIGN CONSIDERATIONS
   - 2.1 General
   - 2.1.1 Linearity, Output Error, E_{RX} or E_{RY}
   - 2.1.2 3-dB Bandwidth and Phase Shift
   - 2.1.3 Maximum Input Voltage
   - 2.1.4 Maximum Output Voltage Swing

3. GENERAL DESIGN PROCEDURES

4. OFFSET AND SCALE FACTOR ADJUSTMENT
   - 4.1 Offset Voltages
   - 4.2 Scale Factor
   - 4.3 Adjustment Procedure

5. DC APPLICATIONS
   - 5.1 Multiply
   - 5.2 Squaring Circuit
   - 5.3 Divide Circuit
   - 5.4 Square Root

6. AC APPLICATIONS
   - 6.1 Frequency Doubler
   - 6.2 Balanced Modulator
   - 6.3 Amplitude Modulation
   - 6.4 Linear Gain Control

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DS 9124 R1

SYMBOL OF SW EXCELLENCE

STEWART-WARNER MICROCIRCUITS Division
STEWART-WARNER CORPORATION

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

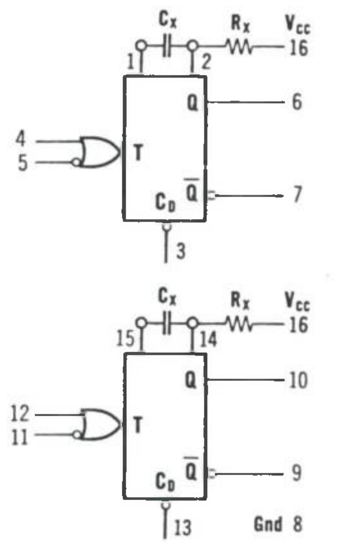
TTL 9602

The 9602 is a dual TTL Monostable Multivibrator with trigger mode selection, reset capability, rapid recovery, internally compensated reference levels and high speed capability. Output pulse duration and accuracy depend on external timing components, and are therefore under user control for each application.

It is well suited for a broad variety of applications, including pulse delay generators, square wave generators, long delay timers, pulse absence detectors, frequency detectors, clock pulse generators and fixed-frequency dividers.

Each input is provided with a clamp diode to limit undershoot and minimize ringing induced by fast fall times acting on system wiring impedances.

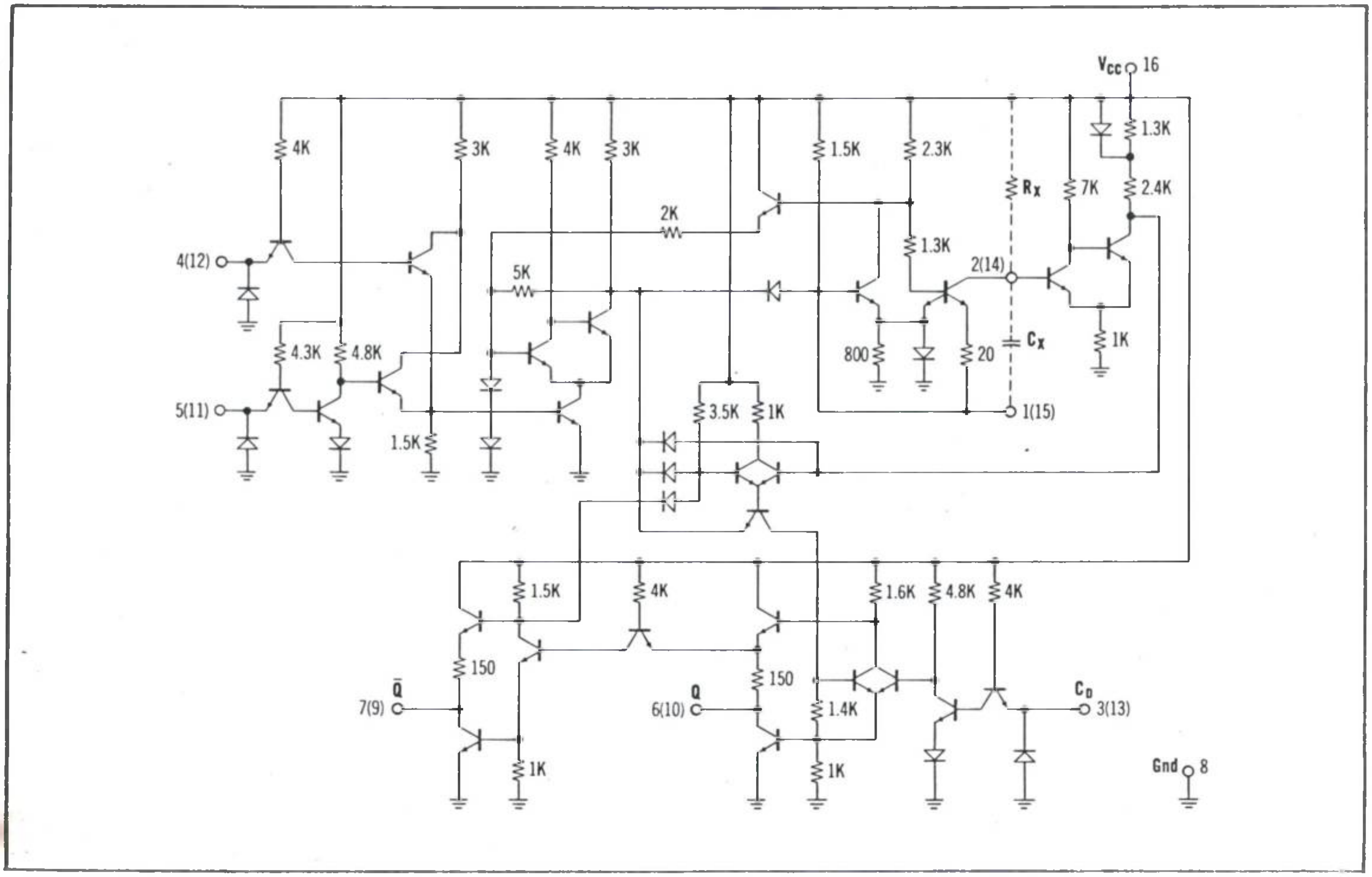
PIN ASSIGNMENTS



FEATURES

- RETRIGGERABLE, 0 to 100% duty cycle.
- D.C. LEVEL TRIGGERING, insensitive to transition times.
- COMPLEMENTARY INPUTS, for "leading edge" or "trailing edge" triggering.
- COMPLEMENTARY OUTPUTS, with active pull-ups for driving load capacitance.
- PULSE WIDTH COMPENSATION for V_{CC} and temperature variations.
- 50 nsec TO ∞ OUTPUT PULSE WIDTH RANGE.
- OPTIONAL RETRIGGER LOCK-OUT CAPABILITY.
- RESETTABLE, for interrupt operations.

SCHEMATIC (½ of circuit shown)



DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

ELECTRICAL CHARACTERISTICS 9602-1

T_A = −55°C to +125°C, V_{CC} = 5 V ±10%

CHARACTERISTIC	SYMBOL	CONDITIONS ①	−55°C MIN	−55°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+125°C MIN	+125°C MAX	UNIT
Output High Voltage	V_{OH}	V_{CC} = 4.5 V; I_{OH} = −1.0 mA ②	2.4		2.4	3.3		2.4		V
Output Low Voltage	V_{OL}	V_{CC} = 4.5 V; I_{OL} = 12.8 mA ②		0.4		0.2	0.4		0.4	V
Input High Voltage	V_{IH}	V_{CC} = 4.5 V ③	2.0		1.7			1.4		V
Input Low Voltage	V_{IL}	V_{CC} = 5.5 V ③		0.80			0.90		0.80	V
Input Load Current	I_F	V_{CC} = 5.5 V; V_F = 0.4 V		−1.6		−1.1	−1.6		−1.6	mA
Input Leakage Current	I_R	V_{CC} = 5.5 V; V_R = 4.5 V		60		15	60		60	μA
Short Circuit Current	I_{SC}	V_{CC} = 5.0 V; V_{OUT} = 1.0 V ②			− 8		−40			mA
Quiescent Power Supply Drain	I_{pd}	V_{CC} = 5.5 V; Ground pins 5 and 11		56			56		56	mA
Max. Allowable Wiring Capacitance	C_{STRAY}	Pin 2(14) to Ground		50			50		50	pf
Timing Resistor	R_X		5	25	5		50	5	50	KΩ

ELECTRICAL CHARACTERISTICS 9602-2

T_A = 0°C to +75°C, V_{CC} = 5 V ±5%

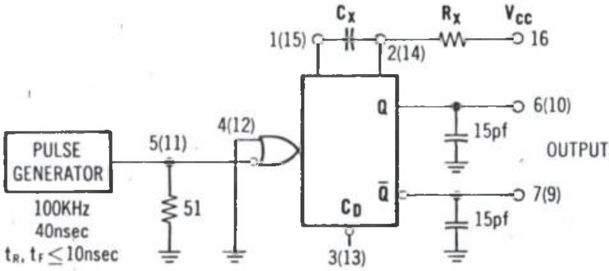
CHARACTERISTIC	SYMBOL	CONDITIONS ①	0°C MIN	0°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+75°C MIN	+75°C MAX	UNIT
Output High Voltage	V_{OH}	V_{CC} = 4.75 V; I_{OH} = −1.0 mA ②	2.4		2.4	3.4		2.4		V
Output Low Voltage	V_{OL}	V_{CC} = 4.75 V; I_{OL} = 12.8 mA ②		0.45		0.2	0.45		0.45	V
Input High Voltage	V_{IH}	V_{CC} = 4.75 V ③	1.9		1.8			1.6		V
Input Low Voltage	V_{IL}	V_{CC} = 5.25 V ③		0.85			0.85		0.85	V
Input Load Current	I_F	V_{CC} = 5.25 V; V_F = 0.45 V		−1.6		−1.0	−1.6		−1.6	mA
Input Leakage Current	I_R	V_{CC} = 5.25 V; V_R = 4.5 V		60		15	60		60	μA
Short Circuit Current	I_{SC}	V_{CC} = 5.0 V; V_{OUT} = 1.0 V ②			− 8		−40			mA
Quiescent Power Supply Drain	I_{pd}	V_{CC} = 5.25 V; Ground pins 5 and 11		56			56		56	mA
Max. Allowable Wiring Capacitance	C_{STRAY}	Pin 2(14) to Ground		50			50		50	pf
Timing Resistor	R_X		5	50	5		50	5	50	KΩ

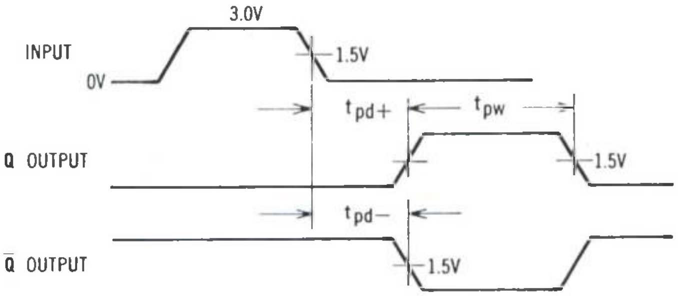
NOTES: ① Unless otherwise noted, 10KΩ resistor placed between Pin 2(14) and V_{CC}, for all tests. (R_X).

② Ground Pin 1(15) for V_{OL} @ Pin 7(9) or V_{OH} @ Pin 6(10) or I_{SC} @ Pin 6(10). Open Pin 1(15) for V_{OL} @ Pin 6(10) or V_{OH} @ Pin 7(9) or I_{SC} @ Pin 7(9).

③ Pulse test to determine V_{IH} and V_{IL} (minimum P.W. 40 ns).

DYNAMIC TEST SPECIFICATIONS



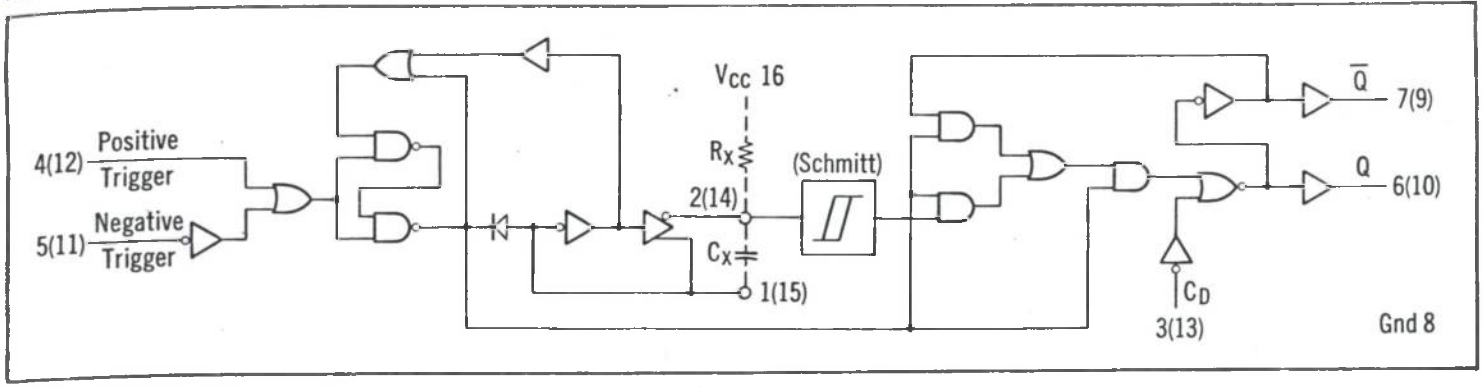


Note: Capacitance includes probe and jig.

V_{CC} = 5.0V, T_A = +25°C

CHARACTERISTIC	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	R_X KΩ	C_X pf
Negative Trigger Input to True Output	t_{pd+}		45	ns	5.0	0
Negative Trigger Input to Complement Output	t_{pd-}		35	ns	5.0	0
Minimum True Output Pulse Width	t_{pw}(min)		80	ns	5.0	0
Pulse Width Variation	t_{pw}	3.4	4.2	μs	10	1000

FUNCTIONAL BLOCK DIAGRAM



OPERATING NOTES

1. TRIGGERING — can be accomplished by a positive-going transition on pin 4(12) or a negative-going transition on pin 5(11). Triggering begins as a signal crosses the input V_{IL}:V_{IH} threshold region; this activates an internal latch whose unbalanced cross-coupling causes it to assume a preferred state. As the latch output goes low it disables the gates leading to the Q output and, through an inverter, turns on the capacitor discharge transistor. The inverted signal is also fed back to the latch input to change its state and effectively end the triggering action; thus the latch and its associated feedback perform the function of a differentiator.

The emitters of the latch transistors return to ground through an enabling transistor which must be turned off between successive triggers in order for the latch to proceed through the proper sequence when triggering is desired. Pin 5(11) must be high in order to trigger at pin 4(12); conversely, pin 4(12) must be low in order to trigger at pin 5(11).

2. RETRIGGERING — In a normal cycle, triggering initiates a rapid discharge of the external timing capacitor, followed by a ramp voltage run-up at pin 2(14). The delay will time out when the ramp voltage reaches the upper trigger point of a Schmitt circuit, causing the outputs to revert to the quiescent state. If another trigger occurs before the ramp voltage reaches the Schmitt threshold, the capacitor will be discharged and the ramp will start again without having disturbed the outputs. The delay period can therefore be extended for an arbitrary length of time by insuring that the interval between triggers is less than the delay time, as determined by the external capacitor and resistor.

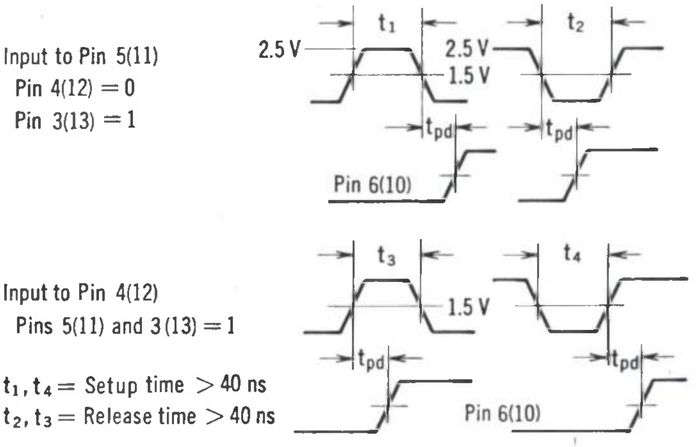
3. NON-RETRIGGERABLE OPERATION — Retriggering can be inhibited logically, by connecting pin 6(10) back to pin 4(12) or by connecting pin 7(9) back to pin 5(11). Either hook-up has the effect of keeping the latch-enabling transistor turned on during the delay period, which prevents the input latch from cycling as discussed above in the section on triggering.

4. OUTPUT PULSE WIDTH — An external resistor R_X and an external capacitor C_X are required, as shown in the logic diagram; to minimize stray capacitance and noise pickup, R_X and C_X should be located as close as possible to the circuit. In applications which require remote trimming of the pulse width, as with a variable resistor, R_X should consist of a fixed resistor in series with the variable resistor; the fixed resistor should be located as close as possible to the circuit. The output pulse width T is defined as follows, where R_X is in KΩ, C_X is in pf and T is in nanoseconds.

$$T = 0.35\, R_X C_X \left(1 + \frac{0.85}{R_X}\right) \text{ (for } C_X \geq 10^3 \text{ pf)}$$

The values of R_X may vary from 5.0K to 50K for 0° to +125°C operation, and 5.0K to 25K for −55° to +0°C operation. C_X may vary from 0 to any value.

5. SETUP AND RELEASE TIMES — The setup times listed below are necessary to allow the latch-enabling transistor to turn off and the node voltages within the input latch to stabilize, thus insuring proper cycling of the latch when the next trigger occurs. The indicated release times (equivalent to trigger duration) allow time for the input latch to cycle and its output signal to propagate.



t_1, t_4 = Setup time > 40 ns
t_2, t_3 = Release time > 40 ns

6. RESET OPERATION — A low signal on C_D, pin 3(13), will terminate an output pulse, causing Q to go low and Q̄ to go high. As long as C_D is held low, a delay period cannot be initiated nor will attempted triggering cause spikes at the outputs. A reset pulse duration, in the low state, of 25 nsec is sufficient to insure resetting. If the reset input goes low at the same time that a trigger transition occurs, the reset will dominate and the outputs will not respond to the trigger. If the reset input goes high coincident will a trigger transition, the circuit will respond to the trigger.

MAXIMUM RATINGS (beyond which device life may be impaired)

Vcc Pin Potential to Ground	−0.5V to +7.0V
Input Voltage (D.C.)	−0.5V to +5.5V
Input Current	−30 mA to +5.0 mA
Voltage Applied to Output when Output is High	0V to +Vcc value
Current Into Output when Output is Low	30 mA

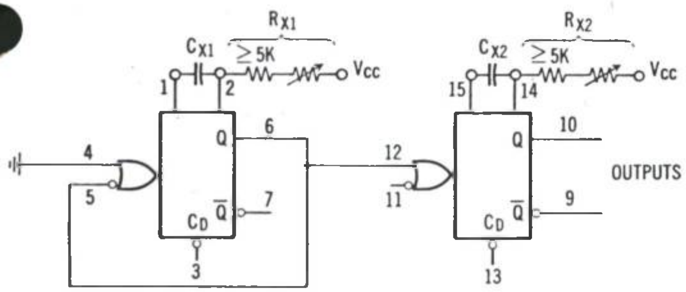
Operating Temperature Range (Military-1)	−55°C to +125°C
Operating Temperature Range (Industrial-2)	0°C to +75°C
Storage Temperature	−65°C to +150°C

9602

STEWART-WARNER MICROCIRCUITS

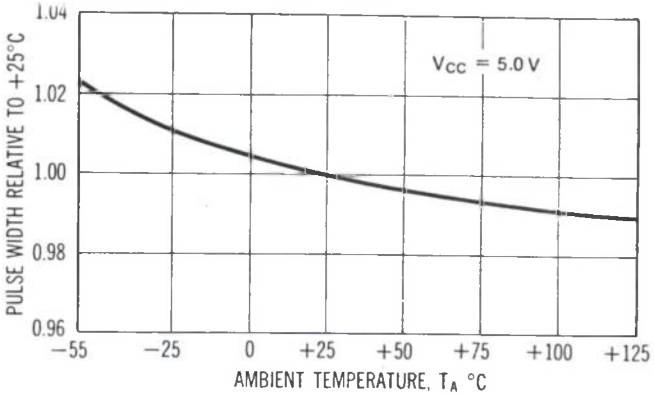
DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

PULSE GENERATOR



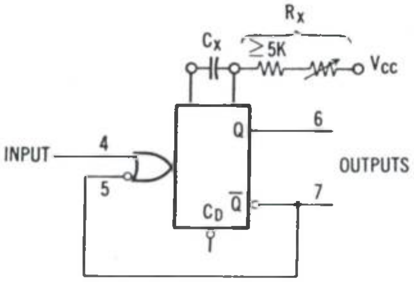
The first one-shot is hooked up in a free-running configuration, with a frequency determined by R_{X1} and C_{X1}. The second one-shot determines the output pulse width. If the $R_{X2} \times C_{X2}$ product exceeds $R_{X1} \times C_{X1}$, the second one-shot will be continually retriggered and its outputs will remain constant.

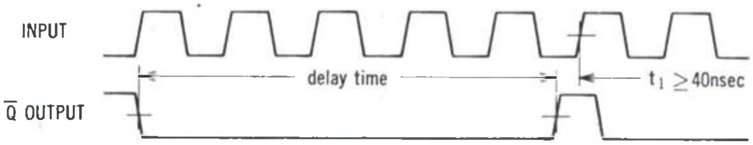
PULSE WIDTH VERSUS TEMPERATURE



With 10KΩ metal-film resistor and 1000 pf dipped mica capacitor, at the same ambient temperature as the device under test.

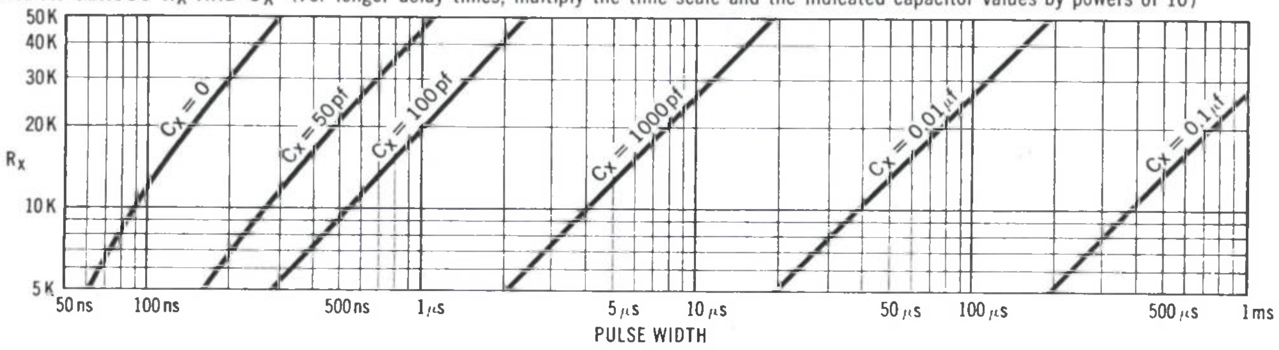
RETRIGGER LOCKOUT



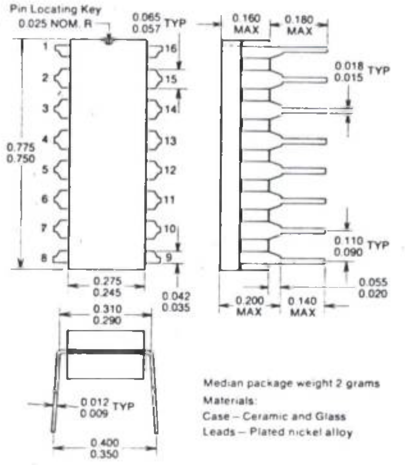


Feedback from pin 7 to pin 5 prevents retriggering by not allowing the triggering latch to re-cycle; connecting pin 6 to pin 4, with the trigger applied to pin 5, achieves the same effect. This same configuration can be used as a fixed-frequency divider or as a means of detecting when an input frequency exceeds some preselected value.

PULSE WIDTH VERSUS R_X AND C_X (For longer delay times, multiply the time scale and the indicated capacitor values by powers of 10)



PACKAGE DIMENSIONS
(IN INCHES)



Median package weight 2 grams

Materials:

Case – Ceramic and Glass

Leads – Plated nickel alloy

Printed in U.S.A.

GENERAL INSTRUMENT

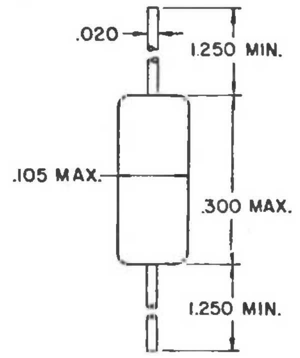
HIGH POWER GLASS SILICON DIODES

1N645
thru
1N649

PRV RANGE
225 Volts to 600 Volts
CURRENT
400 mA at 25°C.
150 mA at 150°C

FEATURES

- Glass, hermetically sealed
- Diffused junction construction
- Available to most current JAN specifications
- Wide temperature range
- High efficiency and rectification ratio
- Ideally suited for miniaturized equipment



DO-7

MECHANICAL DATA

Case	DO-7, Glass, hermetically sealed
Terminals	Tinned axial leads
Mounting Position	Any
Polarity	Color band denotes cathode end
Weight	.007 ounces
Operating Temperature	−65°C to +175°C
Storage Temperature	−65°C to +200°C

ELECTRICAL DATA

TYPE NO.	MAXIMUM RATINGS			ELECTRICAL CHARACTERISTICS				
	PRV	MAXIMUM AVERAGE RECTIFIED CURRENT mA*		MINIMUM SATURATION VOLTAGE at 100°C	MAXIMUM REVERSE CURRENT at PRV μA			MAX FWD VOLTAGE DROP at 400 mA DC at 25°C
	VOLTS	at 25°C	at 150°C	VOLTS	25°C	100°C	150°C	VOLTS
1N645	225	400	150	275	0.2	15		1.0
★1N645	225	400	150	275	0.025		15	1.0
1N646	300	400	150	360	0.2	15		1.0
1N647	400	400	150	480	0.2	20		1.0
★1N647	400	400	150	480	0.025		15	1.0
1N648	500	400	150	600	0.2	20		1.0
1N649	600	400	150	720	0.2	20		1.0
★1N649	600	400	150	720	0.050		25	1.0

* Resistive or Inductive Load
★ MIL-S-19500/240 B Types

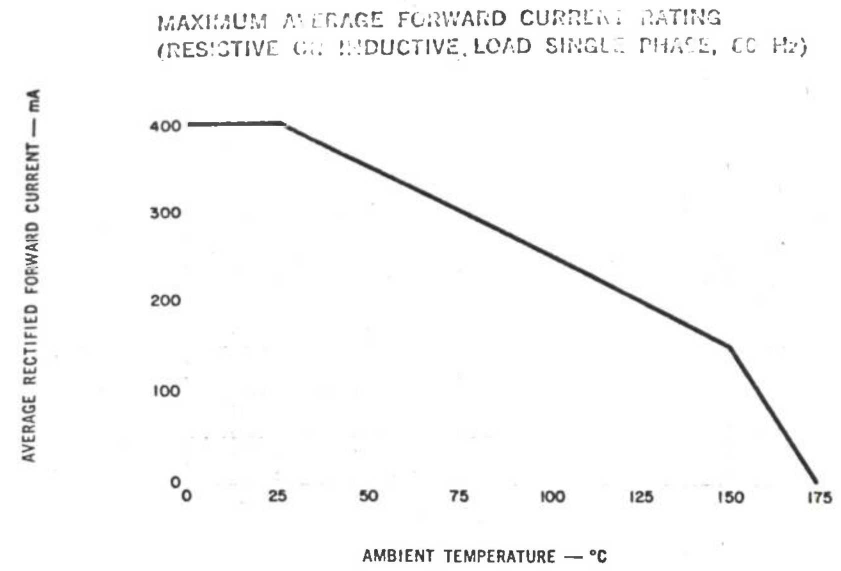


Fig. 1

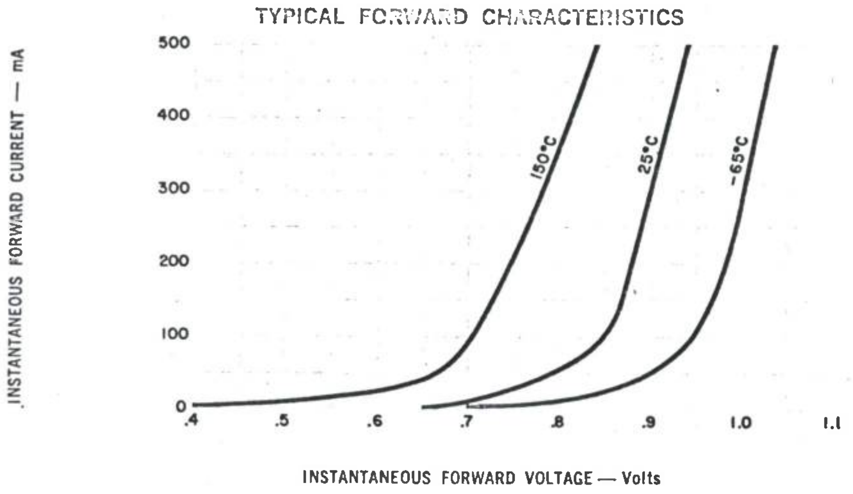


Fig. 2

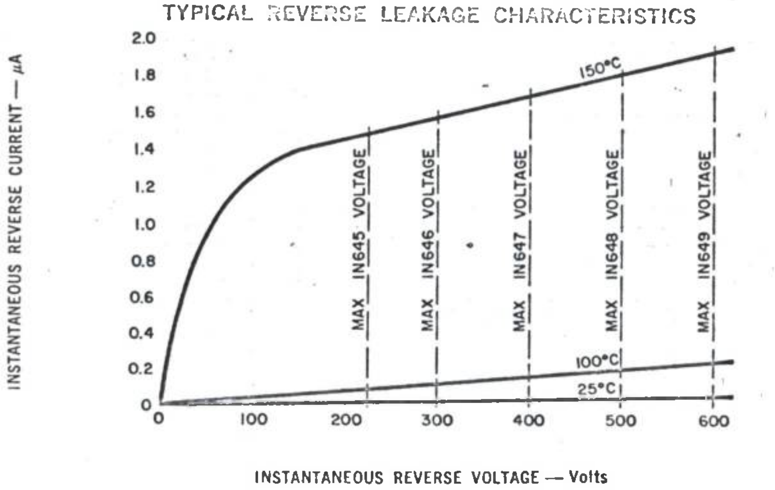


Fig. 3

GENERAL INSTRUMENT CORPORATION

[illegible]

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Western Area Sales Headquarters, 6108 West Venice Blvd., Los Angeles, Calif. 90034, (213) WE 3-7261

RECTIFIER
DIVISION

65 Gouverneur Street
Newark, New Jersey 07104
(201) 485-2100

MOTOROLA
BOX 955 • PHOENIX, ARIZONA 85001

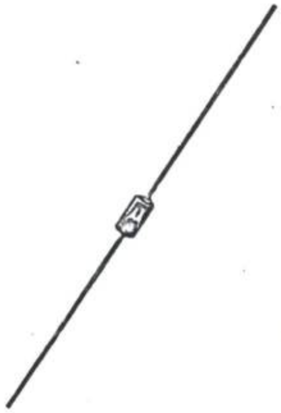
Data Sheet

1N4001 thru 1N4007

LEAD MOUNTED SILICON RECTIFIERS

50-1000 VOLTS
DIFFUSED JUNCTION

MARCH 1967 — DS 6015 R1
(Replaces DS 6015)



SILICON RECTIFIERS
1N4001 thru 1N4007
DS 6015 R1

"SURMETIC"† RECTIFIERS

. . . subminiature size, axial lead mounted rectifiers for general purpose low-power applications.

Designers Data for "Worst Case" Conditions

The Designers† Data Sheets permit the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MAXIMUM RATINGS

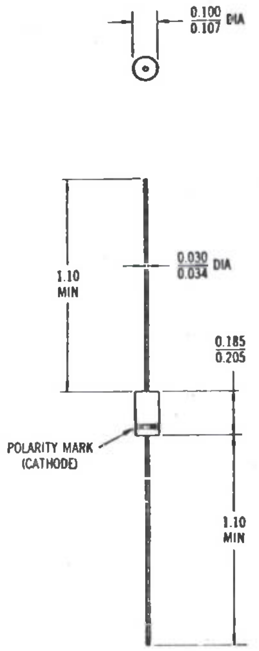
Characteristic	Symbol	1N4001	1N4002	1N4003	1N4004	1N4005	1N4006	1N4007	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	$V_{RM(rep)}$ $V_{RM(wkg)}$ V_R	50	100	200	400	600	800	1000	Volts
Non-Repetitive Peak Reverse Voltage (halfwave, single phase, 60 Hz peak)	$V_{RM(non-rep)}$	60	120	240	480	720	1000	1200	Volts
RMS Reverse Voltage	V_r	35	70	140	280	420	560	700	Volts
Average Rectified Forward Current (single phase, resistive load, 60 Hz, see Figure 6, T_A = 75°C)	I_O	1.0							Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, see Figure 2)	$I_{FM(surge)}$	30 (for 1 cycle)							Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175							°C

ELECTRICAL CHARACTERISTICS

Characteristic and Conditions	Symbol	Max	Unit
Maximum Instantaneous Forward Voltage Drop (i_F = 1.0 Amp. T_J = 25°C) Figure 1	V_F	1.1	Volts
Maximum Full-Cycle Average Forward Voltage Drop (I_O = 1.0 Amp, T_L = 75°C, 1 inch leads)	$V_{F(AV)}$	0.8	Volts
Maximum Reverse Current (rated dc voltage) T_J = 25°C T_J = 100°C	I_R	0.01 0.05	mA
Maximum Full-Cycle Average Reverse Current (I_O = 1.0 Amp. T_L = 75°C, 1 inch leads)	$I_{R(AV)}$	0.03	mA

MECHANICAL CHARACTERISTICS

CASE: Void free, Transfer Molded
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 350°C, 3/8" from case for 10 seconds at 5 lbs. tension
FINISH: All external surfaces are corrosion-resistant, leads are readily solderable
POLARITY: Cathode indicated by color band
WEIGHT: 0.40 Grams (approximately)



CASE 59

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† Trademark of Motorola Inc.

FIGURE 1 — FORWARD VOLTAGE

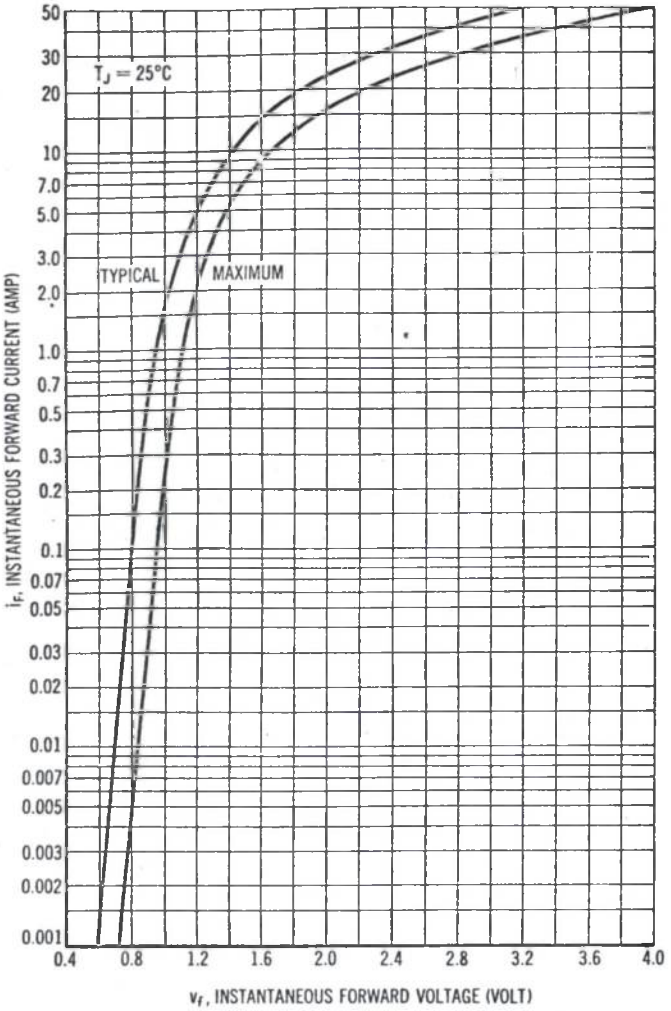


FIGURE 2 — MAXIMUM SURGE CAPABILITY

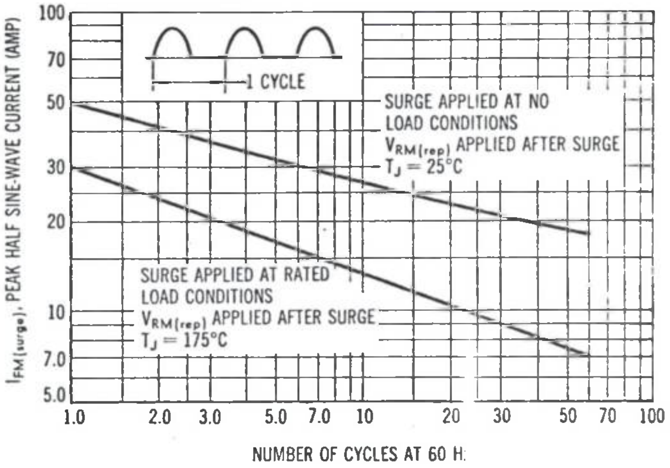


FIGURE 3 — FORWARD VOLTAGE TEMPERA URE COEFFICIENT

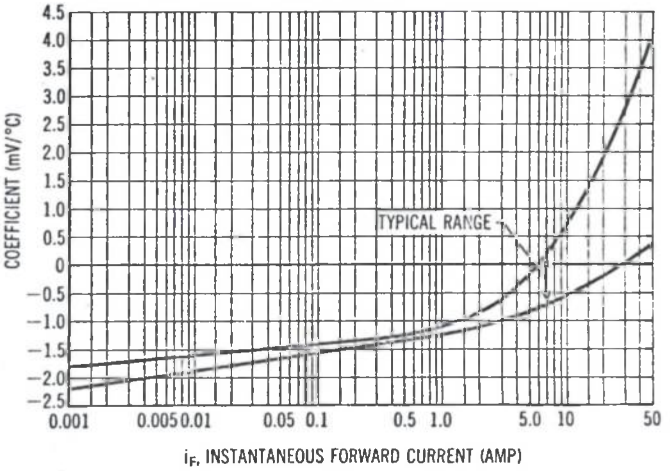
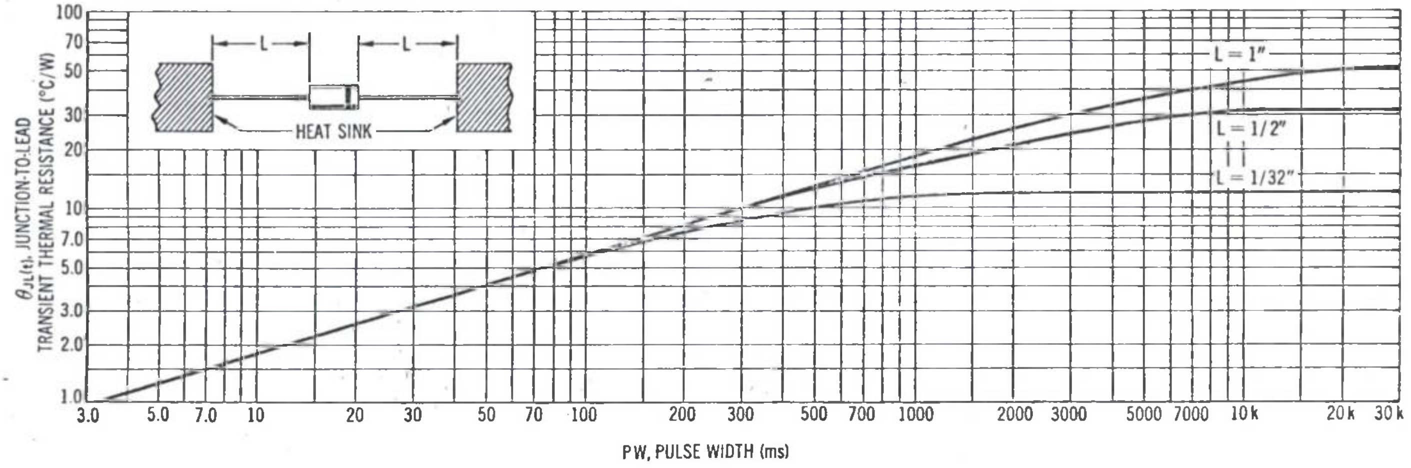


FIGURE 4 — TYPICAL TRANSIENT THERMAL RESISTANCE



FOR $\theta_{JL(t)}$ VALUES AT PULSE WIDTHS LESS THAN 3.0 ms, THE ABOVE CURVE CAN BE EXTRAPOLATED DOWN TO 10 μs AT A CONTINUING SLOPE OF 1/2

CURRENT DERATING DATA

FIGURE 5 — LEAD TEMPERATURE DERATING (DC ONLY)

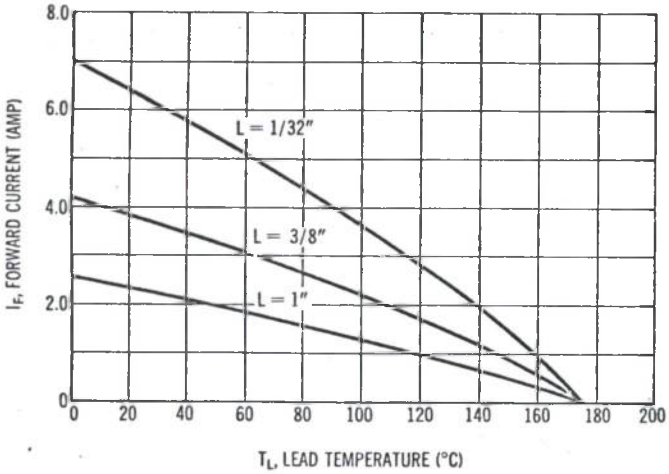


FIGURE 6 — RESISTIVE,INDUCTIVE LOADS

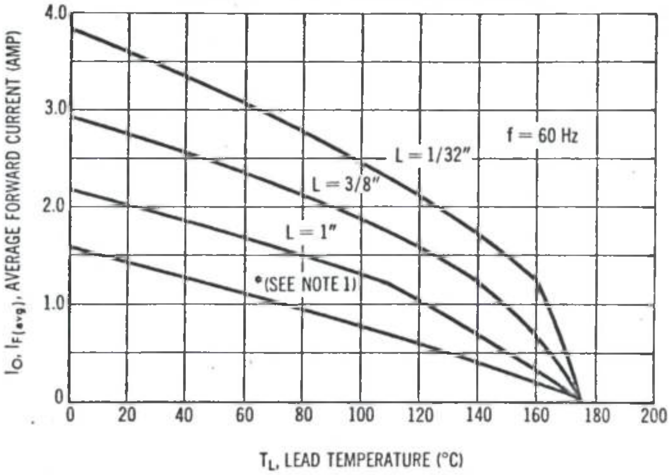


FIGURE 7 — CAPACITIVE LOADS

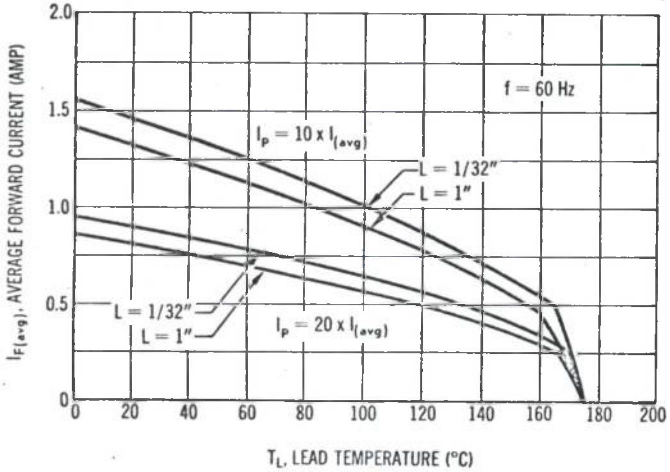
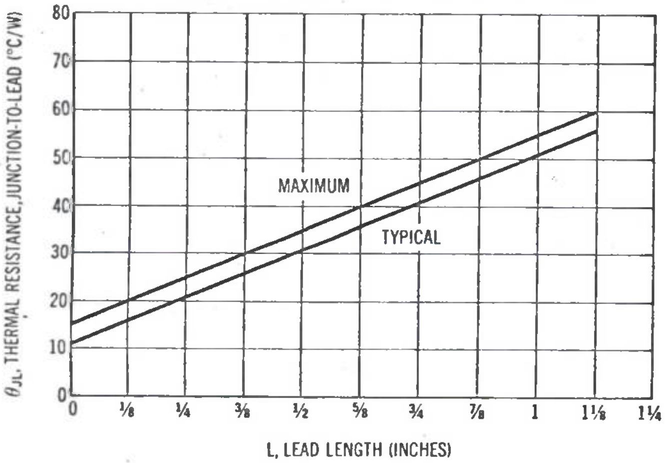


FIGURE 8 — STEADY-STATE THERMAL RESISTANCE

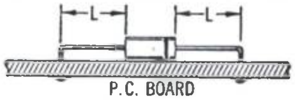


NOTES

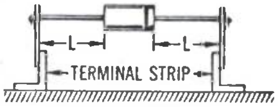
NOTE 1

Data shown for thermal resistance junction-to-ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR θ_{JA} IN STILL AIR



MOUNTING METHOD 1

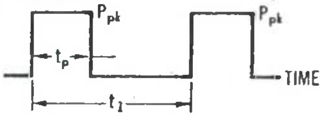


MOUNTING METHOD 2

MOUNTING METHOD	LEAD LENGTH, L (IN.)			θ_{JA}
	1/32	3/8	1	
1	—	75	85	°C/W
2	55	72	85	°C/W

*Using Mounting Method 1 or 2 with L = 1″ the curve marked * in Figure 6 can be used for 60 Hz half-wave resistive/inductive load (Rating vs. Ambient Temperature). The abscissa of Figure 6 then indicates T_A in °C.

NOTE 2



DUTY CYCLE, $D = t_p/t_1$

PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the lead should be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by:

$$T_J = T_L + \Delta T_{JL},$$

where ΔT_{JL} is the increase in junction temperature above the lead temperature. It may be determined by:

$$\Delta T_{JL} = P_{pk} \left[\theta_{JL(\infty)} \cdot D + (1 - D) \cdot \theta_{JL(t_1 + t_p)} + \theta_{JL(t_p)} - \theta_{JL(t_1)} \right]$$

where $\theta_{JL(t)}$ = value of transient thermal resistance at time t, i.e.:

$\theta_{JL(t_1+t_p)}$ = value of $\theta_{JL(t)}$ at time t_1+t_p

$\theta_{JL(t_p)}$ = value of $\theta_{JL(t)}$ at end of pulse width t_p

$\theta_{JL(t_1)}$ = value of $\theta_{JL(t)}$ at time t_1

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 9 — FORWARD RECOVERY TIME

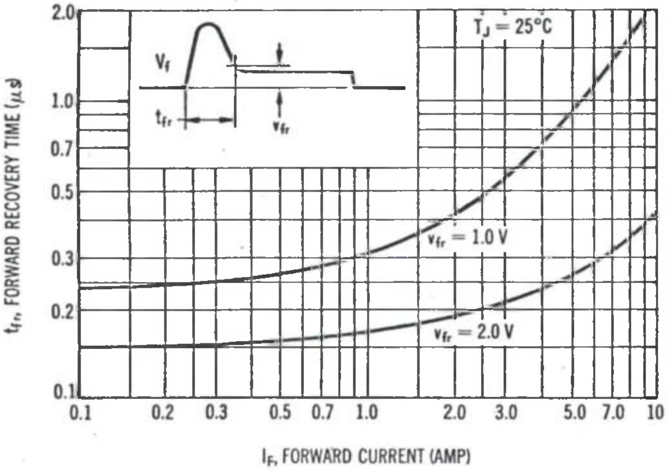


FIGURE 10 — REVERSE RECOVERY TIME

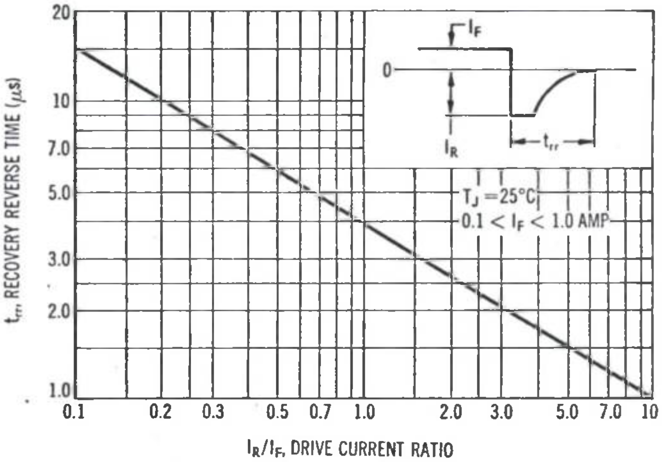


FIGURE 11 — RECTIFICATION WAVEFORM EFFICIENCY

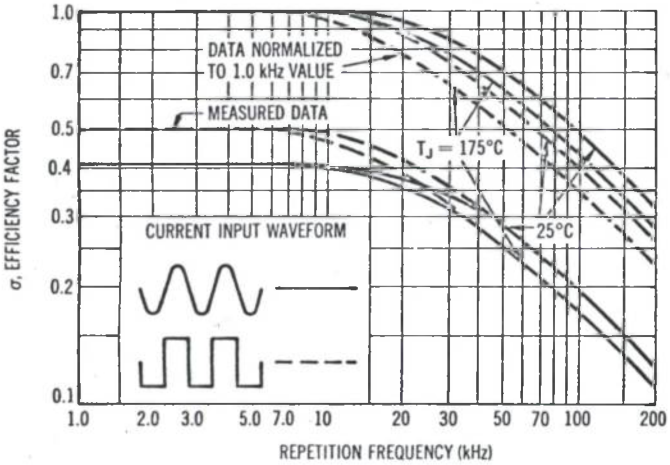
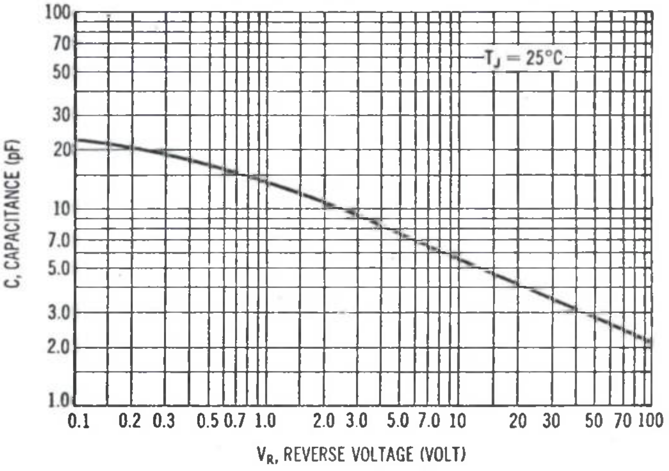
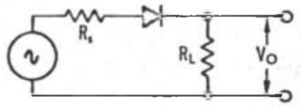


FIGURE 12 — JUNCTION CAPACITANCE



RECTIFIER EFFICIENCY NOTE

FIGURE 13 — SINGLE-PHASE HALF-WAVE RECTIFIER CIRCUIT



The rectification efficiency factor σ shown in Figure 11 was calculated using the formula:

$$\sigma = \frac{P_{dc}}{P_{rms}} = \frac{\dfrac{V^2_O(dc)}{R_L}}{\dfrac{V^2_O(rms)}{R_L}} \cdot 100\% = \frac{V^2_O(dc)}{V^2_O(ac) + V^2_O(dc)} \cdot 100\% \qquad (1)$$

For a sine wave input $V_m \sin(\omega t)$ to the diode, assumed lossless, the maximum theoretical efficiency factor becomes:

$$\sigma(\text{sine}) = \frac{\dfrac{V^2_m}{\pi^2 R_L}}{\dfrac{V^2_m}{4R_L}} \cdot 100\% = \frac{4}{\pi^2} \cdot 100\% = 40.6\% \qquad (2)$$

For a square wave input of amplitude V_m, the efficiency factor becomes:

$$\sigma(\text{square}) = \frac{\dfrac{V^2_m}{2R_L}}{\dfrac{V^2_m}{R_L}} \cdot 100\% = 50\% \qquad (3)$$

(A full wave circuit has twice these efficiencies)

As the frequency of the input signal is increased, the reverse recovery time of the diode (Figure 10) becomes significant, resulting in an increasing ac voltage component across R_L which is opposite in polarity to the forward current, thereby reducing the value of the efficiency factor σ, as shown on Figure 11.

It should be emphasized that Figure 11 shows waveform efficiency only; It does not provide a measure of diode losses. Data was obtained by measuring the ac component of V_O with a true rms ac voltmeter and the dc component with a dc voltmeter. The data was used in Equation 1 to obtain points for Figure 11.

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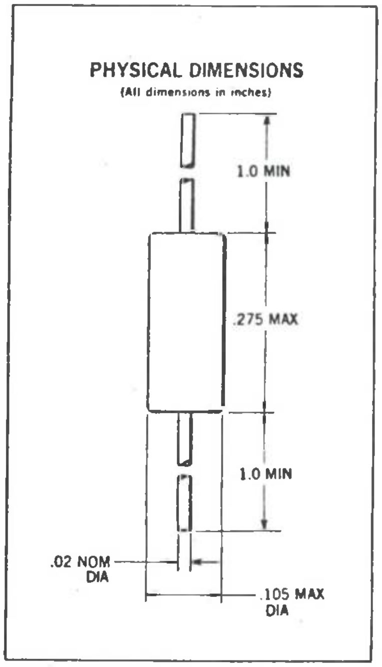
1N3064

ULTRA FAST—LOW CAPACITANCE PLANAR* DIODE

MAXIMUM RATINGS (25°C) [Note 1]

WIV	Working Inverse Voltage	50 Volts
I_o	Average rectified current	75 mA
I_F	Forward current steady state d.c.	115 mA
i_f	Recurrent peak forward current	225 mA
i_f (surge)	Peak forward surge current pulse width of 1.0 Second	500 mA
i_f (surge)	Peak forward surge current pulse width of 1.0 μSecond	2000 mA
P	Power dissipation	250 mW
P	Power dissipation at 125°C	100 mW
T_A	Operating temperature	−65°C to +150°C
T_{stg}	Storage temperature, ambient	−65°C to +175°C



ELECTRICAL SPECIFICATIONS (25°C unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_F	Forward Voltage			1.0	Volt	$I_F = 10$ mA
I_R	Reverse Current			0.1	μA	$V_R = -50$ V
I_R	Reverse Current (150°C)			100	μA	$V_R = -50$ V
BV	Breakdown Voltage	75			Volts	$I_R = 5.0$ μA
t_{rr}	Reverse Recovery Time [Note 2]			4.0	ns	$I_f = 10$ mA $I_r = 10$ mA ($V_r = 1.0$V) $R_L = 100\ \Omega$
V_{fr}	Forward Recovery Peak Voltage [Note 3]			3.0	Volts	$I_f = 100$ mA pulse
C_o	Capacitance [Note 4]			2.0	pF	$V_R = 0$ V $f = 1.0$ MHz
RE	Rectification Efficiency [Note 5]	45			%	$f = 100$ MHz
$\Delta V_F/°C$	Forward Voltage Temperature Coefficient		−1.8		mV	

*Planar is a patented Fairchild process.

NOTES:

(1) The maximum ratings are limiting values above which life or satisfactory performance may be impaired.

(2) Recovery to 1.0 mA in E. G. and G. circuit.

(3) The oscilloscope used as the response detector shall have a band width of at least 10 MHz (3.0 dB down), and shall be calibrated using a deposited carbon resistor of 50 ohms in the diode test clips. t_{fr} is defined as the difference between the 10% point of the pulse and the point where V_F is to within 10% of the quiescent value. Pulse condition shall be 0.1 ns wide at base, 20 ns maximum rise time, repetition rate = 100 KHz maximum.

(4) Capacitance as measured on Boonton Electronic Corporation Model No. 75A-S8 Capacitance Bridge or equivalent.

(5) Rectification efficiency is defined as the ratio of dc load voltage to peak rf input voltage to the detector circuit, measured with 2.0 V rms. input to the circuit. Load resistance 5.0 KΩ, load capacitance 20 pF.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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semtech™ silicon rectifiers
"ministac"™ fast recovery
TENTATIVE DATA SHEET

Type No. SFM30-70

Date 3-1-68

R61

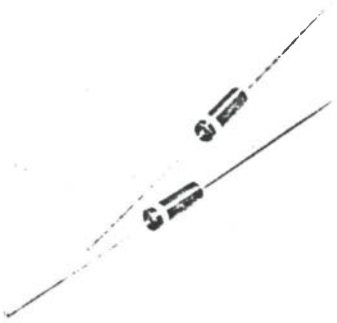
3,000 TO 7000 VOLTS

NANOSEC. REVERSE RECOVERY

UNIQUE CONSTRUCTION

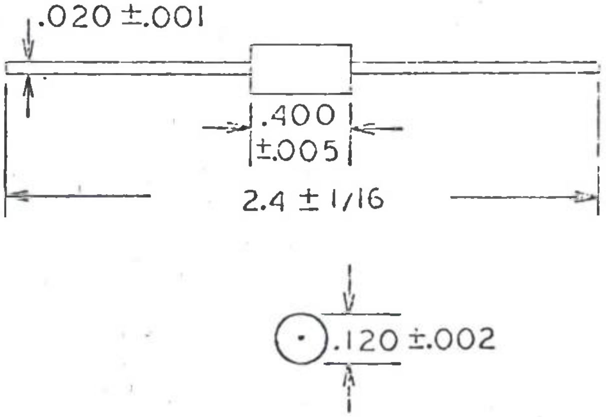
RUGGED HERMETIC SEAL

Semtech Corporation offers "MINISTAC" a Sub-Miniature multipurpose high voltage silicon rectifier. Cylindrical in design with insulated case and nickel leads for simple handling and installation. Better electrical characteristics obtained by Semtech's unique construction. Hermetically sealed and designed to meet requirements of military, industrial and consumer-product applications. Ideally suited for low current high voltage applications and multiplier circuits.



TYPE NO.	PEAK INVERSE VOLTAGE	MAX. STATIC FWD VOLTAGE @ 10 MA	AVERAGE RECTIFIED CURRENT			MAX. STATIC REVERSE CURRENT @ PIV		ONE CYCLE SURGE	RECURRENT SURGE	RECOVERY TIME ①	MAX. JUNCTION CAPACITANCE @ 100 VOLTS
			MILLIAMPS			UA	UA				
	VOLTS	VOLTS	55°C	100°C	150°C	25°C	100°C	AMPS	AMPS	NSEC.	PICOFARADS
SFM30	3000	15	10	5	0	.100	2.0	2	.100	100	1.0
SFM40	4000	15	10	5	0	.100	2.0	2	.100	100	1.0
SFM50	5000	15	10	5	0	.100	2.0	2	.100	100	1.0
SFM60	6000	15	10	5	0	.100	2.0	2	.100	250	1.0
SFM70	7000	15	10	5	0	.100	2.0	2	.100	250	1.0

Operating and Storage Temperature -55°C to +150°C



① Recovery conditions: 5 MA forward current to 10 MA reverse current.

Recovery time measured when rectifier recovers to 2.5 MA.

	1-44	50-99	100-499
SFM30	.95	.84	.81
SFM50	1.58	1.91	1.33

Semtech reserves the right to change specifications without notice.

SEMTECH CORPORATION

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Located in Rancho Conejo Light Manufacturing and Research Center

Case 51

Case 52

Case 54

Case 55

Case 56

Case 17

Case 59

The industry's most extensive line of zener diodes covering a complete range of power categories (from 250 mW to 50 W) and voltages (from 1.8 to 200 V). All diodes are 100% tested for conformity to 4 different specified characteristics.

Standard units are available with voltage tolerances of ±5%, ±10%, and ±20%, but Motorola can supply nonstandard devices to meet virtually any zener-diode requirements.

Table 1 — ZENER DIODES

Table 1a — 250-mW (Low Noise)

CASE 51 (DO-7) (Note 2)

TYPE	Nominal Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Max Imped. Z_{ZT} @ I_{ZT} Ohms (Note 6)
MZ4614	1.8	0.250	1200
MZ4615	2.0		1250
MZ4616	2.2		1300
MZ4617	2.4		1400
MZ4618	2.7		1500
MZ4619	3.0		1600
MZ4620	3.3		1650
MZ4621	3.6		1700
MZ4622	3.9		1650
MZ4623	4.3		1600
MZ4624	4.7		1550
MZ4625	5.1		1500
MZ4626	5.6		1400
MZ4627	6.2		1200
1N4099	6.8		200
1N4100	7.5		
1N4101	8.2		
1N4102	8.7		
1N4103	9.1		
1N4104	10		
1N4105	11		
1N4106	12		
1N4107	13		
1N4108	14		
1N4109	15		100
1N4110	16		
1N4111	17		↓
1N4112	18		
1N4113	19		150
1N4114	20		
1N4115	22		
1N4116	24		
1N4117	25		
1N4118	27		
1N4119	28		200
1N4120	30		
1N4121	33		
1N4122	36		
1N4123	39		
1N4124	43		250
1N4125	47		250
1N4126	51		300
1N4127	56		300
1N4128	60		400
1N4129	62		500
1N4130	68		700
1N4131	75		700
1N4132	82		800
1N4133	87		1000
1N4134	91		1200
1N4135	100		1500

See notes on page 3.

Table 1b — 400-mW

CASE 51 (DO-7)

TYPE	Nominal Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Max Imped. Z_{ZT} @ I_{ZT} Ohms (Note 6)
(Note 1)			
1N4370*	2.4	20	30
1N4371*	2.7		30
1N4372*	3.0		29
1N746*	3.3		28
1N747*	3.6		24
1N748*	3.9		23
1N749*	4.3		22
1N750*	4.7		19
1N751*	5.1		17
1N752*	5.6		11
1N753*	6.2		7.0
1N754*	6.8		5.0
1N755*	7.5		6.0
1N756*	8.2		8.0
1N757*	9.1		10
1N758*	10		17
1N759*	12		30
(Note 3)			
1N957	6.8	18.5	4.5
1N958	7.5	16.5	5.5
1N959	8.2	15.0	6.5
1N960	9.1	14.0	7.5
1N961	10	12.5	8.5
1N962*	11	11.5	9.5
1N963*	12	10.5	11.5
1N964*	13	9.5	13
1N965*	15	8.5	16
1N966*	16	7.8	17
1N967*	18	7.0	21
1N968*	20	6.2	25
1N969*	22	5.6	29
1N970*	24	5.2	33
1N971*	27	4.6	41
1N972*	30	4.2	49
1N973*	33	3.8	58
1N974*	36	3.4	70
1N975*	39	3.2	80
1N976*	43	3.0	93
1N977*	47	2.7	105
1N978*	51	2.5	125
1N979*	56	2.2	150
1N980*	62	2.0	185
1N981*	68	1.8	230
1N982*	75	1.7	270
1N983*	82	1.5	330
1N984*	91	1.4	400
1N985*	100	1.3	500
1N986*	110	1.1	750
1N987*	120	1.0	900
1N988*	130	0.95	1100
1N989*	150	0.85	1500
1N990*	160	0.80	1700
1N991*	180	0.68	2200
1N992*	200	0.65	2500

Table 1c — 500-mW

CASE 51 (DO-7)

TYPE	Nominal Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Max Imped. Z_{ZT} @ I_{ZT} Ohms (Note 6)
(Note 5)			
1N5221	2.4	20	30
1N5222	2.5		
1N5223	2.7		
1N5224	2.8		↓
1N5225	3.0		29
1N5226	3.3		28
1N5227	3.6		24
1N5228	3.9		23
1N5229	4.3		22
1N5230	4.7		19
1N5231	5.1		17
1N5232	5.6		11
1N5233	6.0		7.0
1N5234	6.2		7.0
1N5235	6.8		5.0
1N5236	7.5		6.0
1N5237	8.2		8.0
1N5238	8.7		8.0
1N5239	9.1		10
1N5240	10		17
1N5241	11		22
1N5242	12	↓	30
1N5243	13	9.5	13
1N5244	14	9.0	15
1N5245	15	8.5	16
1N5246	16	7.8	17
1N5247	17	7.4	19
1N5248	18	7.0	21
1N5249	19	6.6	23
1N5250	20	6.2	25
1N5251	22	5.6	29
1N5252	24	5.2	33
1N5253	25	5.0	35
1N5254	27	4.6	41
1N5255	28	4.5	44
1N5256	30	4.2	49
1N5257	33	3.8	58
1N5258	36	3.4	70
1N5259	39	3.2	80
1N5260	43	3.0	93
1N5261	47	2.7	105

*5.0% tolerance types available as JAN/JANTX and "Meg-A-Life II" units.

Table 1c cont'd — 500-mW
CASE 51 (DO-7)

TYPE	Nominal Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Max Imped. Z_{ZT} @ I_{ZT} Ohms (Note 6)
1N5262	51	2.5	125
1N5263	56	2.2	150
1N5264	60	2.1	170
1N5265	62	2.0	185
1N5266	68	1.8	230
1N5267	75	1.7	270
1N5268	82	1.5	330
1N5269	87	1.4	370
1N5270	91	1.4	400
1N5271	100	1.3	500
1N5272	110	1.1	750
1N5273	120	1.0	900
1N5274	130	0.95	1100
1N5275	140	0.90	1300
1N5276	150	0.85	1500
1N5277	160	0.80	1700
1N5278	170	0.74	1900
1N5279	180	0.68	2200
1N5280	190	0.66	2400
1N5281	200	0.65	2500

Table 1d — 1.0-WATT SURMETIC
CASE 59

TYPE	Nominal Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Max Imped. Z_{ZT} @ I_{ZT} Ohms (Note 6)
(Note 1)			
1N4728	3.3	76	100
1N4729	3.6	69	10
1N4730	3.9	64	9.0
1N4731	4.3	58	9.0
1N4732	4.7	53	8.0
1N4733	5.1	49	7.0
1N4734	5.6	45	5.0
1N4735	6.2	41	2.0
1N4736	6.8	37	3.5
1N4737	7.5	34	4.0
1N4738	8.2	31	4.5
1N4739	9.1	28	5.0
1N4740	10	25	7.0
1N4741	11	23	8.0
1N4742	12	21	9.0
1N4743	13	19	10
1N4744	15	17	14
1N4745	16	15.5	16
1N4746	18	14	20
1N4747	20	12.5	22
1N4748	22	11.5	23
1N4749	24	10.5	25
1N4750	27	9.5	35
1N4751	30	8.5	40
1N4752	33	7.5	45
1N4753	36	7.0	50
1N4754	39	6.5	60
1N4755	43	6.0	70
1N4756	47	5.5	80
1N4757	51	5.0	95
1N4758	56	4.5	110
1N4759	62	4.0	125
1N4760	68	3.7	150
1N4761	75	3.3	175
1N4762	82	3.0	200
1N4763	91	2.8	250
1N4764	100	2.5	350
1M110ZS10	110	2.3	450
1M120ZS10	120	2.0	550
1M130ZS10	130	1.9	700
1M150ZS10	150	1.7	1000
1M160ZS10	160	1.6	1100
1M180ZS10	180	1.4	1200
1M200ZS10	200	1.2	1500

See notes on page 3.

Table 1e — 10-WATT
CASE 52 (DO-13)

TYPE	Nominal Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Max Imped. Z_{ZT} @ I_{ZT} Ohms (Note 6)
(Note 1)			
1N3821*	3.3	76	10
1N3822*	3.6	69	10
1N3823*	3.9	64	9.0
1N3824*	4.3	58	9.0
1N3825*	4.7	53	8.0
1N3826*	5.1	49	7.0
1N3827*	5.6	45	5.0
1N3828*	6.2	41	2.0
1N3829	6.8	37	1.5
1N3830	7.5	34	1.5
(Note 3,4)			
1N3016*	6.8	37	3.5
1N3017*	7.5	34	4.0
1N3018*	8.2	31	4.5
1N3019*	9.1	28	5.0
1N3020*	10	25	7.0
1N3021*	11	23	8.0
1N3022*	12	21	9.0
1N3023*	13	19	10
1N3024*	15	17	14
1N3025*	16	15.5	16
1N3026*	18	14.0	20
1N3027*	20	12.5	22
1N3028*	22	11.5	23
1N3029*	24	10.5	25
1N3030*	27	9.5	35
1N3031*	30	8.5	40
1N3032*	33	7.5	45
1N3033*	36	7.0	50
1N3034*	39	6.5	60
1N3035*	43	6.0	70
1N3036*	47	5.5	80
1N3037*	51	5.0	95
1N3038*	56	4.5	110
1N3039*	62	4.0	125
1N3040*	68	3.7	150
1N3041*	75	3.3	175
1N3042*	82	3.0	200
1N3043*	91	2.8	250
1N3044*	100	2.5	350
1N3045*	110	2.3	450
1N3046*	120	2.0	550
1N3047*	130	1.9	700
1N3048*	150	1.7	1000
1N3049*	160	1.6	1100
1N3050*	180	1.4	1200
1N3051*	200	1.2	1500

Table 1f — 1.5-WATT
CASE 55

TYPE	Nominal Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Max Imped. Z_{ZT} @ I_{ZT} Ohms (Note 6)
(Note 3)			
1N3785	6.8	55	2.7
1N3786	7.5	50	3.0
1N3787	8.2	46	3.5
1N3788	9.1	41	4.0
1N3789	10	37	5.0
1N3790	11	34	6.0
1N3791	12	31	7.0
1N3792	13	29	8.0
1N3793	15	25	10
1N3794	16	23	11
1N3795	18	21	13
1N3796	20	19	15
1N3797	22	17	16
1N3798	24	16	17
1N3799	27	14	20
1N3800	30	12	25
1N3801	33	11	30
1N3802	36	10	35
1N3803	39	10	40
1N3804	43	9.0	45
1N3805	47	8.0	55
1N3806	51	7.4	65
1N3807	56	6.7	75
1N3808	62	6.0	85
1N3809	68	5.5	95
1N3810	75	5.0	110
1N3811	82	4.5	130
1N3812	91	4.1	150
1N3813	100	3.7	200
1N3814	110	3.4	300
1N3815	120	3.1	350
1N3816	130	2.9	400
1N3817	150	2.5	700
1N3818	160	2.3	750
1N3819	180	2.1	800
1N3820	200	1.9	1000

Table 1g — 5.0-WATT
CASE 17

TYPE	Nominal Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Max Imped. Z_{ZT} @ I_{ZT} Ohms (Note 6)
(Note 3)			
1N5333	3.3	380	3.0
1N5334	3.6	350	2.5
1N5335	3.9	320	2.0
1N5336	4.3	290	2.0
1N5337	4.7	260	2.0
1N5338	5.1	240	1.5
1N5339	5.6	220	1.0
1N5340	6.0	200	1.0
1N5341	6.2	200	1.0
1N5342	6.8	175	1.0
1N5343	7.5	175	1.5
1N5344	8.2	150	1.5
1N5345	8.7	150	2.0
1N5346	9.1	150	2.0
1N5347	10	125	2.0
1N5348	11	125	2.5
1N5349	12	100	2.5
1N5350	13	100	2.5
1N5351	14	100	2.5
1N5352	15	75	2.5
1N5353	16	75	2.5
1N5354	17	70	2.5
1N5355	18	65	2.5
1N5356	19	65	3.0
1N5357	20	65	3.0
1N5358	22	50	3.5
1N5359	24	50	3.5
1N5360	25	50	4.0
1N5361	27	50	5.0
1N5362	28	50	6.0
1N5363	30	40	8.0
1N5364	33	40	10
1N5365	36	30	11
1N5366	39	30	14
1N5367	43	30	20
1N5368	47	25	25
1N5369	51	25	27
1N5370	56	20	35
1N5371	60	20	40
1N5372	62	20	42
1N5373	68	20	44
1N5374	75	20	45
1N5375	82	15	65
1N5376	87	15	75
1N5377	91	15	75
1N5378	100	12	90
1N5379	110	12	125
1N5380	120	10	170
1N5381	130	10	190
1N5382	140	8.0	230
1N5383	150	8.0	330
1N5384	160	8.0	350
1N5385	170	8.0	380
1N5386	180	5.0	430
1N5387	190	5.0	450
1N5388	200	5.0	480

Table 1h — 10-WATT
CASE 56 (DO-4)

TYPE	Nominal Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Max Imped. Z_{ZT} @ I_{ZT} Ohms (Note 6)
(Note 1,4)			
1N3993*	3.9	640	2.0
1N3994*	4.3	580	1.5
1N3995*	4.7	530	1.2
1N3996*	5.1	490	1.1
1N3997*	5.6	445	1.0
1N3998*	6.2	405	1.1
1N3999*	6.8	370	1.2
1N4000*	7.5	335	1.3

*5.0% tolerance types available as JAN/JANTX and "Meg-A-Life II" units.

Table 1h cont'd — 10-WATT

CASE 56 (DO-4)

TYPE	Nominal Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Max Imped. Z_{ZT} @ I_{ZT} Ohms (Note 6)
(Note 3,4)			
1N2970*	6.8	370	1.2
1N2971*	7.5	335	1.3
1N2972*	8.2	305	1.5
1N2973*	9.1	275	2.0
1N2974*	10	250	3.0
1N2975*	11	230	↓
1N2976*	12	210	
1N2977*	13	190	
1N2979*	15	170	
1N2980*	16	155	4.0
1N2982*	18	140	↓
1N2984*	20	125	
1N2985*	22	115	5.0
1N2986*	24	105	5.0
1N2988*	27	95	7.0
1N2989*	30	85	8.0
1N2990*	33	75	9.0
1N2991*	36	70	10
1N2992*	39	65	11
1N2993*	43	60	12
1N2995*	47	55	14
1N2997*	51	50	15
1N2999*	56	45	16
1N3000*	62	40	17
1N3001*	68	37	18
1N3002*	75	33	22
1N3003*	82	30	25
1N3004*	91	28	35
1N3005*	100	25	40
1N3007*	110	23	55
1N3008*	120	20	75
1N3009*	130	19	100
1N3011*	150	17	175
1N3012*	160	16	200
1N3014*	180	14	260
1N3015*	200	12	300

Table 1j — 50-WATT

CASE 54 CASE 58 (Note 3, 4)

TYPE		Nominal Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Max Imped. Z_{ZT} @ I_{ZT} Ohms (Note 6)
1N4557	1N4549	3.9	3200	0.16
1N4558	1N4550	4.3	2900	0.16
1N4559	1N4551	4.7	2650	0.12
1N4560	1N4552	5.1	2450	↓
1N4561	1N4553	5.6	2250	
1N4562	1N4554	6.2	2000	0.14
1N4563	1N4555	6.8	1850	0.16
1N2804*	1N3305	6.8	1850	0.20
1N4564	1N4556	7.5	1650	0.24
1N2805*	1N3306	7.5	1700	0.3
1N2806*	1N3307	8.2	1500	0.4
1N2807*	1N3308	9.1	1370	0.5
1N2808*	1N3309	10	1200	0.6
1N2809*	1N3310	11	1100	0.8
1N2810*	1N3311	12	1000	1.0
1N2811*	1N3312	13	960	1.1
1N2812	1N3313	14	890	1.2
1N2813*	1N3314	15	830	1.4
1N2814*	1N3315	16	780	1.6
1N2815	1N3316	17	740	1.8
1N2816*	1N3317	18	700	2.0
1N2817	1N3318	19	660	2.2
1N2818*	1N3319	20	630	2.4
1N2819*	1N3320	22	570	2.5
1N2820*	1N3321	24	520	2.6
1N2821	1N3322	25	500	2.7
1N2822*	1N3323	27	460	2.8
1N2823*	1N3324	30	420	3.0
1N2824*	1N3325	33	380	3.2
1N2825*	1N3326	36	350	3.5
1N2826*	1N3327	39	320	4.0
1N2827*	1N3328	43	290	4.5
1N2828	1N3329	45	280	4.5
1N2829*	1N3330	47	270	5.0
1N2830	1N3331	50	250	5.0
1N2831*	1N3332	51	245	5.2
1N2832*	1N3334	56	220	6.0
1N2833*	1N3335	62	200	7.0
1N2834*	1N3336	68	180	8.0
1N2835*	1N3337	75	170	9.0
1N2836*	1N3338	82	150	11
1N2837*	1N3339	91	140	15
1N2838*	1N3340	100	120	20
1N2839	1N3341	105	120	25
1N2840*	1N3342	110	110	30
1N2841*	1N3343	120	100	40
1N2842*	1N3344	130	95	50
1N2843*	1N3346	150	85	75
1N2844*	1N3347	160	80	80
1N2845*	1N3349	180	68	90
1N2846*	1N3350	200	65	100

*5.0% tolerance types available as JAN/JANTX and "Meg-A-Life II" units.

Notes:

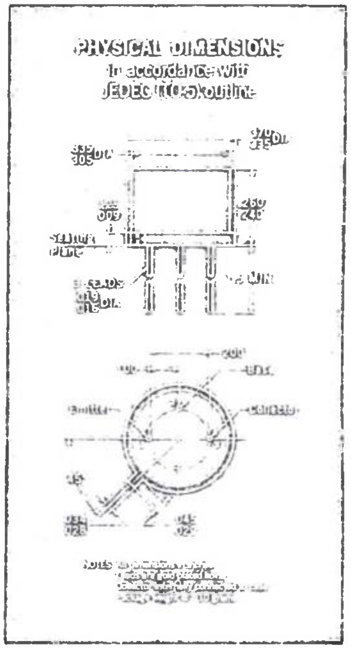
1. Standard types are ±10% tolerance; suffix "A" denotes ±5.0% tolerance.
2. Standard tolerance of ±5.0%.
3. Standard tolerances of 5.0, 10, and 20% are available — no suffix is ±20% tolerance, "A" suffix is ±10% tolerance, and "B" suffix is ±5.0% tolerance.
4. Reverse polarity types available.
5. The JEDEC type numbers shown indicate a tolerance of ±10% with guaranteed limits on V_Z, I_R and V_F. Units with guaranteed limits on V_Z, I_R, V_F, Z_{ZT}, Z_{ZK} and T_C (Temperature Coefficient) are indicated by suffix "A" for ±10% tolerance and suffix "B" for ±5.0% units.
6. Impedance is derived from the 60 cycle ac voltage which results when an ac current having an RMS value equal to 10% of the dc zener current is superimposed upon the dc current.

2N2218A • 2N2219A • 2N2221A • 2N2222A

NPN HIGH SPEED SWITCHES

DIFFUSED SILICON PLANAR EPITAXIAL TRANSISTORS

GENERAL DESCRIPTION - These Fairchild devices are NPN silicon PLANAR epitaxial transistors designed for high-speed switching at collector currents up to 500 mA. They feature useful beta over a wide range of collector current, low leakage currents, and low saturation voltages.



2N2218A • 2N2219A

ABSOLUTE MAXIMUM RATINGS [Note 1]

Maximum Temperatures

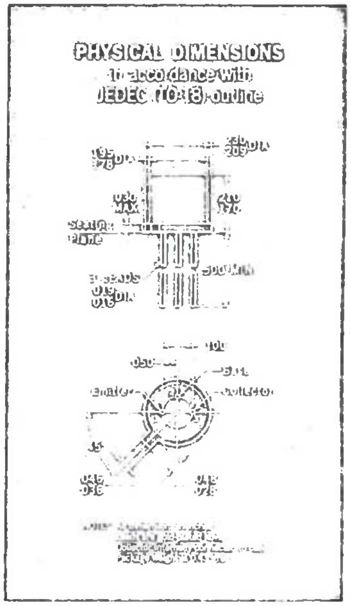
Storage Temperature	-65°C to +300°C
Operating Junction Temperature	+175°C Maximum

Maximum Power Dissipation

		2N2218A 2N2219A	2N2221A 2N2222A
Total Dissipation at 25°C Case Temperature	(Notes 2 & 3)	3.0 Watts	1.8 Watt
at 25°C Ambient Temperature	(Notes 2 & 3)	0.8 Watt	0.5 Watt

Maximum Voltages and Current

V_{CBO}	Collector to Base Voltage		75 Volts
V_{CEO}	Collector to Emitter Voltage	(Note 4)	40 Volts
V_{EBO}	Emitter to Base Voltage		6.0 Volts
I_C	Collector Current		800 mA



2N2221A • 2N2222A

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

		2N2218A 2N2221A		2N2219A 2N2222A			
Symbol	Characteristic	Min.	Max.	Min.	Max.	Units	Test Conditions
h_{FE}	DC Current Gain	20		35			I_C = 100 μA V_{CE} = 10 V
h_{FE}	DC Current Gain	25		50			I_C = 1.0 mA V_{CE} = 10 V
h_{FE}	DC Pulse Current Gain (Note 5)	35		75			I_C = 10 mA V_{CE} = 10 V
h_{FE}	DC Pulse Current Gain (Note 5)	40	120	100	300		I_C = 150 mA V_{CE} = 10 V
h_{FE}	DC Pulse Current Gain (Note 5)	25		40			I_C = 500 mA V_{CE} = 10 V
h_{FE}(-55°C)	DC Pulse Current Gain (Note 5)	15		35			I_C = 10 mA V_{CE} = 10 V
h_{FE}	DC Pulse Current Gain (Note 5)	20		50			I_C = 150 mA V_{CE} = 1.0 V
V_{CE}(sat)	Collector Saturation Voltage (Pulsed, Note 5)		0.3		0.3	Volts	I_C = 150 mA I_B = 15 mA
V_{CE}(sat)	Collector Saturation Voltage (Pulsed, Note 5)		1.0		1.0	Volts	I_C = 500 mA I_B = 50 mA
V_{BE}(sat)	Base Saturation Voltage (Pulsed, Note 5)	0.6	1.2	0.6	1.2	Volts	I_C = 150 mA I_B = 15 mA
V_{BE}(sat)	Base Saturation Voltage (Pulsed, Note 5)		2.0		2.0	Volts	I_C = 500 mA I_B = 50 mA
h_{fe}	High Frequency Current Gain (f = 100 Mc)	2.5		3.0			I_C = 20 mA V_{CE} = 20 V
f_T	Gain-Bandwidth Product (f = 100 Mc)	250		300		Mc	I_C = 20 mA V_{CE} = 20 V

Additional Electrical Characteristics on page 2

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MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3025589, 3064167, 3108359, 3117260. OTHER PATENTS PENDING.

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N2218A 2N2221A MIN.	 MAX.	2N2219A 2N2222A MIN.	 MAX.	UNITS	TEST CONDITIONS	
I_{CEX}	Collector Reverse Current		10		10	nA	$V_{EB} = 3.0$ V	$V_{CE} = 60$ V
I_{CBO}	Collector Reverse Current		10		10	nA	$I_E = 0$	$V_{CB} = 60$ V
I_{CBO}(+150°C)	Collector Reverse Current		10		10	μA	$I_E = 0$	$V_{CB} = 60$ V
I_{EBO}	Base Current		10		10	nA	$I_C = 0$	$V_{EB} = 3.0$ V
C_{obo}	Common Base, Open Circuit Output Capacitance (f = 100 Kc)		8.0		8.0	pf	$I_E = 0$	$V_{CB} = 10$ V
C_{ibo}	Common Base, Open Circuit Input Capacitance (f = 100 Kc)		25		25	pf	$I_C = 0$	$V_{EB} = 0.5$ V
$Re(h_{ie})$	Real Part of Common-Emitter High Frequency Input Impedance (f = 300 Mc)		60		60	Ohms	$I_C = 20$ mA	$V_{CE} = 20$ V
BV_{CBO}	Collector to Base Breakdown Voltage	75		75		Volts	$I_C = 10$ μA	$I_E = 0$
BV_{CEO}	Collector to Emitter Breakdown Voltage (Notes 4 & 5)	40		40		Volts	$I_C = 10$ mA	$I_B = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	6.0		6.0		Volts	$I_C = 0$	$I_E = 10$ μA
I_{BL}	Base Current		20		20	nA	$V_{EB} = 3.0$ V	$V_{CE} = 60$ V
t_d	Turn-on Delay Time		10		10	nsec	$I_{CS} = 150$ mA $I_{B1} = 15$ mA, $V_{BE}(\text{off}) = 0.5$ V	$V_{CC} = 30$ V
t_r	Rise Time		25		25	nsec	$I_{CS} = 150$ mA $I_{B1} = 15$ mA, $V_{BE}(\text{off}) = 0.5$ V	$V_{CC} = 30$ V
t_s	Storage Time		225		225	nsec	$I_{CS} = 150$ mA $I_{B1} = 15$ mA, $I_{B2} = 15$ mA	$V_{CC} = 30$ V
t_f	Fall Time		60		60	nsec	$I_{CS} = 150$ mA $I_{B1} = 15$ mA, $I_{B2} = 15$ mA	$V_{CC} = 30$ V
τ_A	Active Region Time Constant		2.5		2.5	nsec	$I_C = 150$ mA	$V_{CE} = 30$ V
$r_b'C_c$	Collector Base Time Constant (f = 31.8 Mc)		150		150	psec	$I_C = 20$ mA	$V_{CE} = 20$ V
NF	Noise Figure (f = 1.0 Kc)		4.0		4.0		$I_C = 100$ μA $R_g = 1.0$ KΩ	$V_{CE} = 10$ V BW = 1.0 cps

SMALL SIGNAL CHARACTERISTICS (f = 1 kc)

SYMBOL	CHARACTERISTIC	2N2218A 2N2221A MIN.	 MAX.	2N2219A 2N2222A MIN.	 MAX.	UNITS	TEST CONDITIONS	
h_{ie}	Input Resistance	1.0	3.5	2.0	8.0	KΩ	$I_C = 1.0$ mA	$V_{CB} = 10$ V
		0.2	1.0	0.25	1.25	KΩ	$I_C = 10$ mA	$V_{CB} = 10$ V
h_{oe}	Output Conductance	3.0	15	5.0	35	μmhos	$I_C = 1.0$ mA	$V_{CB} = 10$ V
		10	100	25	200	μmhos	$I_C = 10$ mA	$V_{CB} = 10$ V
h_{re}	Voltage Feedback Ratio		500		800	$x10^{-6}$	$I_C = 1.0$ mA	$V_{CB} = 10$ V
			250		400	$x10^{-6}$	$I_C = 10$ mA	$V_{CB} = 10$ V
h_{fe}	Forward Current Transfer Ratio	30	150	50	300		$I_C = 1.0$ mA	$V_{CB} = 10$ V
		50	300	75	375		$I_C = 10$ mA	$V_{CB} = 10$ V

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 175°C and junction-to-case thermal resistance of 50°C/Watt (derating factor of 20 mW/°C); junction-to-ambient thermal resistance of 188°C/Watt (derating factor of 5.33 mW/°C) for the 2N2218A and 2N2219A. For the 2N2221A and 2N2222A, junction-to-case thermal resistance of 83.5°C/Watt (derating factor of 12 mW/°C; junction-to-ambient thermal resistance of 300°C/Watt (derating factor of 3.33 mW/°C).

(4) This rating refers to a high-current point where collector-to-emitter voltage is lowest. For more information send for Fairchild Publication APP-4.

(5) Pulse Conditions: length = 300 μsec; duty cycle = 1%.

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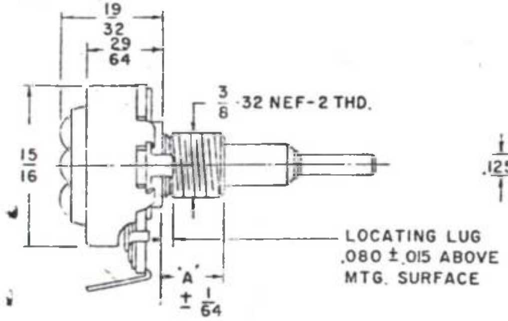
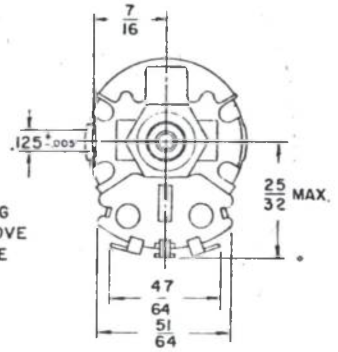
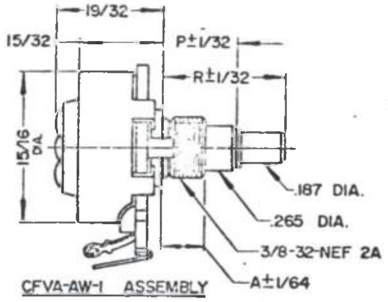
CONCENTRIC VARIABLE RESISTORS

CFVA-45

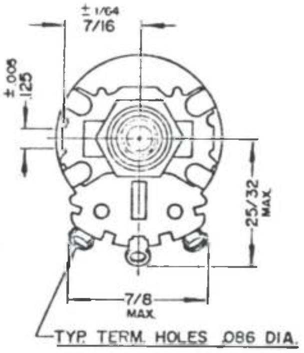


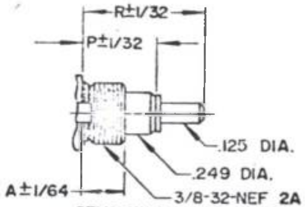


CFVA-AW



CFVA-AW-1 ASSEMBLY





CFVA-AW-2 ASSEMBLY

mechanical specifications

	CFVA-45	CFVA-AW
Angle of Rotation:		
Contact arm	300° ±5°	280° ±5°
Panel shaft*	300°	280°
Rear shaft*	3700° - 10-1/4 turns	3150° - 8-3/4 turns
*Total effective rotation	(1° for each 12.5°)	(1° for each 10.5°)
Bushing Information:		
Diameter, EIA Standard	3/8"-32 NEF-2A thread	
Standard length	3/8" or 1/4" ±1/64"	
Special lengths	Available upon request	
(Refer to General Information for recommended bushing lengths for various shafts.)		
Shafts Available:		
Dia. outer shaft	.250" +.000" -.002"	or .265" ±.001"
Dia. inner shaft	.125" ±.001"	or .187" ±.001"
Length	As required in increments of 1/16"	
Locating Lugs:		
Standard position	Left side terminals down supplied unless otherwise specified.	
Other positions	Lug right side terminals down, without lugs or with lugs both left and right sides.	
Switch:	Not available	

CFVA-45

order from:

CTS Electronics, Inc.
1010 Sycamore Avenue
South Pasadena, California
91030
Phone 213-254-9141

CFVA-AW

order from:

CTS Of Asheville, Inc.
Mills Gap Road
Skyland, North Carolina
28776
Phone 704-684-6451

9-69-EE

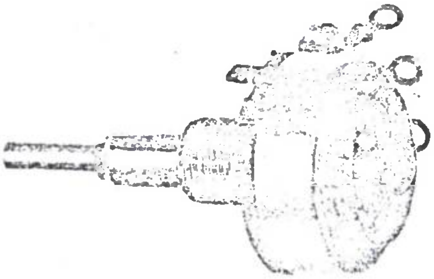
CTS 15/16 Diameter Vernier Concentric Variable Resistors

TYPES CFVA-45 (Carbon) , CFVA-AW (Wirewound)

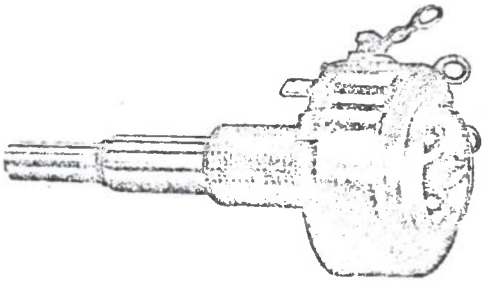
Single section variable resistors with direct and vernier drive on concentric shafts.

- Wide resistance range
- More economical, more reliable, than a 2-section control.
- Resistance tolerances as low as ±5%
- Positive stops on outer shaft; clutch stops on inner shaft.

CFVA-45



CFVA-AW



electrical specifications	CFVA-45	CFVA-AW
Resistance Range: (Linear Taper)	100Ω thru 10 MegΩ	1Ω thru 25KΩ
Resistance Tolerance: Standard	100Ω thru 5 MegΩ ±30% Above 5 MegΩ-10 MegΩ ±40%	1Ω thru 25KΩ ±10%
Special	Available in most resistance values	1Ω thru 25KΩ ±5%
Power Rating:	1/2 watt thru 10KΩ 1/3 watt above 10KΩ-100KΩ 1/4 watt above 100KΩ @ 55°C derated to no load @ 85°C, linear taper mounted on steel panel 4" x 4" x .050".	5 watts @ 25°C, 4 watts @ 55°C, derated to no load @105°C, linear taper, mounted on steel panel 4" x 4" x .050".
Voltage Ratings:* Bushing to Terminals High pot test, 1 min.	1,000 VAC	1,000 VAC
Operating maximum *Not to exceed wattage ratings	750 VDC	500 VDC
Tapers Available: Standard	Linear	Linear
Special	Available	Available
Taps Available: Single	40% or 60% effect. rot.	Not available
Double	35% & 65% effect. rot.	Not available

CTS CORPORATION AND SUBSIDIARIES / MANUFACTURERS OF ELECTRONIC COMPONENTS

ENVIRONMENTAL PERFORMANCE SPECIFICATIONS

Load Life: Allowable resistance change after 1000 hours ±6%.

Rotational Life: Allowable resistance change

Standard bushing after	50,000 cycles	±5%
Standard bushing after	100,000 cycles	±10%
Locking type bushing after	1000 cycles	±5%

Moisture Resistance: Allowable resistance change ±4%

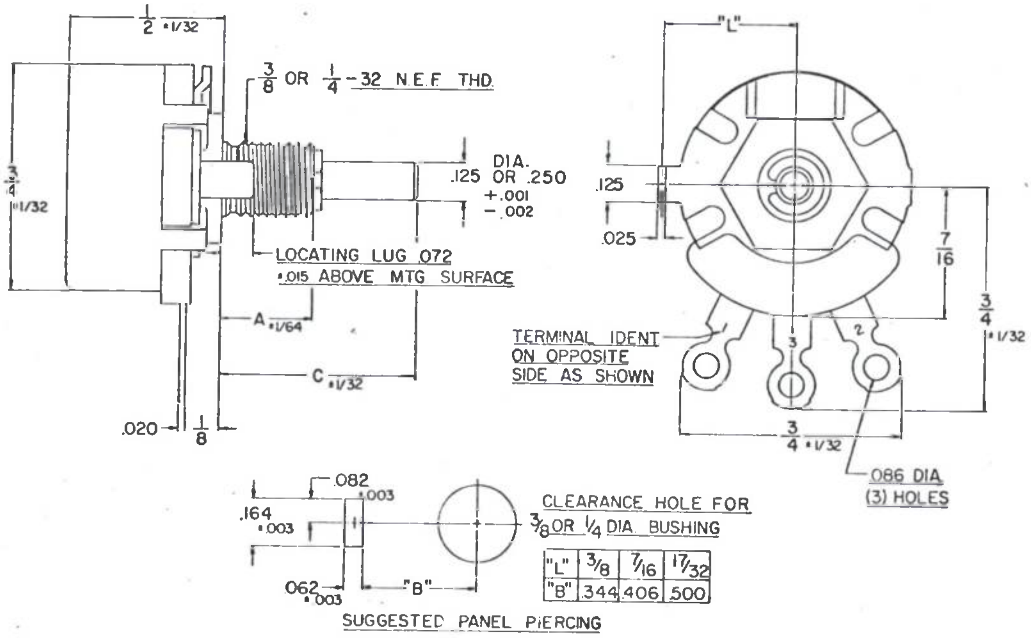
Temperature Coefficient:

Resistance Range	40 ohms to 1.35K ohms	1.36K to 2.9K ohms	3K to 1.35 Meg.	1.36 Meg. to 5 Meg.
Std. T.C. (in PPM/°C)	-50 to +200	-100 to +300	-100 to +250	±250
Special T.C. (in PPM/°C)	-0 to +100	-0 to +250	±100	±150

Temperature Cycling: Allowable resistance change after test ±3%

Voltage Coefficient: Allowable resistance change .05%/V (or less)

CTS SERIES 550



"L"	3/8	7/16	17/32
"B"	.344	.406	.500

order from:

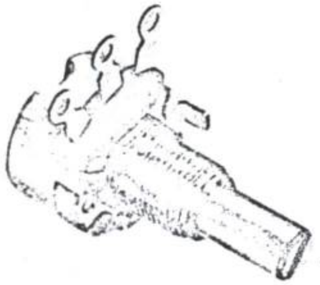
CTS OF BERNE, INC./Berne, Indiana (Subsidiary of CTS Corporation, Elkhart, Indiana)

CTS SERIES 550

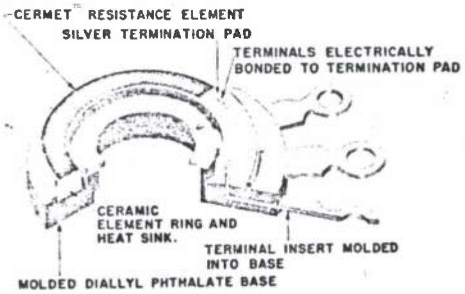
3/4" DIAMETER CERMET VARIABLE RESISTOR

- High Stability and Reliability
- Low Noise and Long Life
- Wide Resistance Range
- Excellent High Frequency Characteristics
- Infinite Resolution
- Excellent Overload Capacity
- CTS CERMET Resistance Element
- Molded Terminal Base
- Closed Construction

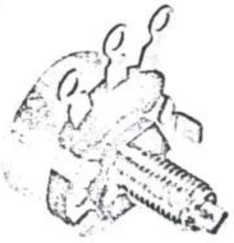
TYPE 550



1/4" DIA. SHAFT


CERMET RESISTANCE ELEMENT
SILVER TERMINATION PAD
TERMINALS ELECTRICALLY BONDED TO TERMINATION PAD
CERAMIC ELEMENT RING AND HEAT SINK.
TERMINAL INSERT MOLDED INTO BASE
MOLDED DIALLYL PHTHALATE BASE

TYPE 551



1/8" DIA. SHAFT

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electrical and mechanical specifications

Resistance Range:
50 Ohms through 5 Megohms

Resistance Tolerance:
Standard - ±20%
Special - ±10%

Voltage Rating:
Across End Terminals
350 VDC load not to exceed wattage rating
Terminals to case

High pot test 1 min.	1000 VAC
@3.4" Mercury	450 VAC
Operating Maximum	500 VDC

Tapers:
Standard - Linear
Special - Available

Attenuators and Multiple Sections Available

Turning Torque - 0.5 to 6 in. oz.

Stop Torque - 5" lbs.

Independent Linearity
Standard - ± 5%
Special - ± 3%

ENR:
Standard - ±2%
Special - ±1%

Power Rating:
2 Watts @ 70°C derated to no load @ 150°C

Angle of Rotation: 280° ±5°

Bushing Information:
Standard - 3/8"-32 NEF-2A Thd.
Non-locking or locking types
Std.Lengths-.375" non-locking
.500" locking
Special Lengths - Available

Shaft Length and Trim -
As required

SERIES 54L/74L

Device	Location	Normalized Input Factor	Normalized Output Factor	Normalized Output Factor
SN54L00/74L00	Any Input	.25		
	Any Output		1.25	2.5*
SN54L04/74L04	Any Input	.25		
	Any Output		1.25	2.5*
SN54L10/74L10	Any Input	.25		
	Any Output		1.25	2.5*
SN54L20/74L20	Any Input	.25		
	Any Output		1.25	2.5*
SN54L30/74L30	Any Input	.25		
	Any Output		1.25	2.5*
SN54L51/74L51	Any Input	.25		
	Any Output		1.25	2.5*
SN54L54/74L54	Any Input	.25		
	Any Output		1.25	2.5*
SN54L55/74L55	Any Input	.25		
	Any Output		1.25	2.5*
SN54L71/74L71	R1, R2, R3, S1, S2, or S3 Input	.25		
	Clock Input	.50		
	Preset or Clear Input	.50		
	Q or $\bar{Q}$ Output		1.25	2.5*
SN54L72/74L72	J1, J2, J3, K1, K2, or K3 Input	.25		
	Clock Input	.50		
	Preset or Clear Input	.50		
	Q or $\bar{Q}$ Output		1.25	2.5*
SN54L73/74L73	J or K Input	.25		
	Clock Input	.50		
	Clear Input	.50		
	Q or $\bar{Q}$ Output		1.25	2.5*
SN54L78/74L78	J or K Input	.25		
	Preset Input	.50		
	Clear or Clock Input	1.00		
	Q or $\bar{Q}$ Output		1.25	2.5*
SN54L86/74L86	Any Input	.25		
	Any Output		1.25	2.5*
SN54L91/74L91	Any Input	.25		
	Any Output		1.25	2.5*
SN54L93/74L93	R_{01} or R_{02} Input	.25		
	B Input	.50		
	A Input	.50		
	Any Output		1.25	2.5*
SN54L95/74L95	Any Input except Mode Control	.25		
	Mode Control Input	.50		
	Any Output		1.25	2.5*

*Use these numbers when driving Series 54L/74L loads only.

Design loading chart

SERIES 54H/74H			
Device	**Location**	**Normalized Input Factor**	**Normalized Output Factor**
SN54H00/74H00	Any Input	1.25	
	Any Output		12.5
SN54H01/74H01	Any Input	1.25	
	Any Output		12.5
SN54H04/74H04	Any Input	1.25	
	Any Output		12.5
SN54H05/74H05	Any Input	1.25	
	Any Output		12.5
SN54H10/74H10	Any Input	1.25	
	Any Output		12.5
SN54H11/74H11	Any Input	1.25	
	Any Output		12.5
SN54H20/74H20	Any Input	1.25	
	Any Output		12.5
SN54H21/74H21	Any Input	1.25	
	Any Output		12.5
SN54H22/74H22	Any Input	1.25	
	Any Output		12.5
SN54H30/74H30	Any Input	1.25	
	Any Output		12.5
SN54H40/74H40	Any Input	1.25	
	Any Output		37.5
SN54H50/74H50	A, B, C, or D Input	1.25	
	X or $\bar{X}$ Input	N/A	
	Any Output		12.5
SN54H51/74H51	Any Input	1.25	
	Any Output		12.5
SN54H52/74H52	A, B, C, D, E, F, G, H, or J Input	1.25	
	X Input	N/A	
	Output		12.5
SN54H53/74H53	A, B, C, D, E, F, G, H, or J Input	1.25	
	X or $\bar{X}$ Input	N/A	
	Output		12.5
SN54H54/74H54	Any Input	1.25	
	Output		12.5
SN54H55/74H55	A, B, C, D, E, F, G, or H Input	1.25	
	X or $\bar{X}$ Input	N/A	
	Output		12.5

SERIES 54H/74H			
Device	**Location**	**Normalized Input Factor**	**Normalized Output Factor**
SN54H60/74H60	Any Input	1.25	
	X or $\bar{X}$ Output		N/A
SN54H61/74H61	Any Input	1.25	
	Any Output		N/A
SN54H62/74H62	Any Input	1.25	
	X or $\bar{X}$ Output		N/A
SN54H71/74H71	J1A, J2A, J1B, J2B, K1A, K2A, K1B, or K2B Input	1.25	
	Clock Input	2.50	
	Preset Input	3.75	
	Q or $\bar{Q}$ Output		12.5
SN54H72/74H72	J1, J2, J3, K1, K2, or K3 Input	1.25	
	Preset or Clear Input	2.50	
	Clock Input	1.25	
	Q or $\bar{Q}$ Output		12.5
SN54H73/74H73	J, K, or Clock Input	1.25	
	Clear Input	2.50	
	Q or $\bar{Q}$ Output		12.5
SN54H76/74H76	J, K, or Clock Input	1.25	
	Clear or Preset Input	2.50	
	Q or $\bar{Q}$ Output		12.5
SN54H78/74H78	J or K Input	1.25	
	Clear Input	5.00	
	Clock or Preset Input	2.50	
	Q or $\bar{Q}$ Output		12.5
SN54H87/74H87	Any Input	1.25	
	Any Output		12.5
54H101/74H101	Any Input except Clock	1.25	
	Clock Input	3.0	
	Any Output		12.5
54H102/74H102	Any Input except Clock	1.25	
	Clock Input	3.0	
	Any Output		12.5
54H103/74H103	Any Input except Clock	1.25	
	Clock Input	3.0	
	Any Output		12.5
54H106/74H106	Any Input except Clock	1.25	
	Clock Input	3.0	
	Any Output		12.5
54H108/74H108	J, K and Preset Inputs	1.25	
	Clear Input	2.50	
	Clock Input	6.0	
	Any Output		12.5

SERIES 54/74

Device	Location	Normalized Input Factor	Normalized Output Factor
SN5475/7475	D_1, D_2, D_3, or D_4 Input	2.0	
	Clock 1-2, or Clock 3-4 Input	4.0	
	Any Output		10.0
SN5476/7476	J or K Input	1.0	
	Clock Input	2.0	
	Clear Input	2.0	
	Preset Input	2.0	
	Q or $\overline{Q}$ Output		10.0
SN5477/7477	Any D Input	2.0	
	Clock 1-2 or Clock 3-4 Input	4.0	
	Any Output		10.0
SN5480/7480	A_1, A_2, B_1, B_2, A_C, or B_C Input	1.0	
	A★or B★Input	1.65	
	C_n Input	5.0	
	$\overline{\Sigma}$ or Σ Output		10.0
	$\overline{C_{n+1}}$ Output		5.0
	A★or B★Output		3.0
SN5481/7481	Write 1 and Write 0 Input	1.0	
	X and Y Inputs:		
	Logical 0	7.0	
	Logical 1	10.0	
	S_0 or S_1		25.0
SN5482/7482	A_1, or B_1 Input	4.0	
	A_2 or B_2 Input	1.0	
	C_{IN} Input	4.0	
	C_2 Output		5.0
	Σ_1 or Σ_2 Output		10.0
SN5483/7483	A_1, B_1, A_2, or B_3 Input	4.0	
	A_2, B_2, A_4, or B_4 Input	1.0	
	C_{IN} Input	4.0	
	C_4 Output		5.0
	Σ_1, Σ_2, Σ_3, or Σ_4 Output		10.0
SN5484/7484	Write 1 and Write 0 Input	1.0	
	X and Y Inputs:		
	Logical 0	7.0	
	Logical 1	10.0	
	S_0 or S_1		25.0
SN5486/7486	Any Input	1.0	
	Any Output		
	Logical 1		20.0
	Logical 0		10.0
SN5490/7490	R_{01}, R_{02}, R_{91}, or R_{92} Input	1.0	
	BD Input	4.0	
	A Input	2.0	
	Any Output		10.0

SERIES 54/74

Device	Location	Normalized Input Factor	Normalized Output Factor
SN5491A/7491A	A or B Input	1.0	
	$\overline{CP}$ Input	1.0	
	Q or $\overline{Q}$ Output		10.0
SN5492/7492	R_{01} or R_{02} Input	1.0	
	BC Input	4.0	
	A Input	2.0	
	Any Output		10.0
SN5493/7493	R_{01} or R_{02} Input	1.0	
	B Input	2.0	
	A Input	2.0	
	Any Output		10.0
SN5494/7494	Any Input except Preset 1 or 2	1.0	
	Preset 1 or Preset 2 Input	4.0	
	Any Output		10.0
SN5495/7495	Any Input except Mode Control	1.0	
	Mode Control Input	2.0	
	Any Output		10.0
SN5496/7496	Any Input except Preset	1.0	
	Preset Input	5.0	
	Any Output		10.0
SN54100/74100	Any D Input		
	Clock 1 or	2.0	
	Clock 2 Input	8.0	
	Any Output		10.0
SN54121/74121	A_1 and A_2 Inputs	1.0	
	B Input	2.0	
	Any Output		10.0
SN54145/74145	Any Input	1.0	
	Any Output		12.5
SN54150/74150	Any Input	1.0	
	Any Output		
	Logical 1		20.0
	Logical 0		10.0
SN54151/74151	Any Input	1.0	
	Any Output		
	Logical 1		20.0
	Logical 0		10.0
SN54152/74152	Any Input	1.0	
	Any Output		
	Logical 1		20.0
	Logical 0		10.0
SN54180/74180	Any Input	1.0	
	Any Output		
	Logical 1		20.0
	Logical 0		10.0

Design loading chart

SERIES 54/74

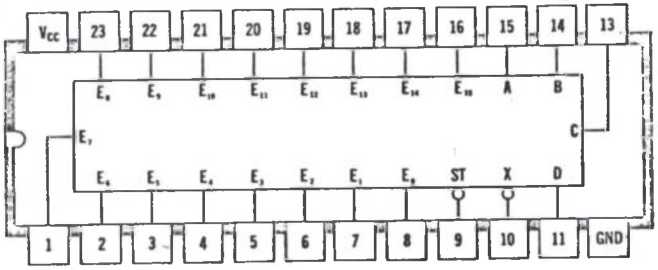
Device	Location	Normalized Input Factor	Normalized Output Factor
SN5400/7400	Any Input	1.0	
	Any Output		10.0
SN5401/7401	Any Input	1.0	
	Any Output		10.0
SN5402/7402	Any Input	1.0	
	Any Output		10.0
SN5403/7403	Any Input	1.0	
	Any Output		10.0
SN5404/7404	Any Input	1.0	
	Any Output		10.0
SN5405/7405	Any Input	1.0	
	Any Output		10.0
SN5410/7410	Any Input	1.0	
	Any Output		10.0
SN5420/7420	Any Input	1.0	
	Any Output		10.0
SN5430/7430	Any Input	1.0	
	Output		10.0
SN5440/7440	Any Input	1.0	
	Any Output		30.0
SN7441A	B, C, or D Input	1.0	
	A Input	2.0	
	Any Output		N/A
SN5442/7442	Any Input	1.0	
	Any Output		10.0
SN5443/7443	Any Input	1.0	
	Any Output		10.0
SN5444/7444	Any Input	1.0	
	Any Output		10.0
SN5445/7445	Any Input	1.0	
	Any Output		12.5
SN5446/7446	Any Input except		
	BI/RBO	1.0	
	BI/RBO Node	2.6	
	Any Output except		
	BI/RBO		12.5
	BI/RBO Node		5.0

SERIES 54/74

Device	Location	Normalized Input Factor	Normalized Output Factor
SN5447/7447	Any Input except		
	BI/RBO	1.0	
	BI/RBO Node	2.6	
	Any Output except		
	BI/RBO		12.5
	BI/RBO Node		5.0
SN5448/7448	Any Input except		
	BI/RBO	1.0	
	BI/RBO Node	2.6	
	Any Output except		
	BI/RBO		6.0
	BI/RBO Node		5.0
SN5449/7449	Any Input	1.0	
	Any Output		6.0
SN5450/7450	A, B, C, or D Input	1.0	
	X and $\bar{X}$ Input	N/A	
	Any Output		10.0
SN5451/7451	Any Input	1.0	
	Any Output		10.0
SN5453/7453	A, B, C, D, E, F, G, and H Input	1.0	
	X or $\bar{X}$ Input	N/A	
	Output		10.0
SN5454/7454	Any Input	1.0	
	Output		10.0
SN5460/7460	Any Input	1.0	
	X or $\bar{X}$ Output		N/A
SN5470/7470	$J_1, J_2, J^\star, K_1, K_2,$ or $K^\star$ Input	1.0	
	Clock Input	1.0	
	Preset or Clear Input	2.0	
	Q or $\bar{Q}$ Output		10.0
SN5472/7472	$J_1, J_2, J_3, K_1, K_2,$ or K_3 Inputs	1.0	
	Clock Input	2.0	
	Preset or Clear Inputs	2.0	
	Q or $\bar{Q}$ Output		10.0
SN5473/7473	J or K Input	1.0	
	Clock Input	2.0	
	Clear Input	2.0	
	Q or $\bar{Q}$ Output		10.0
SN5474/7474	D Input	1.0	
	Clock Input	2.0	
	Preset Input	2.0	
	Clear Input	3.0	
	Q or $\bar{Q}$ Output		10.0

SN54150N/SN74150N

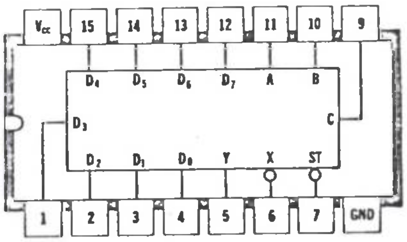
16-bit data selector/multiplexer



Propagation delay — 20 nsec
Power dissipation — 210 mW
Fan out — 10 Series 54/74 loads

SN54151N/SN74151N
SN54151J/SN74151J

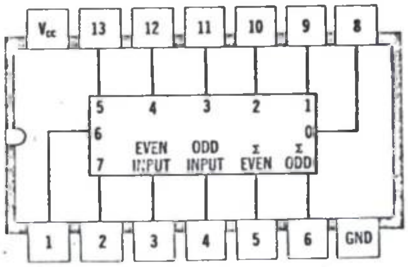
8-bit data selector/multiplexer



Propagation delay — 20 nsec
Power dissipation — 140 mW
Fan out — 10 Series 54/74 loads

SN54180N/SN74180N
SN54180J/SN74180J

8-bit parity generator/checker



Propagation delay
(data to output) — 40 nsec
(control inputs to output) — 10 nsec
Power dissipation — 170 mW
Fan out — 10 Series 54/74 loads

SWITCHING CHARACTERISTICS
($T_A = 25°C$)

FIGURE 6 — TURN-ON DELAY TIME

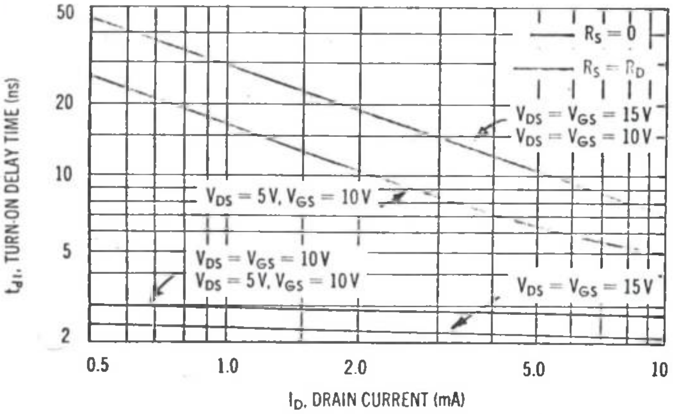


FIGURE 7 — RISE TIME

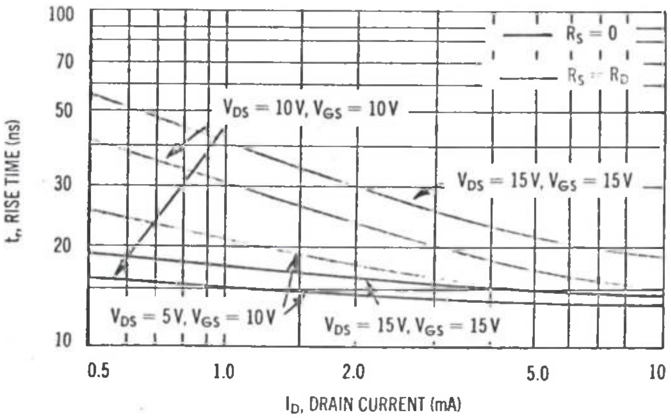


FIGURE 8 — TURN-OFF DELAY TIME

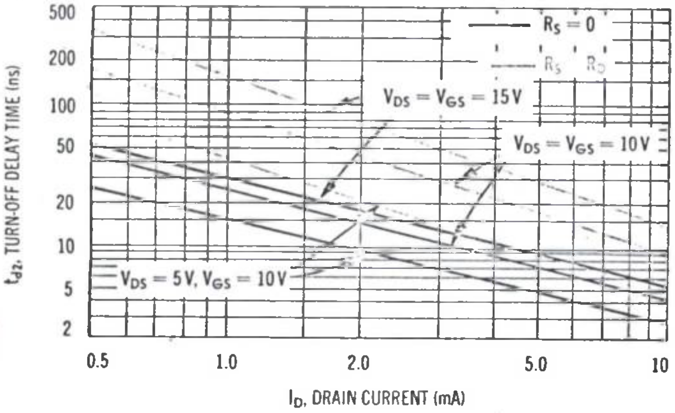


FIGURE 9 — FALL TIME

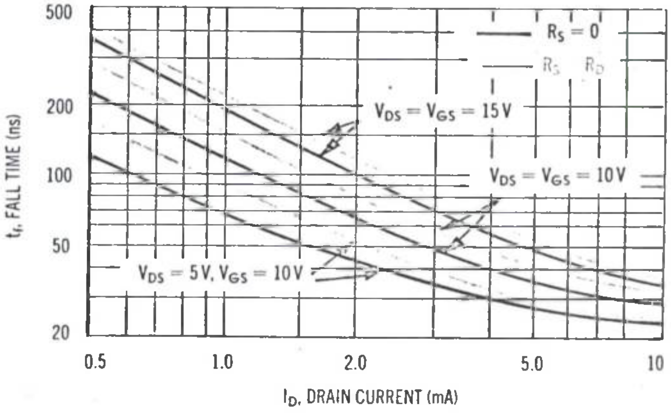
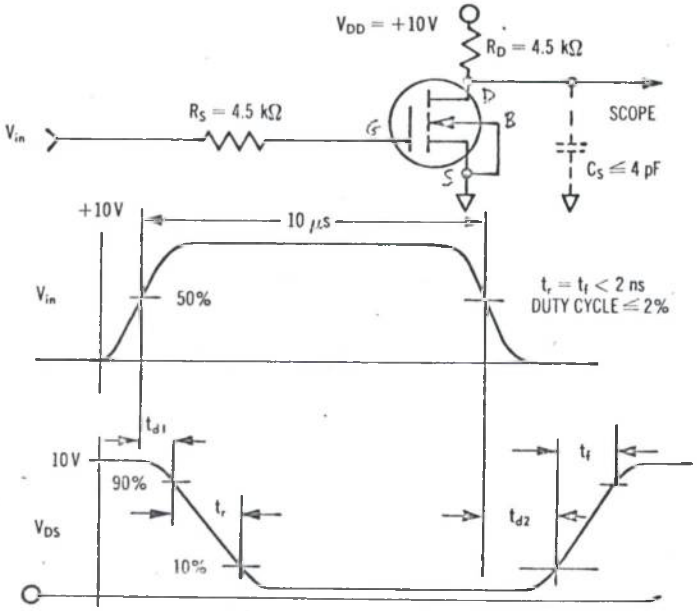


FIGURE 10 — SWITCHING CIRCUIT and WAVEFORMS



The switching characteristics shown above were measured in a test circuit similar to Figure 10. At the beginning of the switching interval, the gate voltage is at ground and the gate-source capacitance ($C_{gs} = C_{iss} - C_{rss}$) has no charge. The drain voltage is at V_{DD}, and thus the feedback capacitance (C_{rss}) is charged to V_{DD}. Similarly, the drain-substrate capacitance ($C_{d(sub)}$) is charged to V_{DD} since the substrate and source are connected to ground.

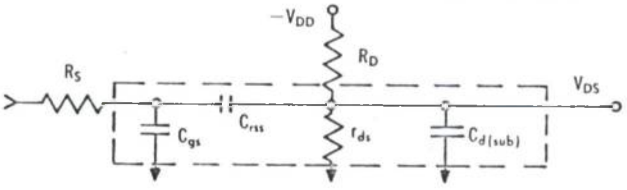
During the turn-on interval, C_{gs} is charged to V_{GS} (the input voltage) through R_S (generator impedance) (Figure 11). C_{rss} must be discharged to $V_{GS} - V_{D(on)}$ through R_S and the parallel combination of the load resistor (R_D) and the channel resistance (r_{ds}). In addition, $C_{d(sub)}$ is discharged to a low value ($V_{D(on)}$) through R_D in parallel with r_{ds}. During turn-off this charge flow is reversed.

Predicting turn-on time proves to be somewhat difficult since the channel resistance (r_{ds}) is a function of the gate-source voltage (V_{GS}). As C_{gs} becomes charged V_{GS} is approaching V_{in} and r_{ds} decreases (see Figure 4) and since C_{rss} and $C_{d(sub)}$ are charged through r_{ds}, turn-on time is quite non-linear.

If the charging time of C_{gs} is short compared to that of C_{rss} and $C_{d(sub)}$, then r_{ds} (which is in parallel with R_D) will be low compared to R_D during the switching interval and will largely determine the turn-on time. On the other hand, during turn-off r_{ds} will be almost an open circuit requiring C_{rss} and $C_{d(sub)}$ to be charged through R_D and resulting in a turn-off time that is long compared to the turn-on time. This is especially noticeable for the curves where $R_S = 0$ and C_{gs} is charged through the pulse generator impedance only.

The switching curves shown with $R_S = R_D$ simulate the switching behavior of cascaded stages where the driving source impedance is normally the same as the load impedance. The set of curves with $R_S = 0$ simulates a low source impedance drive such as might occur in complementary logic circuits.

FIGURE 11 — SWITCHING CIRCUIT with IGFET EQUIVALENT MODEL



MOTOROLA Semiconductor Products Inc.
BOX 955 • PHOENIX, ARIZONA 85001 • A SUBSIDIARY OF MOTOROLA INC.

FIGURE 3 — TRANSFER CHARACTERISTICS

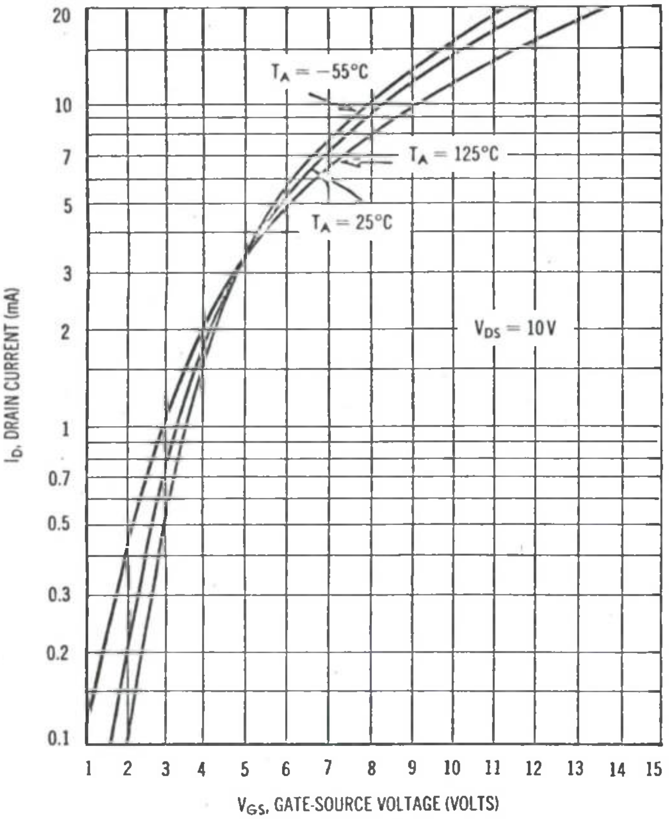


FIGURE 4 — DRAIN-SOURCE "ON" RESISTANCE

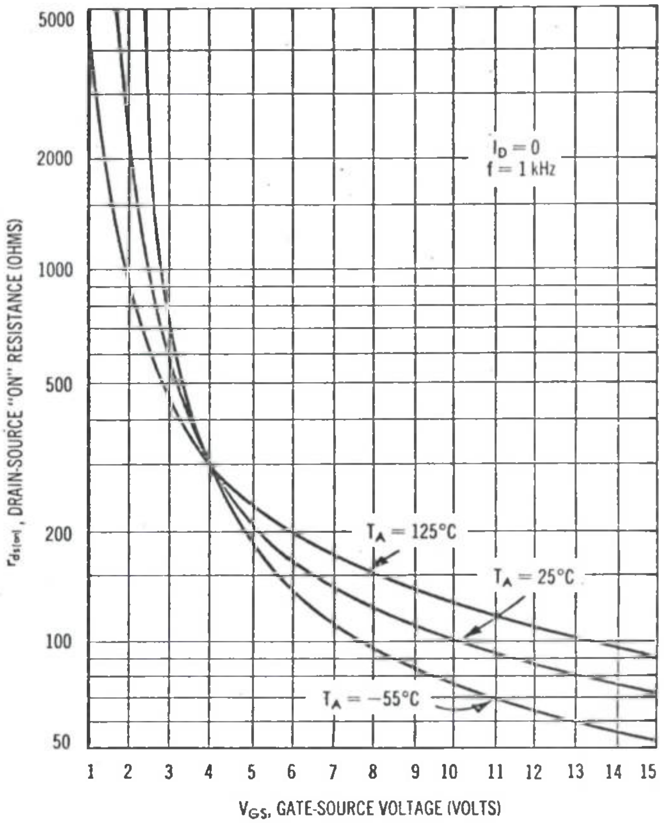
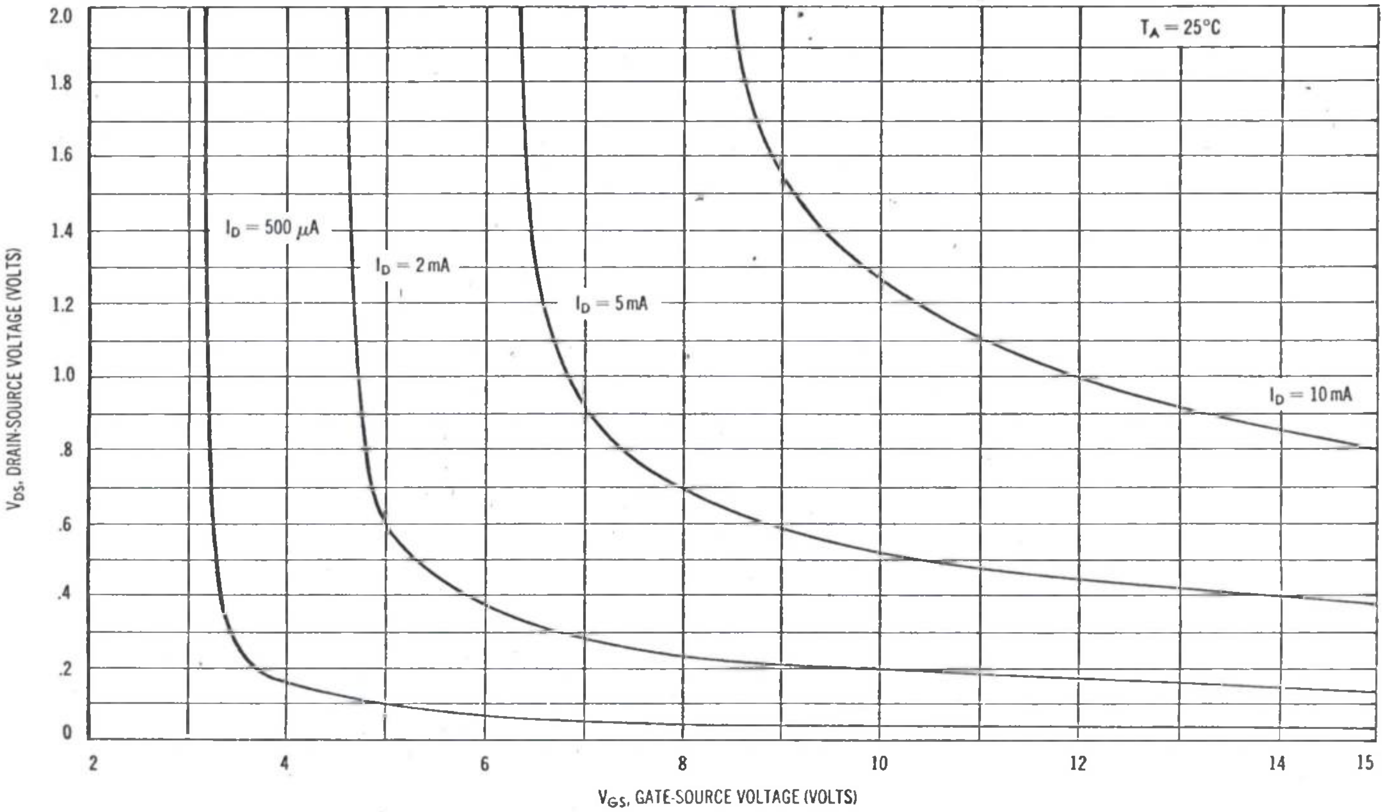


FIGURE 5 — "ON" DRAIN-SOURCE VOLTAGE



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Substrate connected to source.

Characteristic	Figure No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = 10 μA, V_{GS} = 0)	—	$V_{(BR)DSS}$	25	—	Vdc
Gate Leakage Current (V_{GS} = ±25 V, V_{DS} = 0)	—	I_{GSS}	—	±10	pAdc
Zero-Gate-Voltage Drain Current (V_{DS} = 10 V, V_{GS} = 0)	—	I_{DSS}	—	10	nAdc
ON CHARACTERISTICS					
Gate-Source Threshold Voltage (V_{DS} = 10 V, I_D = 10 μA)	—	$V_{GS(TH)}$	1.0	5	Vdc
"ON" Drain Current (V_{GS} = 10 V, V_{DS} = 10 V)	3	$I_{D(on)}$	3	—	mAdc
Drain-Source "ON" Voltage (I_D = 2 mA, V_{GS} = 10 V)	—	$V_{DS(on)}$	—	1.0	V
SMALL SIGNAL CHARACTERISTICS					
Drain-Source Resistance (V_{GS} = 10 V, I_D = 0, f = 1 kHz)	4	$r_{ds(on)}$	—	300	ohms
Forward Transfer Admittance (V_{DS} = 10 V, I_D = 2 mA, f = 1 kHz)	1	$\|y_{fs}\|$	1000	—	μmho
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 0, f = 140 kHz)	2	C_{rss}	—	2.5	pF
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 140 kHz)	2	C_{iss}	—	5.5	pF
Drain-Substrate Capacitance ($V_{D(SUB)}$ = 10 V, f = 140 kHz)	—	$C_{d(sub)}$	—	4.0	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Figure No.	Symbol	Min	Max	Unit
Turn-On Delay	I_D = 2 mA, V_{DD} = 10 V, V_{GS} = 10 V, R_D = R_S = 4.5 k ohms (See Figure 10; Times Circuit Determined)	6, 10	t_{d1}	—	45	ns
Rise Time		7, 10	t_r	—	65	ns
Turn-Off Delay		8, 10	t_{d2}	—	35	ns
Fall Time		9, 10	t_f	—	75	ns

FIGURE 1 — FORWARD TRANSFER ADMITTANCE

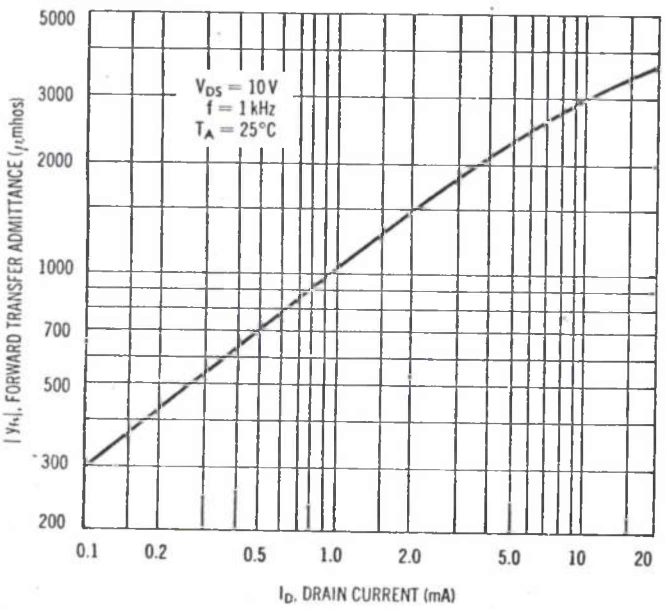
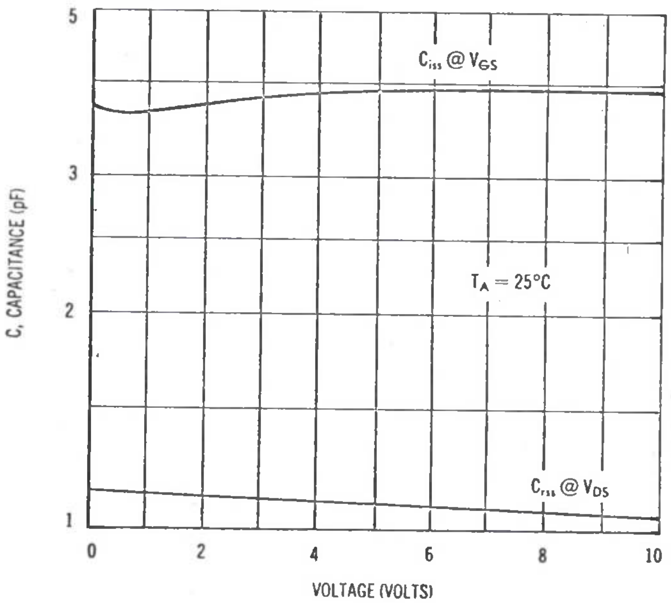


FIGURE 2 — CAPACITANCE



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2N4351

N-CHANNEL
INSULATED GATE

170

FIELD-EFFECT
TRANSISTOR

AUGUST 1966 — DS 5179

SILICON N-CHANNEL INSULATED GATE FIELD EFFECT TRANSISTOR

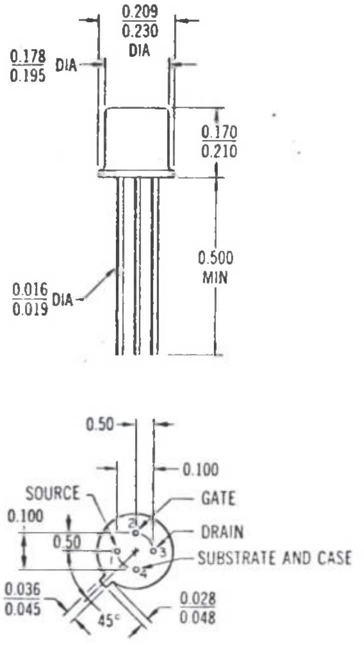
. . . designed for enhancement-mode operation in low-power switching applications.

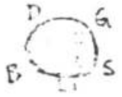
- Low Drain-Source Resistance
  $r_{ds(on)}$ = 300 ohms max
- Low Reverse Transfer Capacitance
  C_{rss} = 2.5 pF max
- Guaranteed Switching Limits
  t_{d1}, t_r, t_{d2}, t_f

IN STOCK
MOTOROLA from HAMILTON
UPton 0-7171

MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	±35	Vdc
Gate-Source Voltage	V_{GS}	±35	Vdc
Drain Current	I_D	30	mAdc
Power Dissipation at T_A = 25°C Derate above 25°C	P_D	300 1.7	mW mW/°C
Power Dissipation at T_C = 25°C Derate about 25°C	P_D	800 4.56	mW mW/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature	T_{stg}	-65 to +200	°C





TO-72 PACKAGE

HANDLING CONSIDERATIONS:

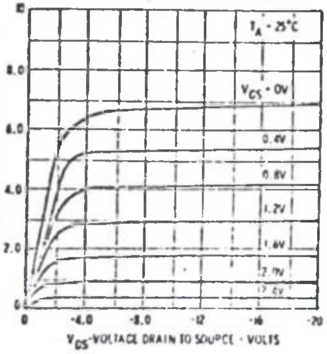
Insulated gate field-effect transistors, due to their extremely high input resistance, are subject to potential damage by the accumulation of excess static charge. To avoid possible damage to the devices while handling, testing, or in actual operation, the following procedure should be followed:

1. The leads of the devices should remain wrapped in the shipping foil except when being tested or in actual operation to avoid the build-up of static charge.
2. Avoid unnecessary handling; when handled, the devices should be picked up by the can instead of the leads.
3. The devices should not be inserted or removed from circuits with the power on as transient voltages may cause permanent damage to the devices.

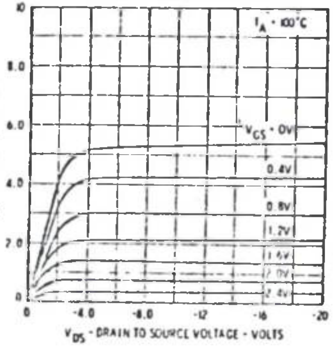
TYPICAL ELECTRICAL CHARACTERISTICS (Note 3)

2N4342

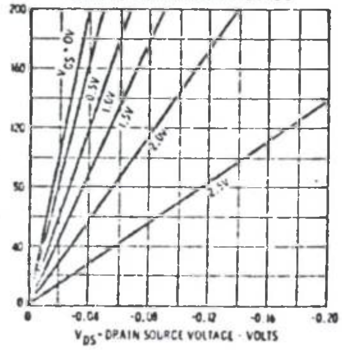
DRAIN CHARACTERISTICS



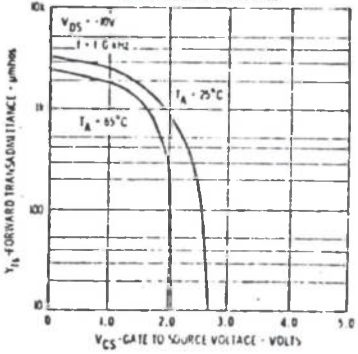
DRAIN CHARACTERISTICS



LOW VOLTAGE DRAIN CHARACTERISTICS

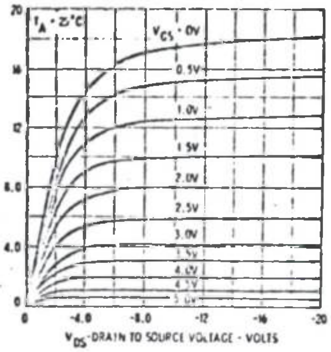


FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE

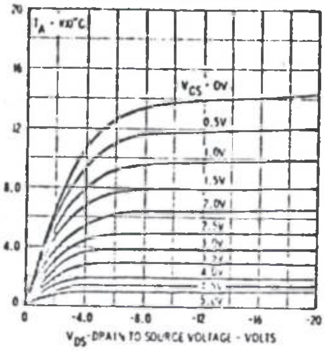


2N4343

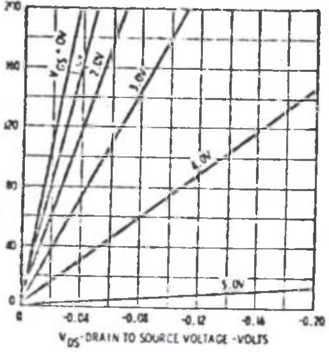
DRAIN CHARACTERISTICS



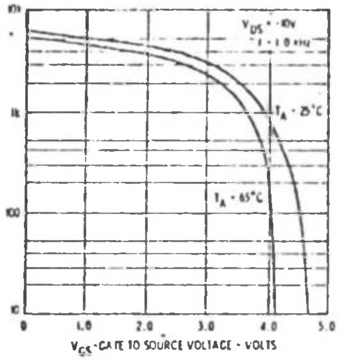
DRAIN CHARACTERISTICS



LOW VOLTAGE DRAIN CHARACTERISTICS

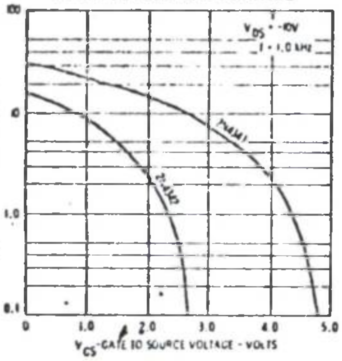


FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE

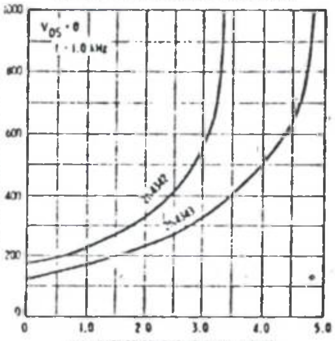


2N4342-2N4343

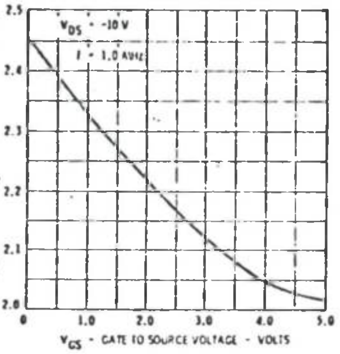
OUTPUT ADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



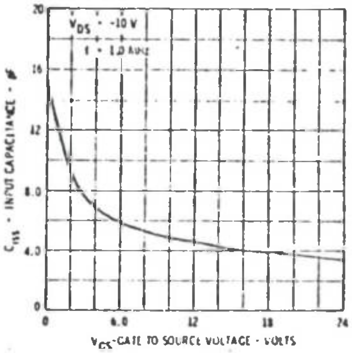
DRAIN RESISTANCE VERSUS GATE TO SOURCE VOLTAGE



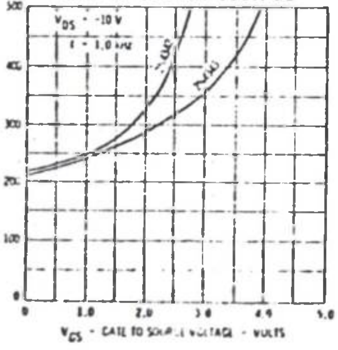
REVERSE TRANSFER CAPACITANCE VERSUS GATE TO SOURCE VOLTAGE



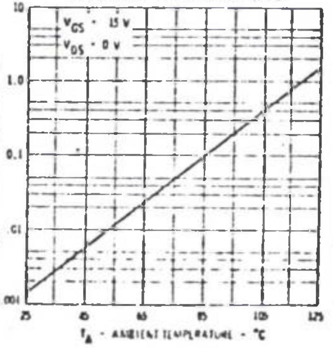
INPUT CAPACITANCE VERSUS GATE TO SOURCE VOLTAGE



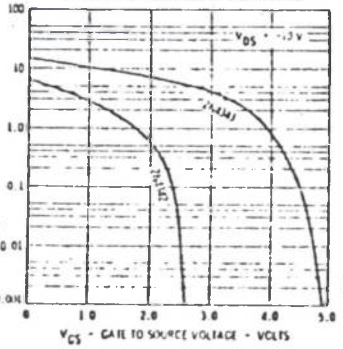
AMPLIFICATION FACTOR VERSUS GATE TO SOURCE VOLTAGE



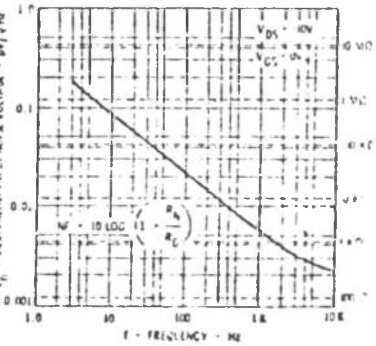
GATE REVERSE CURRENT VERSUS AMBIENT TEMPERATURE



DRAIN CURRENT VERSUS GATE TO SOURCE VOLTAGE



EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



2.15 1.90 .95

JULY 19

2N4342 · 2N4343 · 2N436

P-CHANNEL FIELD-EFFECT TRANSISTORS

DIFFUSED SILICON PLANAR* TRANSISTORS

- LOW NOISE VOLTAGE – 0.08 μV/√Hz (MAX) @ 100 Hz
- HIGH Y_{fs} – 4000 μmhos (MIN)
- LOW r_{DS} (on) – 350 Ω (MAX)
- LOW COST EPOXY PACKAGE

HYER
Denver 771-5285
Albuquerque 265-5767
Phoenix 264-0231
Salt Lake Cit 363-6773

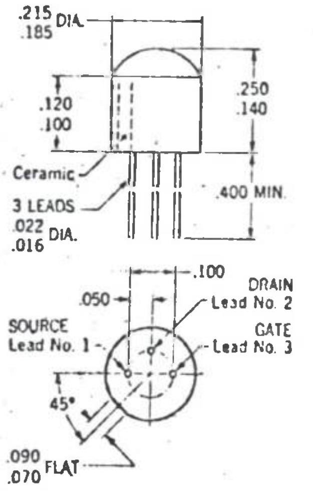
ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures	
Operating Junction Temperature	125°C
Storage Temperature	-55°C to +125°C
Soldering Temperature (10 seconds time limit)	260°C
Maximum Power Dissipation	
Total Dissipation at 25°C Case Temperature (Note 2)	0.5 Watt
at 65°C Case Temperature (Note 2)	0.3 Watt
at 25°C Ambient Temperature (Note 2)	0.2 Watt

Maximum Voltages

		2N4360	2N4342 2N4343
BV_{SGO}	Source to Gate Breakdown Voltage	-20 Volts	-25 Volts
BV_{DSO}	Drain to Source Breakdown Voltage	-20 Volts	-25 Volts
BV_{DGO}	Drain to Gate Breakdown Voltage	-20 Volts	-25 Volts

PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Characteristic	2N4360 Min.	2N4360 Typ.	2N4360 Max.	2N4342 Min.	2N4342 Typ.	2N4342 Max.	2N4343 Min.	2N4343 Typ.	2N4343 Max.	Units	Test Conditions
e_n	Equivalent Input Noise Voltage (f = 100 Hz)		0.02	0.08		0.02	0.08		0.02	0.08	μV/√Hz	V_{DS} = -10 V V_{GS} = 0
NF	Noise Figure (f = 100 Hz)		0.1	1.5		0.1	1.5		0.1	1.5	dB	V_{DS} = -10 V V_{GS} = 0 R_G = 1.0 MΩ BW = 15 Hz
Y_{fs}	Forward Transadmittance (f = 1.0 kHz)	2000	4000	8000	2000	3500	6000	4000	6000	8000	μmhos	V_{DS} = -10 V V_{GS} = 0
Y_{os}	Output Admittance (f = 1.0 kHz)		35	100		25	75		35	100	μmhos	V_{DS} = -10 V V_{GS} = 0
BV_{GSS}	Gate to Source Breakdown Voltage	20			25			25			Volts	I_G = 10 μA V_{DS} = 0
I_{DSS}	Drain Current	3.0	10	30	4.0	7.0	12	10	18	30	mA	V_{DS} = -10 V V_{GS} = 0
V_{GS}	Gate to Source Voltage	0.7	5.0	9.0							Volts	V_{DS} = -10 V I_D = 0.3 mA
V_{GS}	Gate to Source Voltage				0.7	3.0	5.0				Volts	V_{DS} = -10 V I_D = 0.4 mA
V_{GS}	Gate to Source Voltage							1.8	6.0	9.0	Volts	V_{DS} = -10 V I_D = 1.0 mA
V_{GS} (off)	Gate to Source Cutoff Voltage			10			5.5			10	Volts	V_{DS} = -10 V I_D = 1.0 μA
I_{GSS}	Gate Reverse Current		0.15	10		0.15	10		0.15	10	nA	V_{GS} = 15 V V_{DS} = 0
I_{GSS}(65°C)	Gate Reverse Current		.002	0.5		0.002	0.5		0.002	0.5	μA	V_{GS} = 15 V V_{DS} = 0
C_{iss}	Input Capacitance (f = 1.0 MHz)		15	20		15	20		15	20	pF	V_{DS} = -10 V V_{GS} = 0
C_{rss}	Reverse Transfer Capacitance (f = 1.0 MHz)		3.0	5.0		3.0	5.0		3.0	5.0	pF	V_{DS} = -10 V V_{GS} = 0
r_{DS}(on)	Drain "On" Resistance (f = 1.0 kHz)		350	700		300	700		180	350	Ohms	I_D = 0 V_{GS} = 0
$R_e(Y_{fs})$	Forward Transconductance (f = 1.0 MHz)	1500	3000		1500	2500		3000	5500		μmhos	V_{DS} = -10 V V_{GS} = 0

NOTES:

*Planar is a patented Fairchild process.

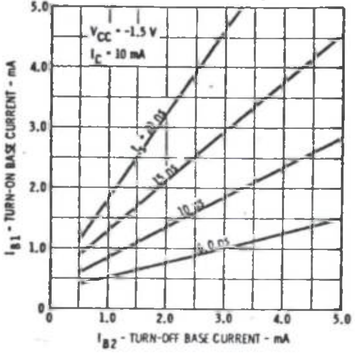
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C); junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).

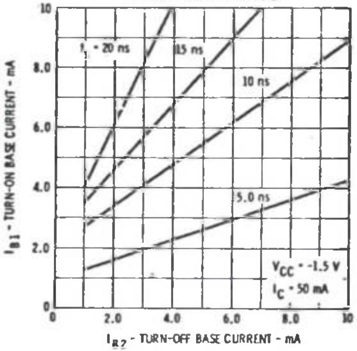
(3) Both 2N4342 and 2N4343 typical curves apply to 2N4360.

TYPICAL ELECTRICAL CHARACTERISTICS

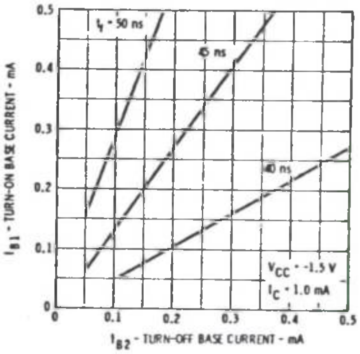
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



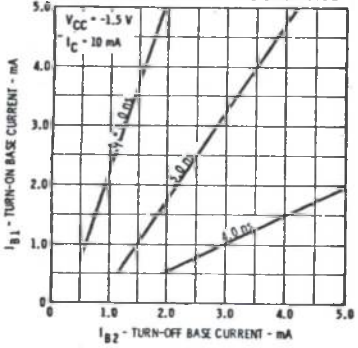
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



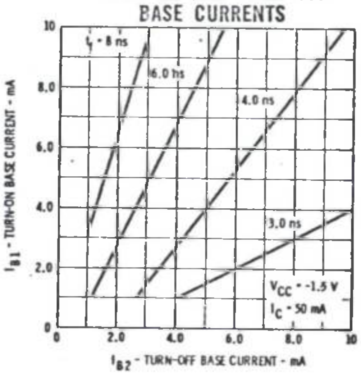
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



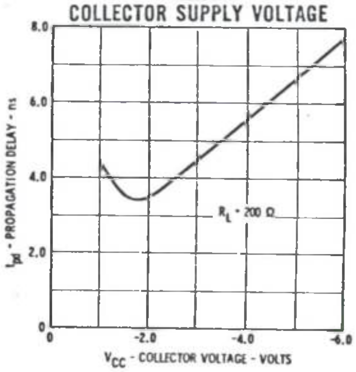
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



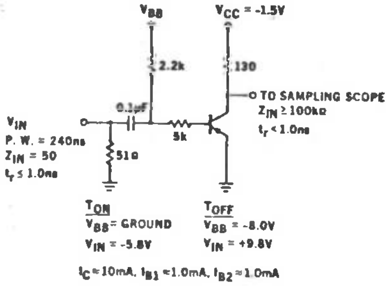
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



PROPAGATION DELAY TIME VERSUS COLLECTOR SUPPLY VOLTAGE



TURN ON AND TURN OFF TEST CIRCUIT

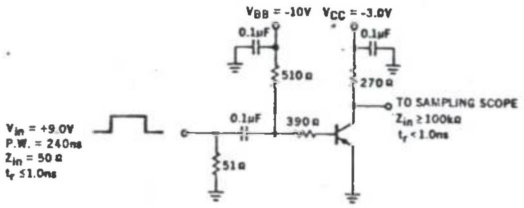


T_{ON}
V_{BB} = GROUND
V_{IN} = -5.8V

T_{OFF}
V_{BB} = -8.0V
V_{IN} = +9.8V

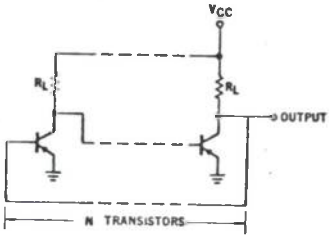
$I_C \approx 10mA$, $I_{B1} \approx 1.0mA$, $I_{B2} \approx 1.0mA$

CHARGE STORAGE TIME TEST CIRCUIT



$I_C \approx 10mA$, $I_{B1} \approx 10mA$, $I_{B2} \approx -10mA$

FIVE STAGE RING OSCILLATOR FOR MEASUREMENT OF PROPAGATION DELAY



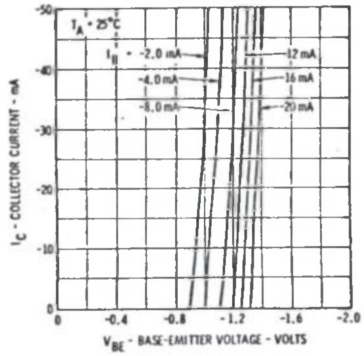
$$t_{pd} = \frac{1}{2Nf_{osc}}$$

NOTES:

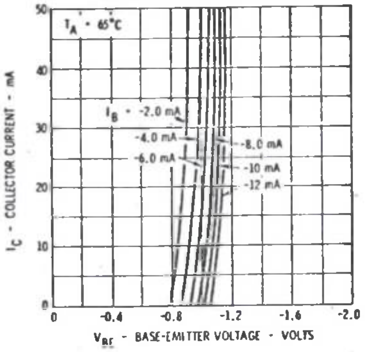
(1) These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
(3) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 200°C/watt (derating factor of 5.0 mW/°C); junction-to-ambient thermal resistance of 500°C/watt (derating factor of 2.0 mW/°C).
(4) This rating refers to a high-current point where collector-to-emitter voltage is lowest.
(5) Pulse Conditions: length = 300 µsec; duty cycle = 1%.
(6) See switching circuit for exact values of I_C, I_{B1} and I_{B2}.

TYPICAL ELECTRICAL CHARACTERISTICS

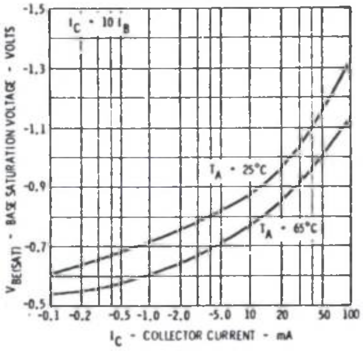
BASE CHARACTERISTICS*



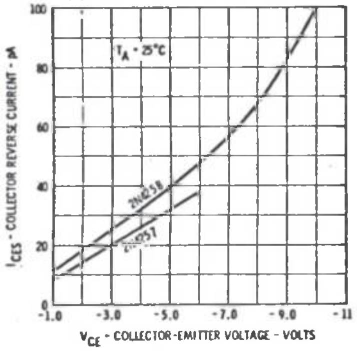
BASE CHARACTERISTICS*



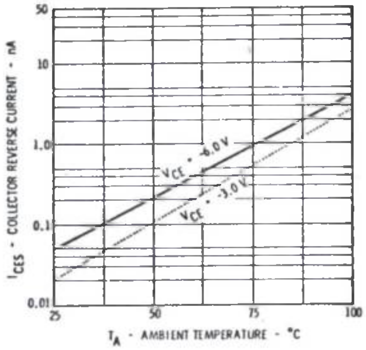
BASE SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



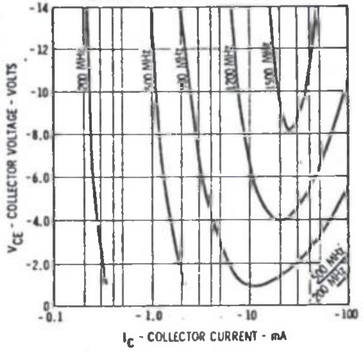
COLLECTOR REVERSE CURRENT VERSUS COLLECTOR-EMITTER VOLTAGE



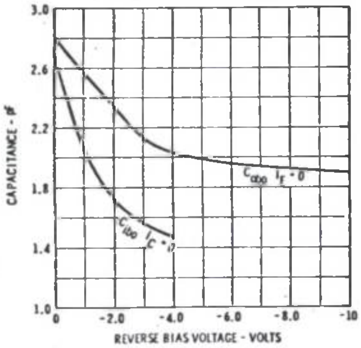
COLLECTOR REVERSE CURRENT VERSUS AMBIENT TEMPERATURE



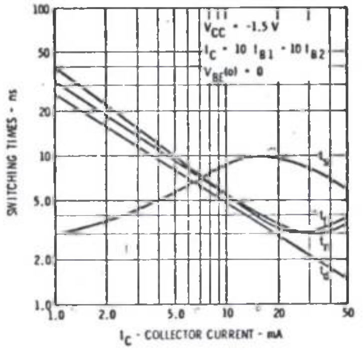
CONTOURS OF CONSTANT GAIN BANDWIDTH PRODUCT (f_T)



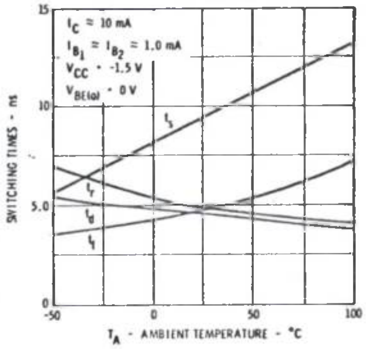
INPUT AND OUTPUT CAPACITANCE VERSUS REVERSE BIAS VOLTAGE



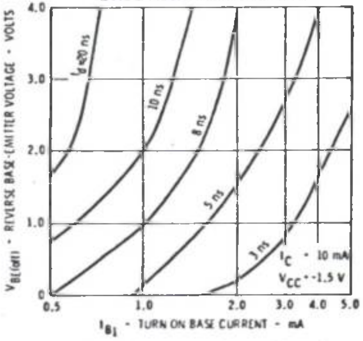
SWITCHING TIMES VERSUS COLLECTOR CURRENT



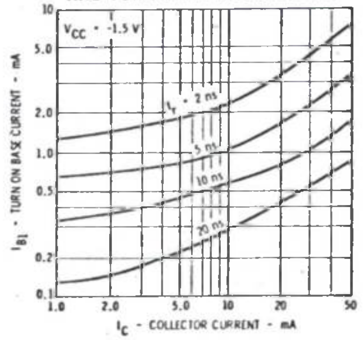
SWITCHING TIMES VERSUS AMBIENT TEMPERATURE



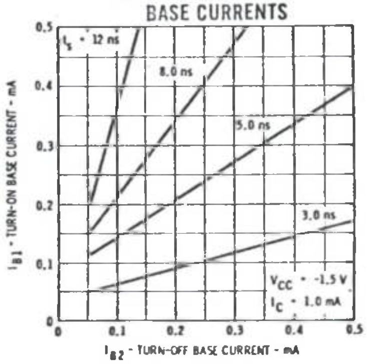
DELAY TIME VERSUS TURN ON BASE CURRENT AND REVERSE BASE EMITTER VOLTAGE



RISE TIME VERSUS COLLECTOR AND TURN ON BASE CURRENTS



STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



* Single family characteristic on Transistor Curve Tracer.

FAIRCHILD TRANSISTORS 2N4257 • 2N4258

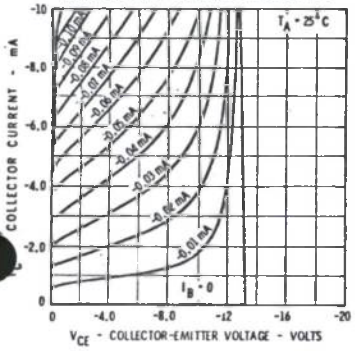
ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N4257 MIN.	 TYP.	 MAX.	2N4258 MIN.	 TYP.	 MAX.	UNITS	TEST CONDITIONS	
V_{BE} (sat)	Pulsed Base Saturation Voltage [Note 5]	−0.8	−0.88	−0.95	−0.8	−0.88	−0.95	Volts	$I_C = 10$ mA	$I_B = 1.0$ mA
V_{BE} (sat)	Pulsed Base Saturation Voltage [Note 5]		−1.16	−1.5		−1.16	−1.5	Volts	$I_C = 50$ mA	$I_B = 5.0$ mA
I_{CES}	Collector Reverse Current		0.02	10				nA	$V_{CE} = -3.0$ V	$V_{BE} = 0$
I_{CES}	Collector Reverse Current					0.02	10	nA	$V_{CE} = -6.0$ V	$V_{BE} = 0$
I_{CES} (+65°C)	Collector Reverse Current		0.3	5.0				μA	$V_{CE} = -3.0$ V	$V_{BE} = 0$
I_{CES} (+65°C)	Collector Reverse Current					0.5	5.0	μA	$V_{CE} = -6.0$ V	$V_{BE} = 0$
V_{CEO} (sust)	Collector to Emitter Sustaining Voltage [Notes 4 and 5]	−6.0			−12			Volts	$I_C = 3.0$ mA	$I_B = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	−4.5			−4.5			Volts	$I_C = 0$	$I_E = 100$ μA
BV_{CES}	Collector to Emitter Breakdown Voltage	−6.0			−12			Volts	$I_C = 100$ μA	$V_{BE} = 0$
BV_{CBO}	Collector to Base Breakdown Voltage	−6.0			−12			Volts	$I_C = 100$ μA	$I_E = 0$

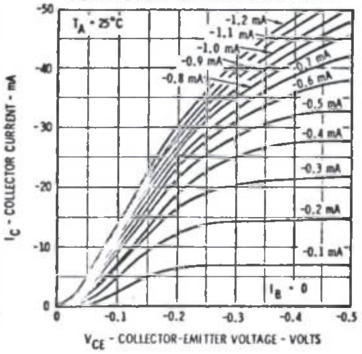
TYPICAL ELECTRICAL CHARACTERISTICS

2N4257

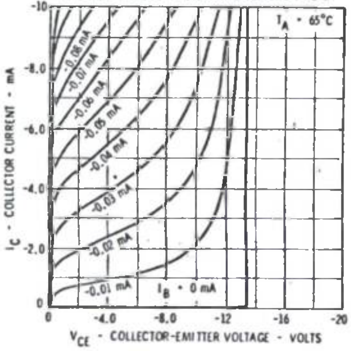
COLLECTOR CHARACTERISTICS*



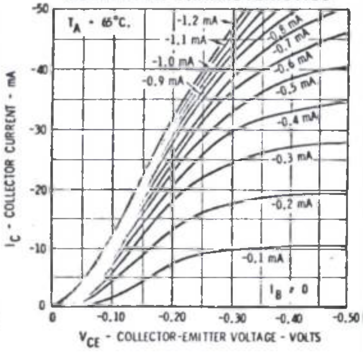
COLLECTOR CHARACTERISTICS*



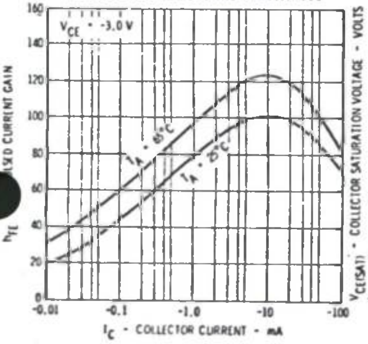
COLLECTOR CHARACTERISTICS*



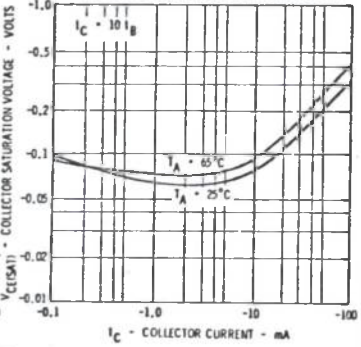
COLLECTOR CHARACTERISTICS*



DC PULSED CURRENT GAIN VERSUS COLLECTOR CURRENT

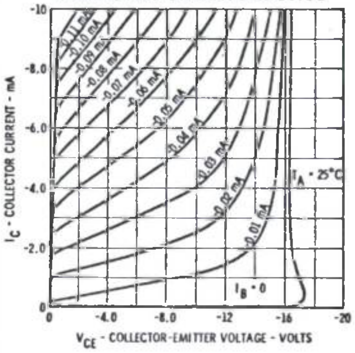


COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT

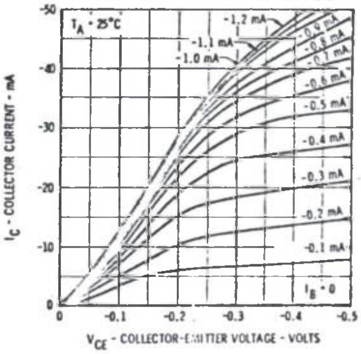


2N4258

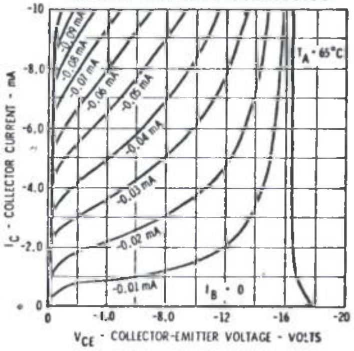
COLLECTOR CHARACTERISTICS*



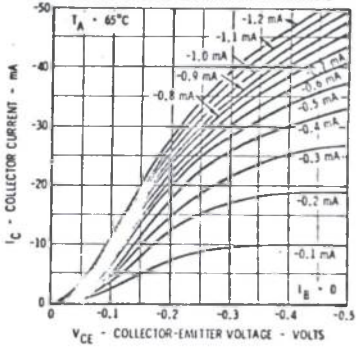
COLLECTOR CHARACTERISTICS*



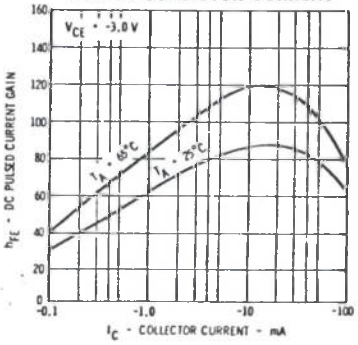
COLLECTOR CHARACTERISTICS*



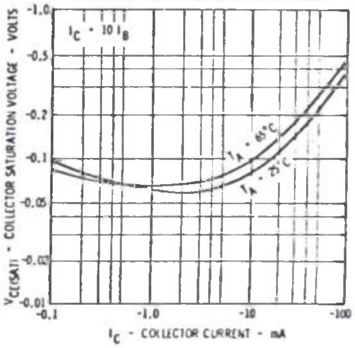
COLLECTOR CHARACTERISTICS*



DC PULSED CURRENT GAIN VERSUS COLLECTOR CURRENT



COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



* Single family characteristic on Transistor Curve Tracer.

2N4257 • 2N4258

PNP ULTRA HIGH-SPEED LOGIC SWITCHES

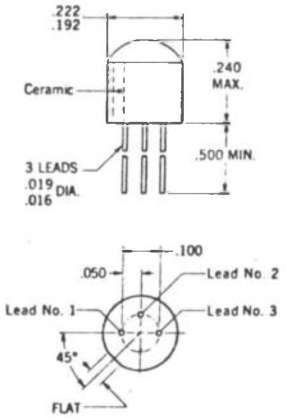
SILICON PLANAR* EPITAXIAL TRANSISTORS

FEATURES

- LOW STORAGE TIME — τ_s = 20 ns (Max).
- LOW CAPACITANCE — C_{obo} = 3.0 pF (Max), C_{ibo} = 3.5 pF (Max).
- HIGH FREQUENCY — f_T = 700 MHz (Min).
- LOW SATURATION VOLTAGE — V_{CE} (sat) = −0.15 V (Max) @ I_C = 10 mA

* Planar is a patented Fairchild process.

PHYSICAL DIMENSIONS
Epoxy package
TO-106



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram

ABSOLUTE MAXIMUM RATINGS [Note 1]

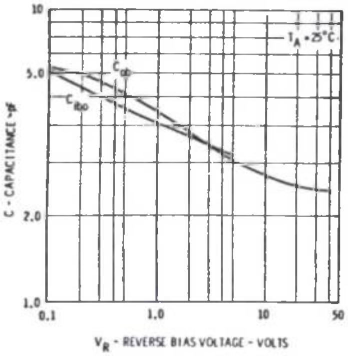
Maximum Temperatures			
Storage Temperature			−55°C to +125°C
Operating Junction Temperature			+125°C Maximum
Lead Temperature (Soldering, 10 seconds time limit)			+260°C Maximum
Maximum Power Dissipation			
Total Dissipation at 25°C Case Temperatures [Notes 2 and 3]			0.5 Watt
at 25°C Free Air Temperature [Notes 2 and 3]			0.2 Watt
Maximum Voltages		2N4257	2N4258
V_{CBO}	Collector to Base Voltage	−6.0 Volts	−12 Volts
V_{CEO}	Collector to Emitter Voltage [Note 4]	−6.0 Volts	−12 Volts
V_{EBO}	Emitter to Base Voltage	−4.5 Volts	−4.5 Volts

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

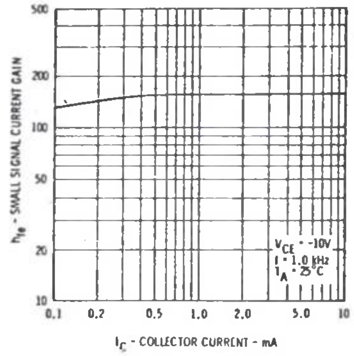
SYMBOL	CHARACTERISTIC	2N4257 MIN.	TYP.	MAX.	2N4258 MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
τ_s	Charge Storage Time [Note 6]		11	15		13	20	ns	$I_C \approx$ 10 mA	$I_{B1} \approx$ 10 mA $I_{B2} \approx$ −10 mA
t_{on}	Turn On Time [Note 6]		9.0	15		9.0	15	ns	$I_C \approx$ 10 mA	$I_{B1} \approx$ 1.0 mA
t_{off}	Turn Off Time [Note 6]		12	15		14	20	ns	$I_C \approx$ 10 mA	$I_{B1} \approx$ 1.0 mA $I_{B2} \approx$ −1.0 mA
h_{fe}	High Frequency Current Gain (f = 100 MHz)	5.0	11						I_C = 10 mA	V_{CE} = −5.0 V
h_{fe}	High Frequency Current Gain (f = 100 MHz)				7.0	13			I_C = 10 mA	V_{CE} = −10 V
C_{obo}	Common Base, Open Circuit Output Capacitance		2.0	3.0		2.0	3.0	pF	V_{CB} = −5.0 V	I_E = 0
C_{ibo}	Common Base, Open Circuit Input Capacitance		2.4	3.5		2.4	3.5	pF	I_C = 0	V_{EB} = −0.5 V
h_{FE}	DC Pulse Current Gain [Note 5]	15	40		15	40			I_C = 1.0 mA	V_{CE} = −0.5 V
h_{FE}	DC Pulse Current Gain [Note 5]	30	67	120	30	67	120		I_C = 10 mA	V_{CE} = −0.3 V
h_{FE}	DC Pulse Current Gain [Note 5]	30	80		30	80			I_C = 50 mA	V_{CE} = −1.0 V
V_{CE} (sat)	Pulsed Collector Saturation Voltage [Note 5]		−0.08	−0.15		−0.08	−0.15	Volts	I_C = 10 mA	I_B = 1.0 mA
V_{CE} (sat)	Pulsed Collector Saturation Voltage [Note 5]		−0.2	−0.5		−0.2	−0.5	Volts	I_C = 50 mA	I_B = 5.0 mA

TYPICAL ELECTRICAL CHARACTERISTICS

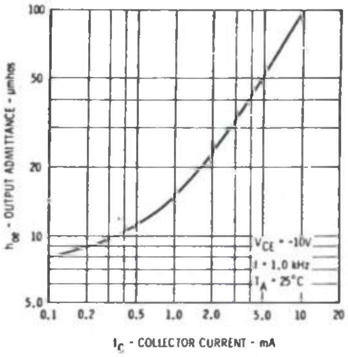
CAPACITANCE VERSUS REVERSE BIAS VOLTAGE



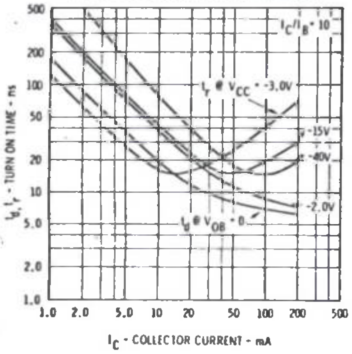
SMALL SIGNAL CURRENT GAIN VERSUS COLLECTOR CURRENT



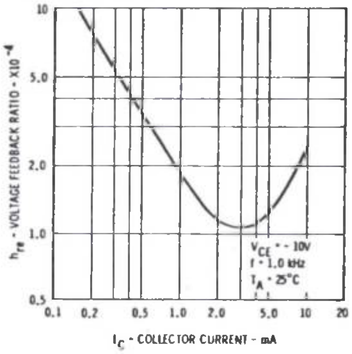
OUTPUT ADMITTANCE VERSUS COLLECTOR CURRENT



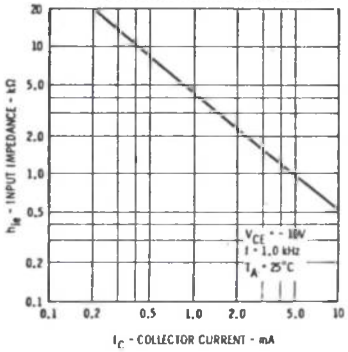
TURN ON TIME VERSUS COLLECTOR CURRENT



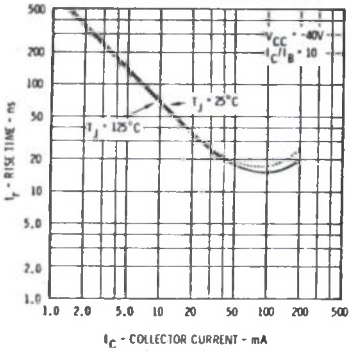
VOLTAGE FEEDBACK RATIO VERSUS COLLECTOR CURRENT



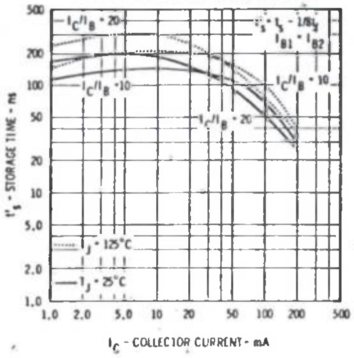
INPUT IMPEDANCE VERSUS COLLECTOR CURRENT



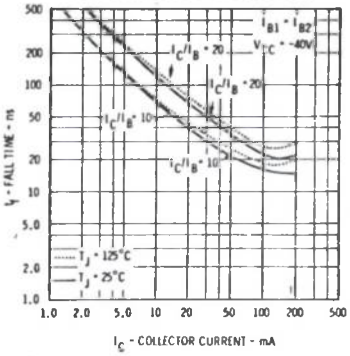
RISE TIME VERSUS COLLECTOR CURRENT



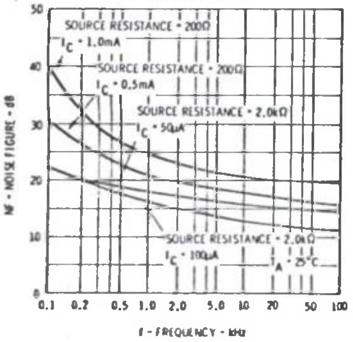
STORAGE TIME VERSUS COLLECTOR CURRENT



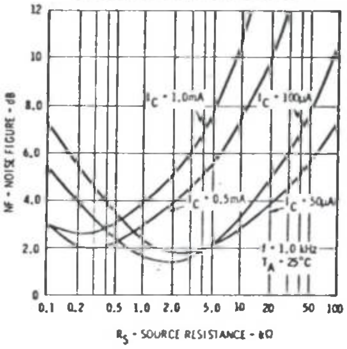
FALL TIME VERSUS COLLECTOR CURRENT



NOISE FIGURE VERSUS FREQUENCY



NOISE FIGURE VERSUS SOURCE RESISTANCE



"ON" VOLTAGE VERSUS COLLECTOR CURRENT

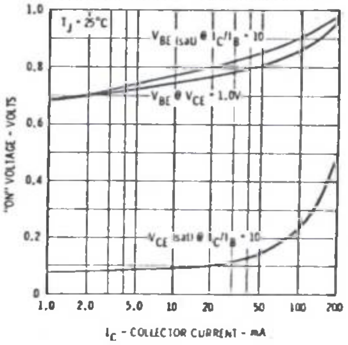


FIGURE 1 – DELAY AND RISE TIME EQUIVALENT TEST CIRCUIT

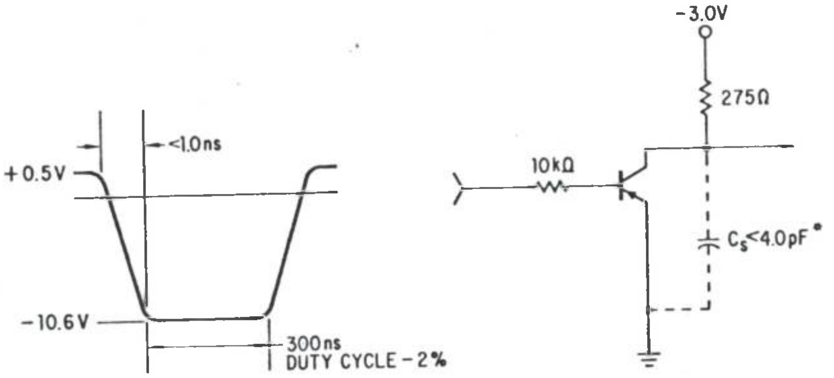
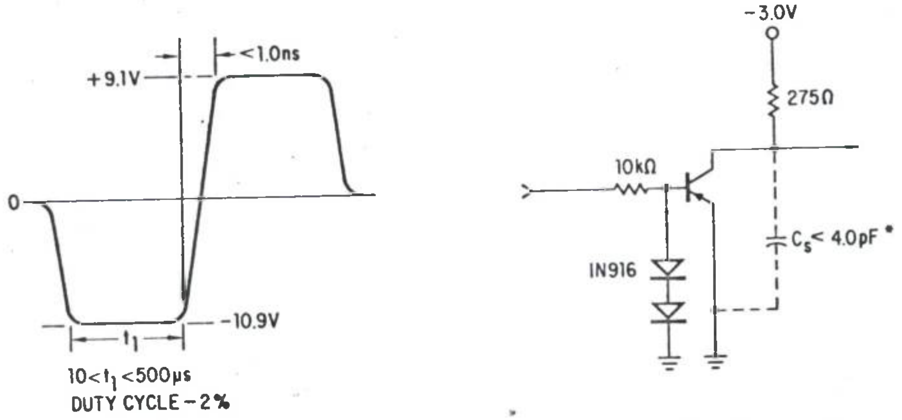


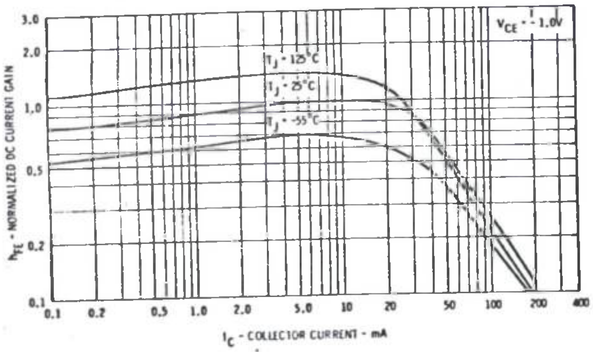
FIGURE 2 – STORAGE AND FALL TIME EQUIVALENT TEST CIRCUIT



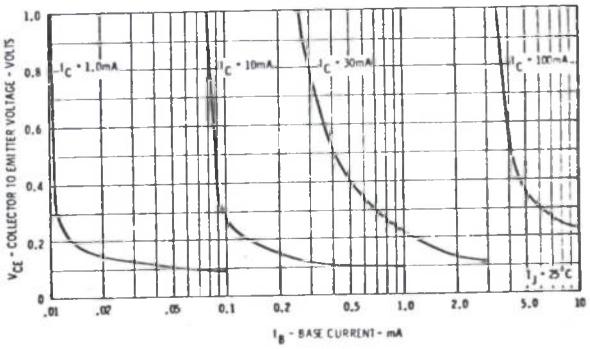
* Total shunt capacitance of test jig and connectors

TYPICAL ELECTRICAL CHARACTERISTICS

NORMALIZED DC CURRENT GAIN VERSUS COLLECTOR CURRENT



COLLECTOR TO EMITTER VOLTAGE VERSUS BASE CURRENT

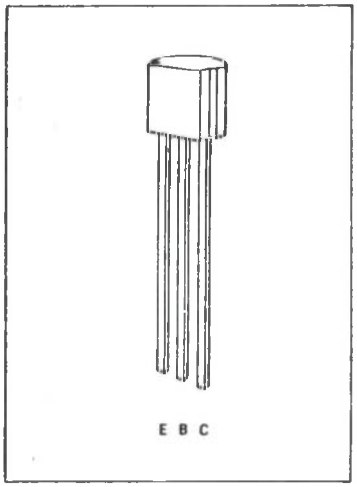


2N3905 • 2N3906

PNP GENERAL PURPOSE AMPLIFIERS AND SWITCHES

FAIRCHILD DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

- **MEDIUM VOLTAGE . . .** V_{CEO} = −40 V (MIN)
- **HIGH GAIN . . . .** h_{FE} = 100-300 AT 10 mA
- **LOW NOISE . . . .** NF = 4.0 dB (MAX) WIDEBAND
- **COMPLEMENTARY TO 2N3903 • 2N3904**



ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures	
†Storage Temperature	−55°C to +135°C
†Operating Junction Temperature	+135°C
†Lead Temperature (Soldering, 60 seconds time limit)	+230°C
Maximum Power Dissipation (Notes 2 and 3)	
†Total Dissipation at 25°C Ambient Temperature	0.31 Watt
at 60°C Ambient Temperature	0.21 Watt
Maximum Voltages and Current	
†V_{CBO} Collector to Base Voltage	−40 Volts
†V_{CEO} Collector to Emitter Voltage (Note 4)	−40 Volts
†V_{EBO} Emitter to Base Voltage	−5.0 Volts
†I_C Collector Current	200 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N3905 MIN.	2N3905 MAX.	2N3906 MIN.	2N3906 MAX.	UNITS	TEST CONDITIONS	
†h_{FE}	DC Pulse Current Gain (Note 5)	30		60			I_C = 0.1 mA,	V_{CE} = −1.0 V
†h_{FE}	DC Pulse Current Gain (Note 5)	40		80			I_C = 1.0 mA,	V_{CE} = −1.0 V
†h_{FE}	DC Pulse Current Gain (Note 5)	50	150	100	300		I_C = 10 mA,	V_{CE} = −1.0 V
†h_{FE}	DC Pulse Current Gain (Note 5)	30		60			I_C = 50 mA,	V_{CE} = −1.0 V
†h_{FE}	DC Pulse Current Gain (Note 5)	15		30			I_C = 100 mA,	V_{CE} = −1.0 V
†$V_{CE(sat)}$	Collector Saturation Voltage (Note 5)		−0.25		−0.25	Volts	I_C = 10 mA,	I_B = 1.0 mA
†$V_{CE(sat)}$	Collector Saturation Voltage (Note 5)		−0.4		−0.4	Volts	I_C = 50 mA,	I_B = 5.0 mA
†$V_{BE(sat)}$	Base Saturation Voltage (Note 5)	−0.65	−0.85	−0.65	−0.85	Volts	I_C = 10 mA,	I_B = 1.0 mA
†$V_{BE(sat)}$	Base Saturation Voltage (Note 5)		−0.95		−0.95	Volts	I_C = 50 mA,	I_B = 5.0 mA
†I_{CEX}	Collector Cutoff Current		50		50	nA	V_{CE} = −30V ,	V_{BE} = 3.0 V
†I_{BL}	Base Cutoff Current		50		50	nA	V_{CE} = −30V ,	V_{BE} = 3.0 V
†BV_{CBO}	Collector to Base Breakdown Voltage	−40		−40		Volts	I_C = 10 μA,	I_E = 0
†BV_{CEO}	Collector to Emitter Breakdown Voltage (Note 5)	−40		−40		Volts	I_C = 1.0 mA	I_B = 0
†BV_{EBO}	Base to Emitter Breakdown Voltage	−5.0		−5.0		Volts	I_C = 0,	I_E = 10 μA
†C_{obo}	Output Capacitance (f = 100 kHz)		4.5		4.5	pF	I_E = 0,	V_{CB} = −5.0 V
†C_{Ibo}	Input Capacitance (f = 100 kHz)		10		10	pF	I_C = 0,	V_{EB} = −0.5 V
†h_{fe}	High Frequency Current Gain (f = 100 MHz)	2.0		2.5			I_C = 1.0mA	V_{CE} = −20 V
†f_T	Current Gain Bandwidth Product (f = 100 MHz)	200		250		MHz	I_C = 10 mA,	V_{CE} = −20 V
†t_d	Delay Time (See Figure 1)		35		35	ns	$I_C \approx$ 10 mA,	$I_{B1} \approx$ 1.0 mA
†t_r	Rise Time (See Figure 1)		35		35	ns	$I_C \approx$ 10 mA,	$I_{B1} \approx$ 1.0 mA
†t_s	Storage Time (See Figure 2)		200		225	ns	$I_C \approx$ 10 mA, $I_{B2} \approx$ −1.0 mA	$I_{B1} \approx$ 1.0 mA
†t_f	Fall Time (See Figure 2)		60		75	ns	$I_C \approx$ 10 mA, $I_{B2} \approx$ −1.0 mA	$I_{B1} \approx$ 1.0 mA
†h_{Ie}	Input Impedance (f = 1.0 kHz)	0.5	8.0	2.0	12	kΩ	I_C = 1.0 mA,	V_{CE} = −10 V
†h_{re}	Voltage Feedback Ratio (f=1.0 kHz)	0.1	5.0	1.0	10	X10^{-4}	I_C = 1.0 mA,	V_{CE} = −10 V
†h_{fe}	Small Signal Current Gain (f=1.0 kHz)	50	200	100	400		I_C = 1.0 mA,	V_{CE} = −10 V
†h_{oe}	Output Admittance (f = 1.0 kHz)	1.0	40	3.0	60	μmho	I_C = 1.0 mA,	V_{CE} = −10 V
†NF	Noise Figure (f=10 Hz to 15.7 kHz)		5.0		4.0	dB	I_C = 100 μA, R_s = 1.0 kΩ	V_{CE} = −5.0 V

†JEDEC Registered Values

*Planar is a patented Fairchild process.

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 135°C and junction to ambient thermal resistance of 357°C/Watt (derating factor of 2.81 mW/ °C).

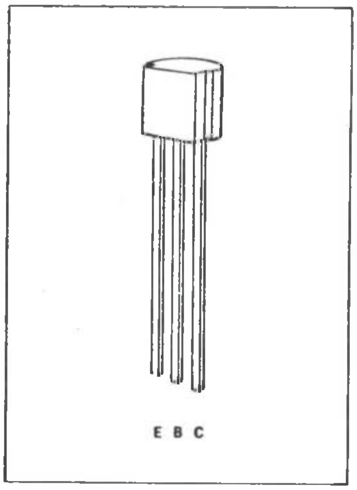
(4) Rating refers to a high current point where collector to emitter voltage is lowest.

(5) Pulse conditions: length = 300 μs; duty cycle = 2%.

NPN GENERAL PURPOSE AMPLIFIERS AND SWITCHES

FAIRCHILD DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

- MEDIUM VOLTAGE . . . V_{CEO} = 40 V (MIN)
- HIGH GAIN . . . . h_{FE} = 100-300 AT 10 mA
- LOW NOISE . . . . NF = 5.0 dB (MAX) WIDEBAND
- COMPLEMENTARY TO 2N3905 • 2N3906



ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures	
†Storage Temperature	-55°C to +135°C
†Operating Junction Temperature	+135°C
†Lead Temperature (Soldering, 60 secons time limit)	+230°C
Maximum Power Dissipation (Notes 2 and 3)	
†Total Dissipation at 25°C Ambient Temperature	0.31 Watt
at 60°C Ambient Temperature	0.21 Watt
Maximum Voltages and Current	
†V_{CBO} Collector to Base Voltage	60 Volts
†V_{CEO} Collector to Emitter Voltage (Note 4)	40 Volts
†V_{EBO} Emitter to Base Voltage	6.0 Volts
†I_C Collector Current	200 mA

ELECTRICAL CHARACTERISTICS (25° Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N3903 MIN.	2N3903 MAX.	2N3904 MIN.	2N3904 MAX.	UNITS	TEST CONDITIONS	
†h_{FE}	DC Pulse Current Gain (Note 5)	20		40			I_C = 0.1 mA,	V_{CE} = 1.0 V
†h_{FE}	DC Pulse Current Gain (Note 5)	35		70			I_C = 1.0 mA,	V_{CE} = 1.0 V
†h_{FE}	DC Pulse Current Gain (Note 5)	50	150	100	300		I_C = 10 mA,	V_{CE} 1.0 V
†h_{FE}	DC Pulse Current Gain (Note 5)	30		60			I_C = 50 mA,	V_{CE} = 1.0 V
†h_{FE}	DC Pulse Current Gain (Note 5)	15		30			I_C = 100 mA,	V_{CE} = 1.0 V
†$V_{CE(sat)}$	Collector Saturation Voltage (Note 5)		0.2		0.2	Volts	I_C = 10 mA,	I_B = 1.0 mA
†$V_{CE(sat)}$	Collector Saturation Voltage (Note 5)		0.3		0.3	Volts	I_C = 50 mA,	I_B = 5.0 mA
†$V_{BE(sat)}$	Base Saturation Voltage (Note 5)	0.65	0.85	0.65	0.85	Volts	I_C = 10 mA,	I_B = 1.0 mA
†$V_{BE(sat)}$	Base Saturation Voltage (Note 5)		0.95		0.95	Volts	I_C = 50 mA,	I_B = 5.0 mA
†I_{CEX}	Collector Cutoff Current		50		50	nA	V_{CE} = 30 V,	V_{BE} = -3.0 V
†I_{BL}	Base Cutoff Current		50		50	nA	V_{CE} = 30 V,	V_{BE} = -3.0 V
†BV_{CBO}	Collector to Base Breakdown Voltage	60		60		Volts	I_C = 10 μA,	I_E = 0
†BV_{CEO}	Collector to Emitter Breakdown Voltage (Note 5)	40		40		Volts	I_C = 1.0 mA	I_B = 0
†BV_{EBO}	Base to Emitter Breakdown Voltage	6.0		6.0		Volts	I_C = 0,	I_E = 10 μA
†C_{obo}	Output Capacitance (f = 100 kHz)		4.0		4.0	pF	I_E = 0,	V_{CB} = 5.0 V
†C_{ibo}	Input Capacitance (f = 100 kHz)		8.0		8.0	pF	I_C = 0,	V_{EB} = 0.5 V
†h_{fe}	High Frequency Current Gain (f = 100 MHz)	2.5		3.0*			I_C = 10 mA,	V_{CE} = 20 V
†f_T	Current Gain Bandwidth Product (f = 100 MHz)	250		300		MHz	I_C = 10 mA,	V_{CE} = 20 V
†t_d	Delay time (See Figure 1)		35		35	ns	$I_C \approx$ 10 mA,	$I_{B1} \approx$ 1.0 mA
†t_r	Rise Time (See Figure 1)		35		35	ns	$I_C \approx$ 10 mA,	$I_{B1} \approx$ 1.0 mA
†t_s	Storage Time (See Figure 2)		175		200	ns	$I_C \approx$ 10 mA, $I_{B2} \approx$ 1.0 mA	$I_{B1} \approx$ 1.0 mA
†t_f	Fall Time (See Figure 2)		50		50	ns	$I_C \approx$ 10 mA, $I_{B2} \approx$ -1.0 mA	$I_{B1} \approx$ 1.0 mA
†h_{ie}	Input Impedance (f = 1.0 kHz)	0.5	8.0	1.0	10	kΩ	I_C = 1.0 mA,	V_{CE} = 10 V
†h_{re}	Voltage Feedback Ration (f = 1.0 kHz)	0.1	5.0	0.5	8.0	X10^{-4}	I_C = 1.0 mA,	V_{CE} = 10 V
†h_{fe}	Small Signal Current Gain f = 1.0 kHz)	50	200	100	400		I_C = 1.0 mA,	V_{CE} = 10 V
†h_{oe}	Output Admittance (f = 1.0 kHz)	1.0	40	1.0	40	μmho	I_C = 1.0 mA,	V_{CE} = 10 V
†NF	Noise Figure (f = 10 Hz to 15.7 kHz)		6.0		5.0	dB	I_C = 100 μA, R_s = 1.0 kΩ	V_{CE} = 5.0 V

†JEDEC Registered Values

*Planar is a patented Fairchild process.

These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

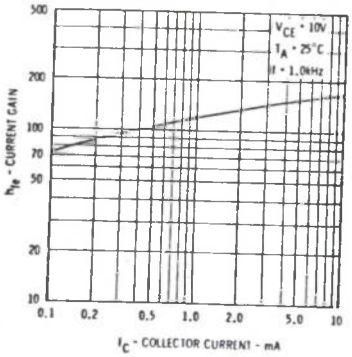
(3) These ratings give a maximum junction temperature of 135°C and junction to ambient thermal resistance of 357°C/Watt (derating factor of 2.81 mW/°C).

(4) Rating refers to a high current point where collector to emitter voltage is lowest.

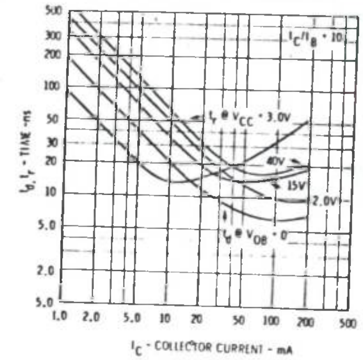
(5) Pulse conditions length = 300 μs; duty cycle = 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

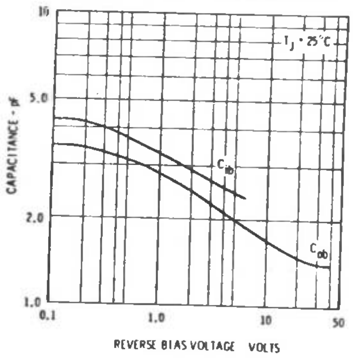
SMALL SIGNAL CURRENT GAIN VERSUS COLLECTOR CURRENT



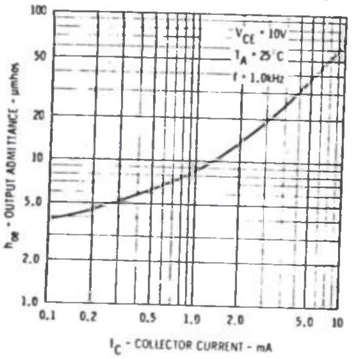
TURN ON TIME VERSUS COLLECTOR CURRENT



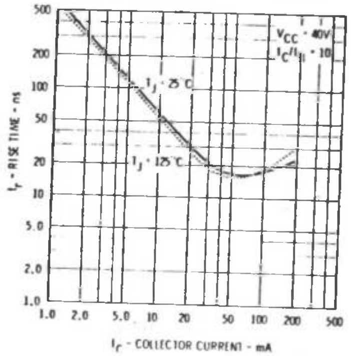
CAPACITANCE VERSUS REVERSE BIAS VOLTAGE



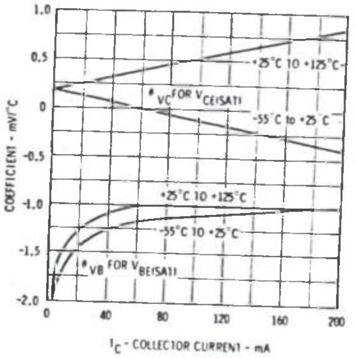
OUTPUT ADMITTANCE VERSUS COLLECTOR CURRENT



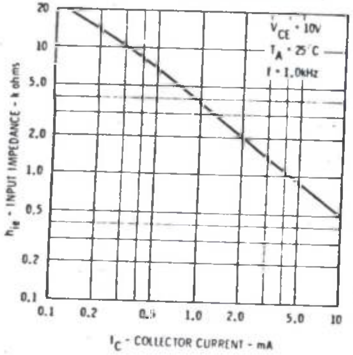
RISE TIME VERSUS COLLECTOR CURRENT



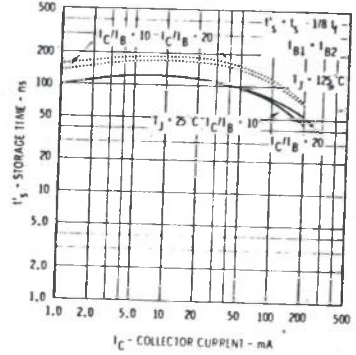
TEMPERATURE COEFFICIENTS VERSUS COLLECTOR CURRENT



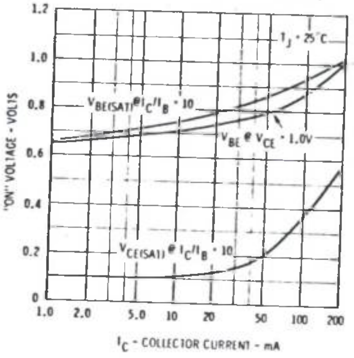
INPUT IMPEDANCE VERSUS COLLECTOR CURRENT



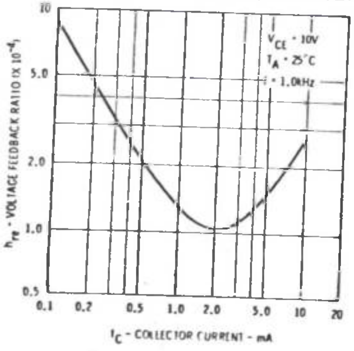
STORAGE TIME VERSUS COLLECTOR CURRENT



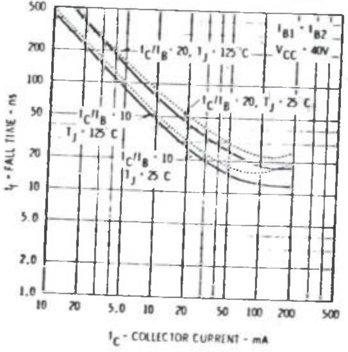
"ON" VOLTAGE VERSUS COLLECTOR CURRENT



VOLTAGE FEEDBACK RATIO VERSUS COLLECTOR CURRENT



FALL TIME VERSUS COLLECTOR CURRENT



CHARGE DATA VERSUS COLLECTOR CURRENT

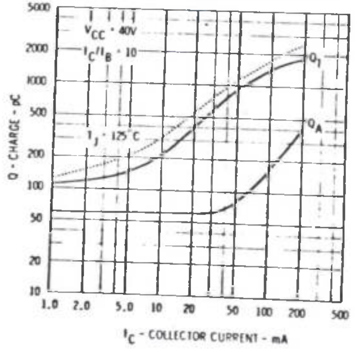


FIGURE 1—DELAY AND RISE TIME EQUIVALENT TEST CIRCUIT

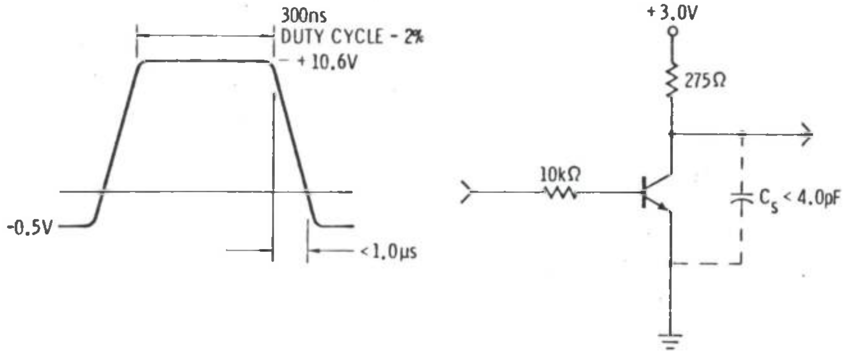
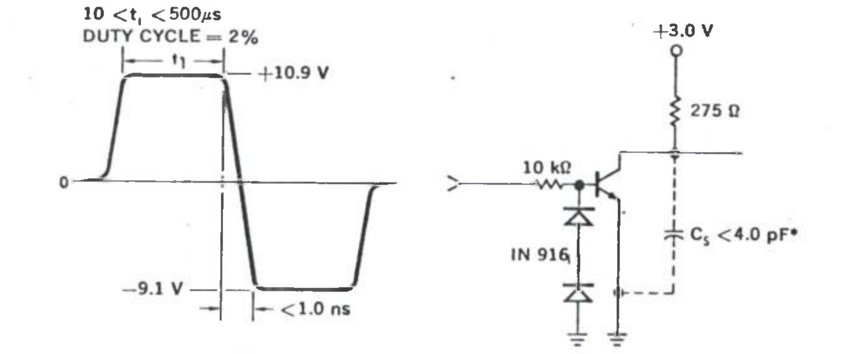


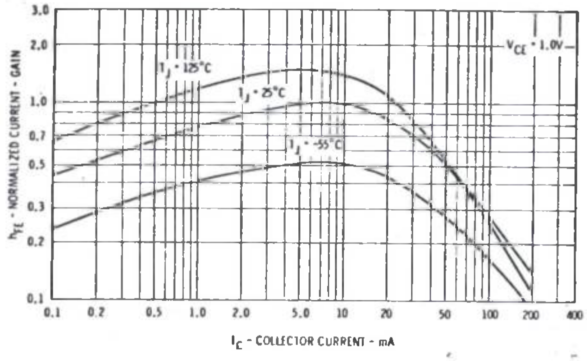
FIGURE 2—STORAGE AND FALL TIME EQUIVALENT TEST CIRCUIT



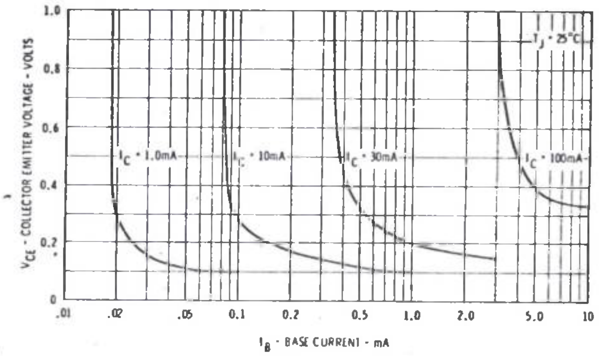
*Total shunt capacitance of test jig and connectors

TYPICAL ELECTRICAL CHARACTERISTICS

NORMALIZED DC CURRENT GAIN VERSUS COLLECTOR CURRENT

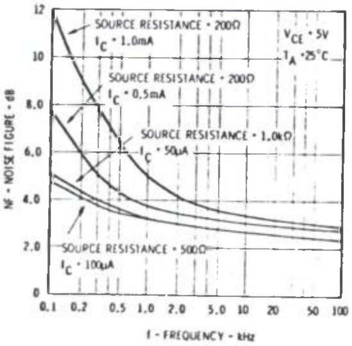


COLLECTOR TO EMITTER VOLTAGE VERSUS BASE CURRENT



NOISE FIGURE VARIATIONS V_{CE} = 5.0 V, T_A = 25°C

NOISE FIGURE VERSUS FREQUENCY



NOISE FIGURE VERSUS SOURCE RESISTANCE

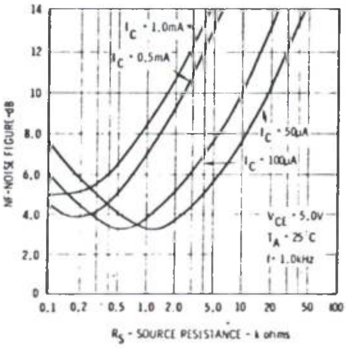


FIGURE 6 — SMALL-SIGNAL CURRENT GAIN versus FREQUENCY

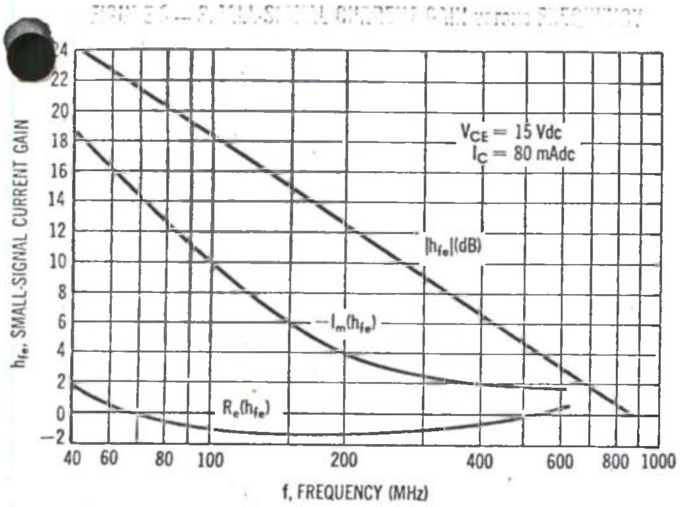


FIGURE 7 — OUTPUT CAPACITANCE versus COLLECTOR VOLTAGE

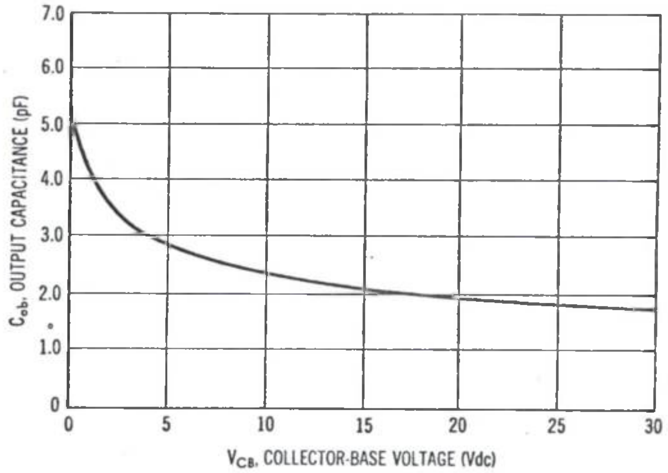


FIGURE 8 — f_T versus COLLECTOR CURRENT

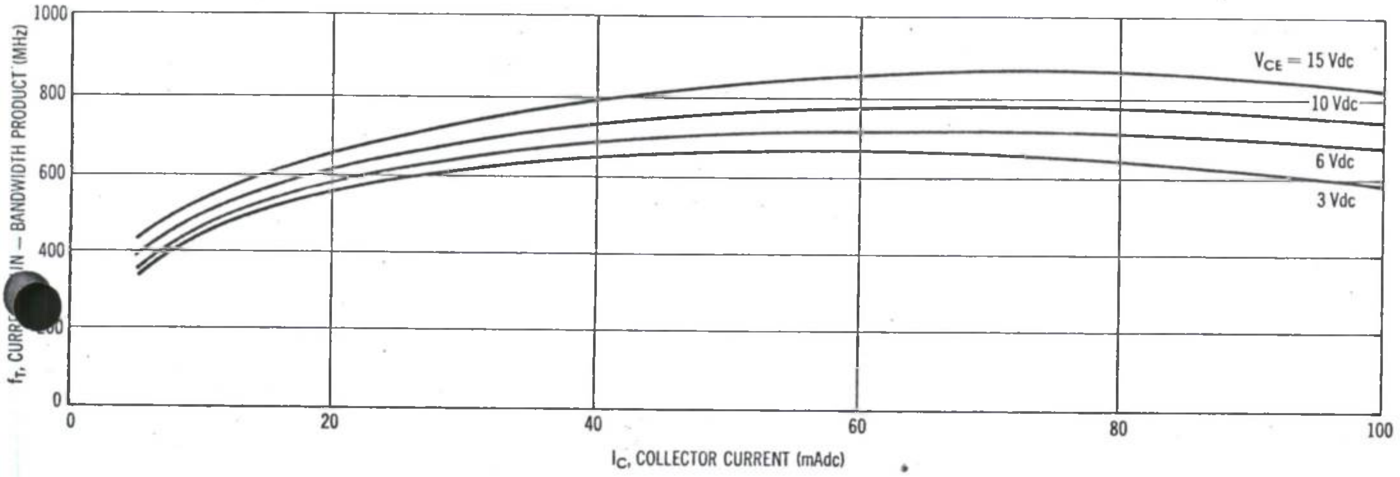


FIGURE 9 — $r_b'C_c$ versus COLLECTOR CURRENT

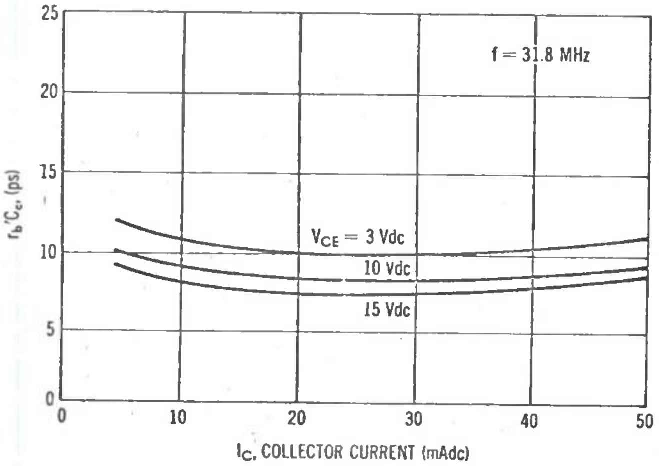
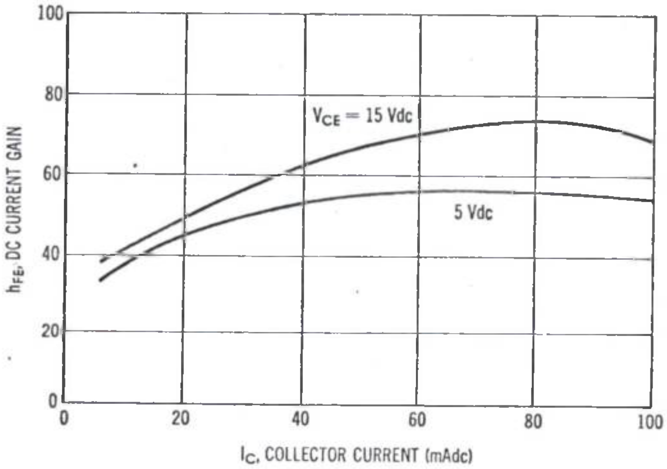


FIGURE 10 — DC CURRENT GAIN versus COLLECTOR CURRENT



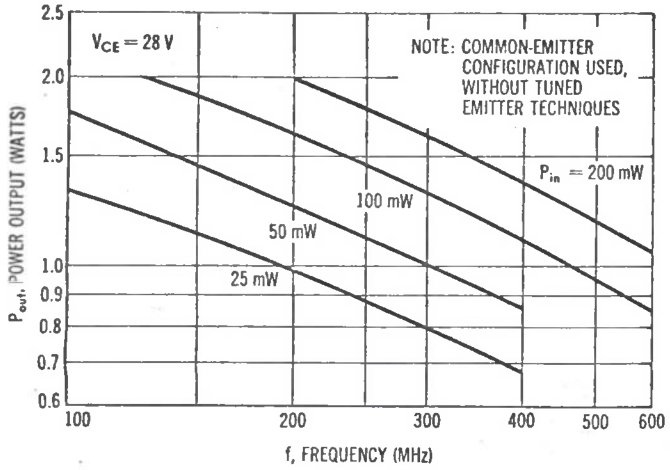


FIGURE 2 — POWER OUTPUT versus FREQUENCY (Class C)

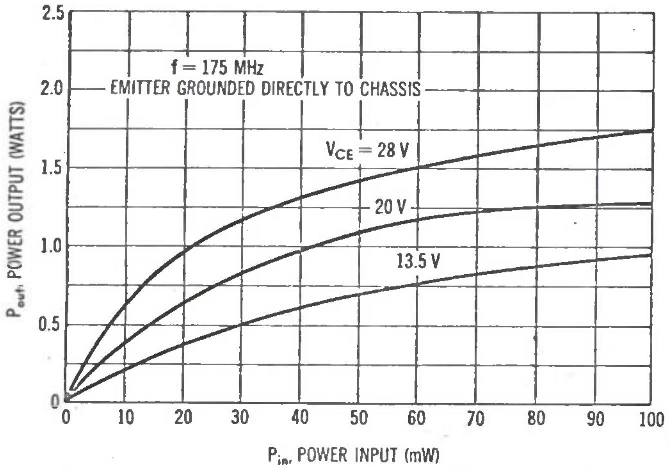


FIGURE 3 — POWER OUTPUT versus POWER INPUT (Class C)

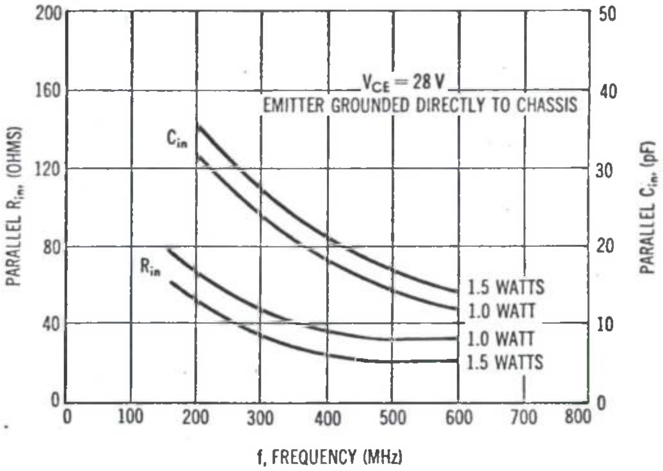


FIGURE 4 — PARALLEL INPUT RESISTANCE AND CAPACITANCE versus FREQUENCY (Class C)

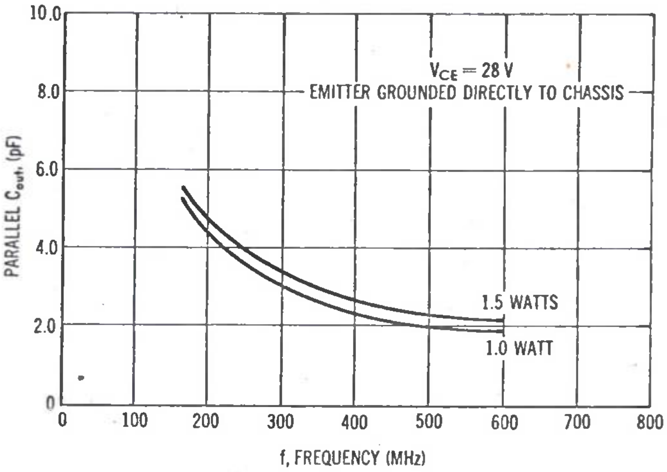


FIGURE 5 — PARALLEL OUTPUT CAPACITANCE versus FREQUENCY (Class C)

DESIGN NOTE

Figures 11 through 18 show small-signal admittance-parameter data. This data can be used for Class A amplifier designs.

For Class C power-amplifier designs, the small-signal parameters are not applicable. Figures 4 and 5 give parallel output capacitance and the parallel input resistance and capacitance for Class C power-amplifier operation.

The parallel resistive portion of the collector load impedance for a power amplifier, R_L', may be computed by assuming a peak voltage swing equal to V_{CC}, and using the expression

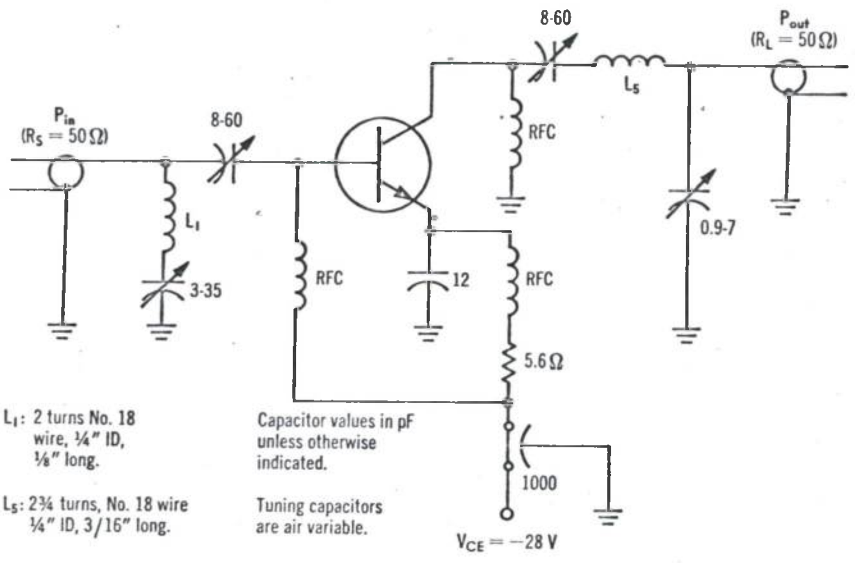
$$R_L' = \frac{V_{CC}^2}{2P}$$

where P = RF power output. The computed R_L' may then be combined with the data in Figures 2 and 3 to comprise complete device impedance data for Class C power amplifier design.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 5 mAdc, I_B = 0)	$BV_{CEO(sus)}$	30	—	—	Vdc
Collector-Base Breakdown Voltage (I_E = 0, I_C = 0.1 mAdc)	BV_{CBO}	55	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	BV_{EBO}	3.5	—	—	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, I_B = 0)	I_{CEO}	—	—	20	μA
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.36 Adc, V_{CE} = 5 Vdc) (I_C = 0.05 Adc, V_{CE} = 5 Vdc)	h_{FE}	 5 10	 — —	 — 200	—
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 25 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	f_T	—	800	—	MHz
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	2.0	3.0	pF
FUNCTIONAL TEST					
Power Gain Test Circuit-Figure 1 P_{in} = 0.1 W, V_{CE} = 28 Vdc f = 400 MHz	G_{pe}	10	—	—	dB
Power Output	P_{out}	1.0	—	—	Watts
Collector Efficiency	η	45	—	—	%

FIGURE 1 — 400 MHz RF AMPLIFIER CIRCUIT FOR POWER-OUTPUT TEST



L_1: 2 turns No. 18 wire, ¼″ ID, ⅛″ long.

L_S: 2¾ turns, No. 18 wire ¼″ ID, 3/16″ long.

Capacitor values in pF unless otherwise indicated.

Tuning capacitors are air variable.

MOTOROLA
Semiconductors
BOX 955 • PHOENIX, ARIZONA 85001

THE LINE

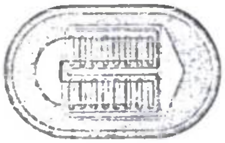
2N3866

NPN SILICON AMPLIFIER TRANSISTOR

MARCH 1966 — DS 5145

2N3866
DS 5145

NPN SILICON HIGH-FREQUENCY TRANSISTOR

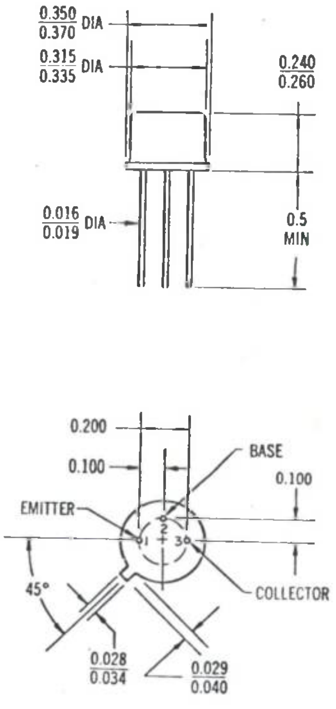


. . . designed for amplifier, frequency-multiplier, or oscillator applications in military and industrial equipment. Suitable for use as output, driver, or pre-driver stages in VHF and UHF equipment.

- G_{pe} = 10 dB Minimum at 400 MHz
- 1 Watt Minimum Power Output at 400 MHz
- Multiple-Emitter Construction for Excellent High-Frequency Performance

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	55	Vdc
Emitter-Base Voltage	V_{EB}	3.5	Vdc
Collector Current	I_C	0.4	Amp
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	5 28.6	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C



TO-39 PACKAGE

ACTIVE REGION DC SAFE OPERATING AREA

FIGURE 1 – 2N3771, 2N3772

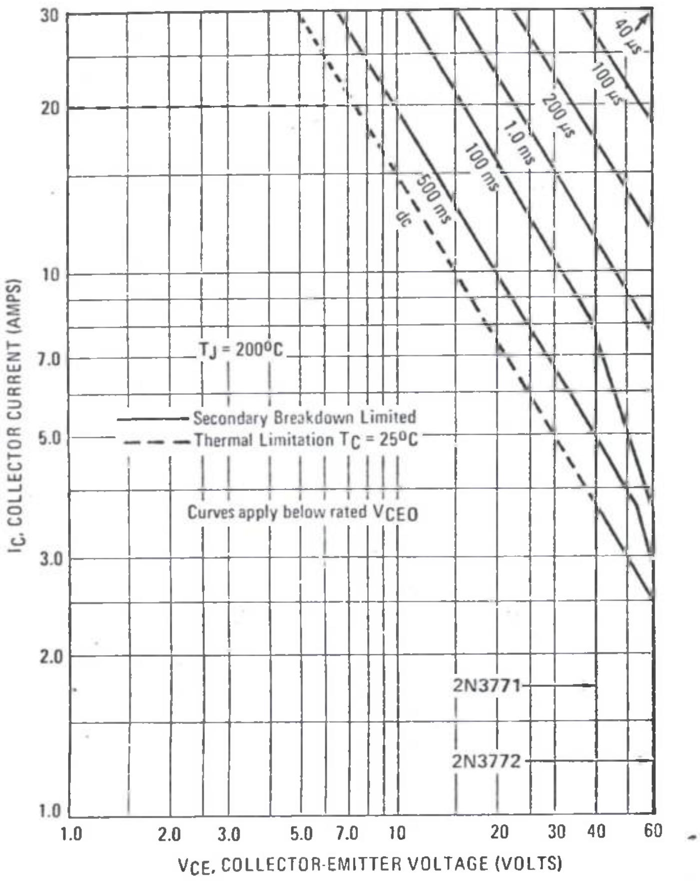
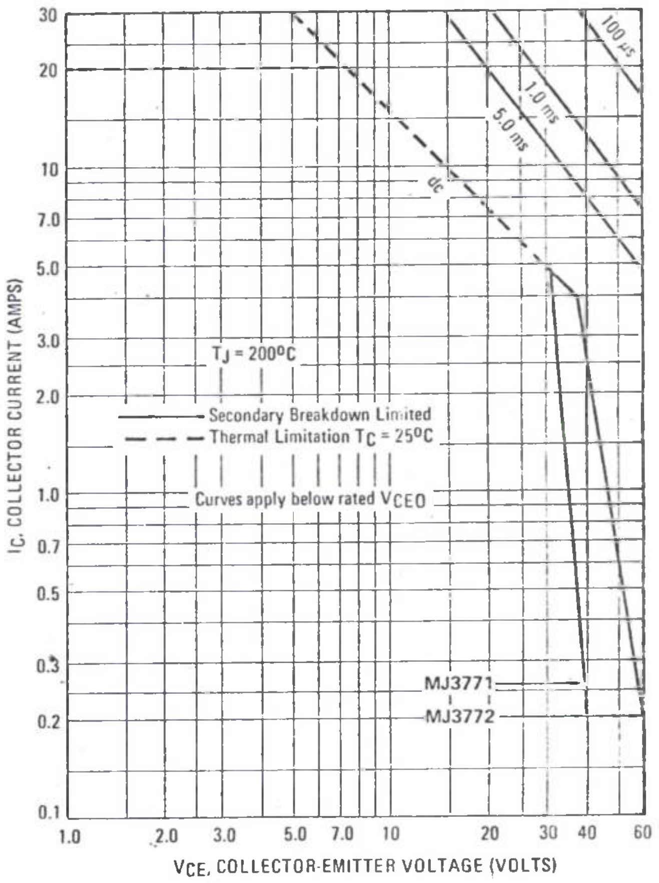


FIGURE 2 – MJ3771, MJ3772



The Safe Operating Area Curves indicate I_C-V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
*Collector-Emitter Sustaining Voltage (Note 1)		$V_{CEO(sus)}$				Vdc
(I_C = 200 mAdc, I_B = 0)	2N3771, MJ3771		40	–	–	
	2N3772, MJ3772		60	–	–	
*Collector Cutoff Current		I_{CEO}				mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N3771, MJ3771		–	–	10	
(V_{CE} = 50 Vdc, I_B = 0)	2N3772, MJ3772		–	–	10	
*Collector Cutoff Current		I_{CEX}				mAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)	2N3771, MJ3771		–	–	2.0	
	2N3772, MJ3772		–	–	5.0	
(V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	All Types		–	–	10	
Collector Cutoff Current		I_{CBO}				mAdc
*(V_{CB} = Rated V_{CB}, I_E = 0)	2N3771, MJ3771		–	–	2.0	
	2N3772, MJ3772		–	–	5.0	
(V_{CB} = 30 Vdc, I_E = 0, T_C = 150°C)	All Types		–	–	10	
*Emitter Cutoff Current		I_{EBO}				mAdc
(V_{BE} = Rated V_{BE}, I_C = 0)			–	–	5.0	
ON CHARACTERISTICS						
*DC Current Gain (Note 1)		h_{FE}				–
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)	2N3771, MJ3771		15	–	60	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	2N3772, MJ3772		15	–	60	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N3771, MJ3771		5.0	–	–	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N3772, MJ3772		5.0	–	–	
*Collector-Emitter Saturation Voltage (Note 1)		$V_{CE(sat)}$				Vdc
(I_C = 15 Adc, I_B = 1.5 Adc)	2N3771		–	–	2.0	
	MJ3771		–	–	1.0	
(I_C = 10 Adc, I_B = 1.0 Adc)	2N3772		–	–	1.4	
	MJ3772		–	–	1.0	
(I_C = 30 Adc, I_B = 6.0 Adc)	2N3771, MJ3771		–	–	4.0	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N3772, MJ3772		–	–	4.0	
Base-Emitter Saturation Voltage (Note 1)		$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	MJ3771, MJ3772		–	–	1.7	
(I_C = 15 Adc, I_B = 1.5 Adc)	MJ3771, MJ3772		–	–	1.8	
(I_C = 20 Adc, I_B = 2.0 Adc)	MJ3771, MJ3772		–	–	2.5	
*Base-Emitter On Voltage (Note 1)		$V_{BE(on)}$				Vdc
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)	2N3771		–	–	2.7	
	MJ3771		–	–	1.7	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	2N3772		–	–	2.2	
	MJ3772		–	–	1.7	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product		f_T				MHz
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 50 kHz)	2N3771, 2N3772		0.2	–	–	
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	MJ3771, MJ3772		2.0	–	–	
Small Signal Current Gain (I_C = 10 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	40	–	–	–
SWITCHING CHARACTERISTICS						
Rise Time (V_{CC} = 10 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	MJ3771, MJ3772	t_r	–	350	–	ns
Storage Time	MJ3771, MJ3772	t_s	–	700	–	ns
Fall Time	MJ3771, MJ3772	t_f	–	300	–	ns

*Indicates JEDEC Registered Data (2N3771, 2N3772).

Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

MOTOROLA
Semiconductors
BOX 20912 . PHOENIX, ARIZONA 85036

2N3771 2N3772
MJ3771 MJ3772

HIGH-POWER NPN SILICON TRANSISTORS

. . . designed for use in power amplifier and switching circuits applications.

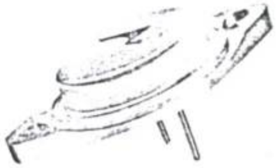
- High DC Current Gain —
  h_{FE} = 15 (Min) @ I_C = 15 Adc – 2N3771, MJ3771
  15 (Min) @ I_C = 10 Adc – 2N3772, MJ3772
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 15 Adc – MJ3771
  1.0 Vdc (Max) @ I_C = 10 Adc – MJ3772

20 AND 30 AMPERE
POWER TRANSISTORS

NPN SILICON

40-60 VOLTS
150 WATTS

MAY 1969 – DS 3129



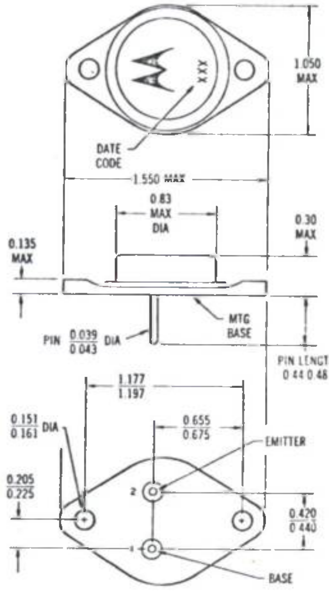
*MAXIMUM RATINGS

Rating	Symbol	2N3771 MJ3771	2N3772 MJ3772	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Collector-Emitter Voltage	V_{CEX}	50	80	Vdc
Collector-Base Voltage	V_{CB}	50	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0	7.0	Vdc
Collector Current – Continuous Peak	I_C	30 30	20 30	Adc
Base Current – Continuous	I_B	7.5	5.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	150 0.86		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^oC/W$

*Indicates JEDEC Registered Data (2N3771, 2N3772).



CASE 11
TO-3

SMALL SIGNAL y PARAMETERS

$T_A = 25°C$

FIGURE 7 — INPUT ADMITTANCE

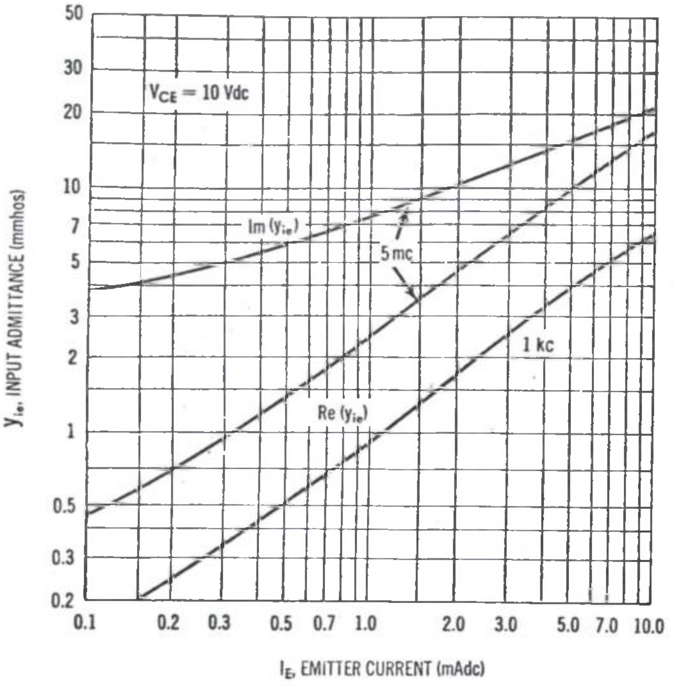


FIGURE 8 — REVERSE TRANSFER ADMITTANCE

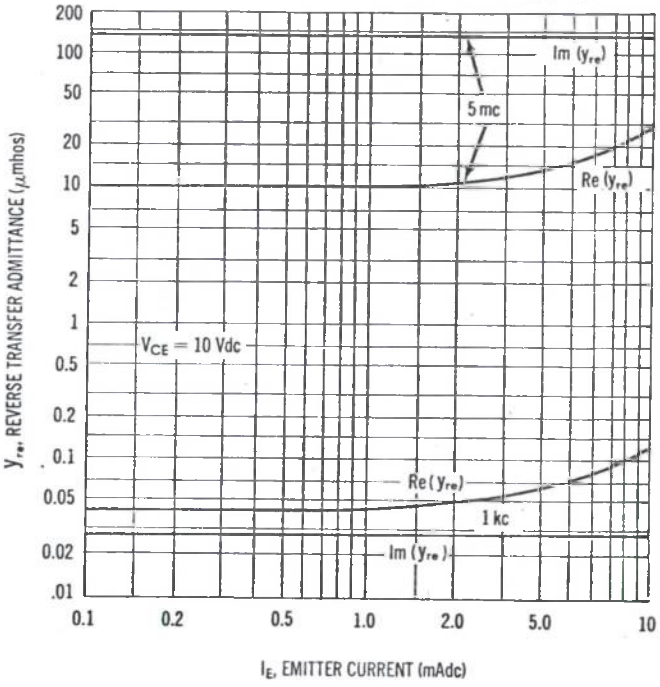


FIGURE 9 — FORWARD TRANSFER ADMITTANCE

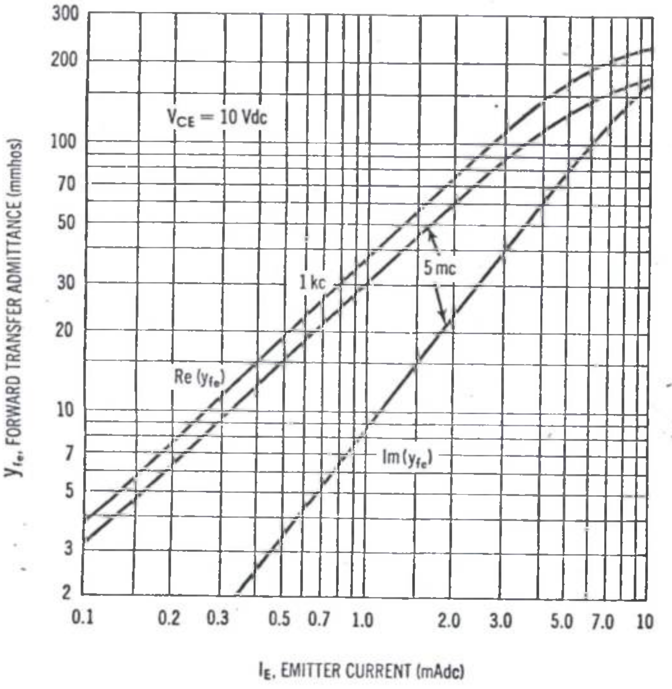


FIGURE 10 — OUTPUT ADMITTANCE

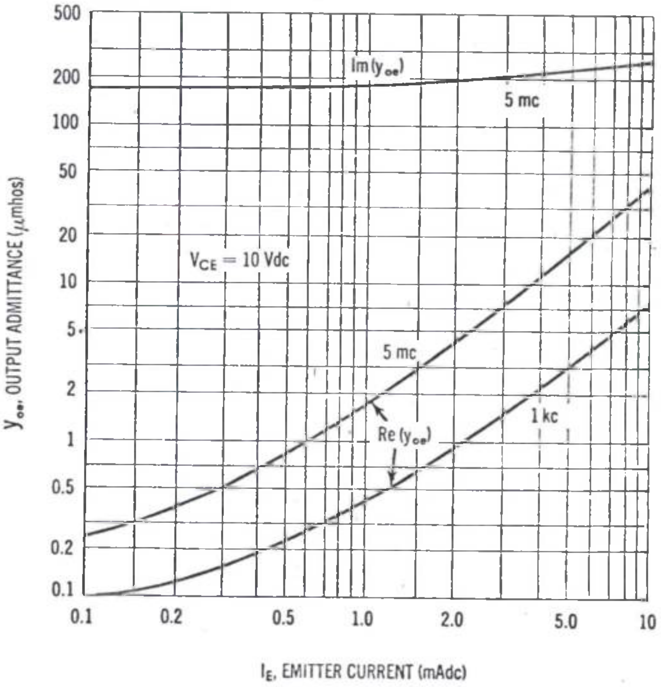


FIGURE 3 — DC CURRENT GAIN CHARACTERISTICS versus JUNCTION TEMPERATURE

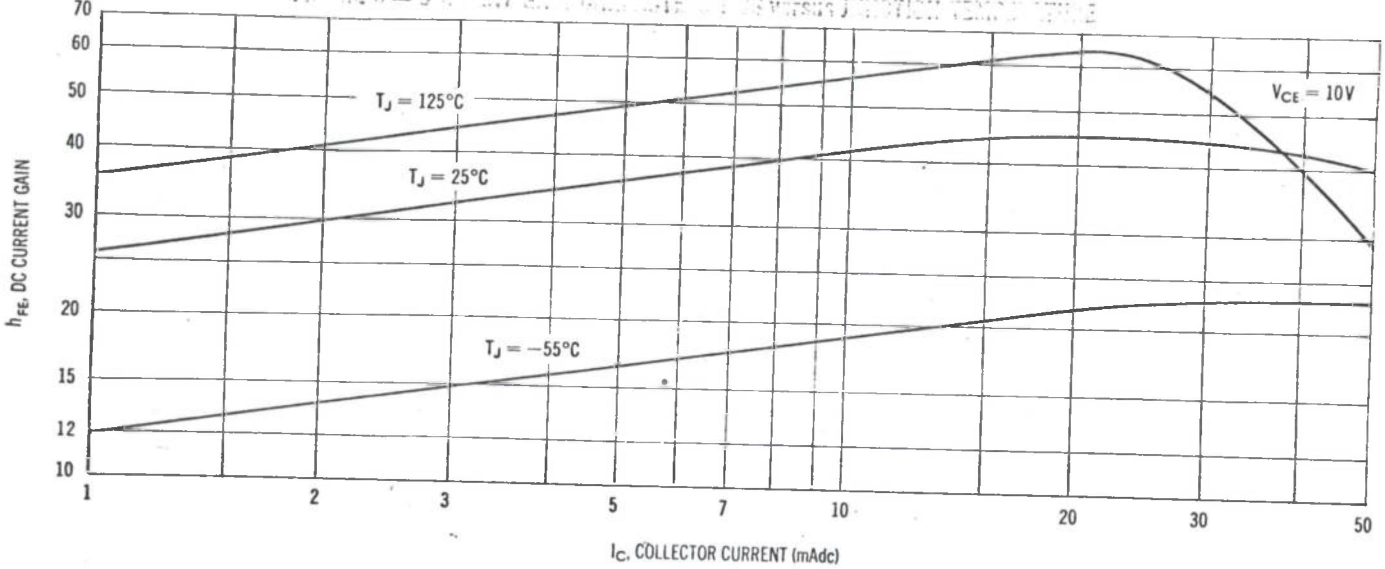


FIGURE 4 — CURRENT GAIN CHARACTERISTICS versus COLLECTOR-EMITTER VOLTAGE

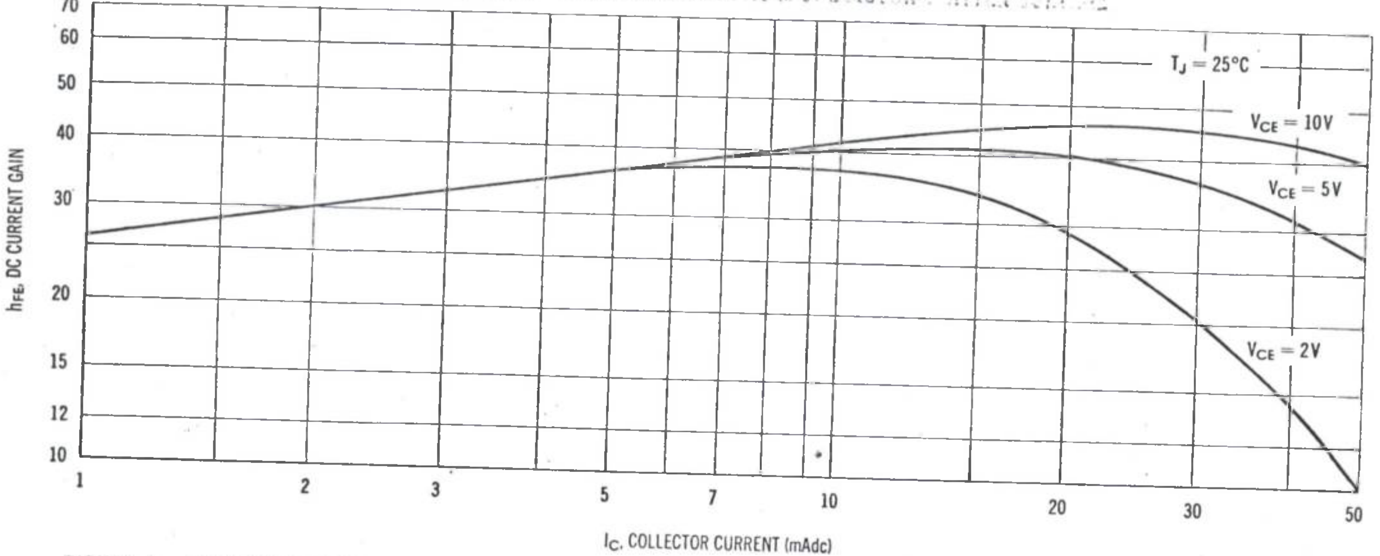


FIGURE 5 — COLLECTOR-EMITTER SATURATION VOLTAGE

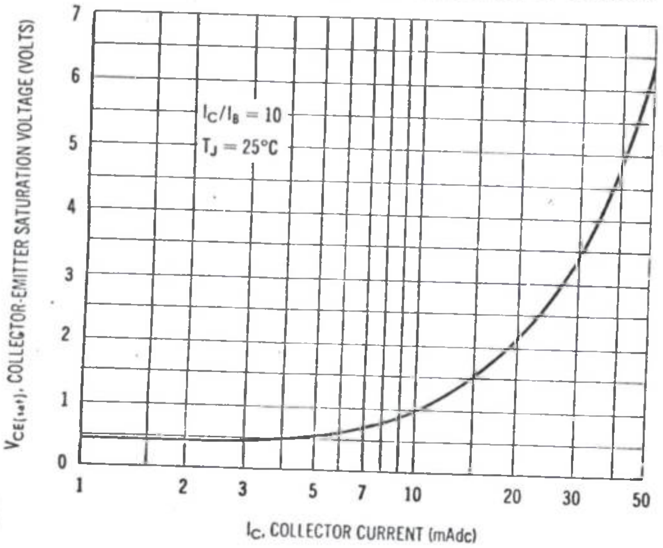
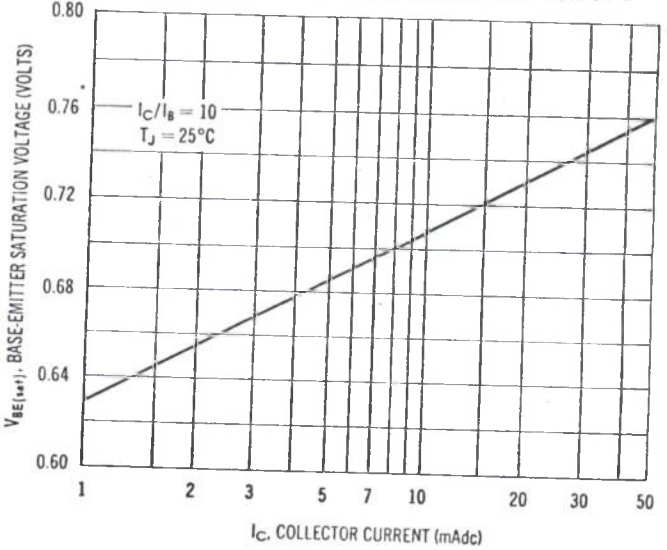


FIGURE 6 — BASE-EMITTER SATURATION VOLTAGE



ELECTRICAL CHARACTERISTIC (At 25°C ambient unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	300	—	Vdc
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc, I_B = 0)	BV_{CEO}*	300	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 100μAdc, I_C = 0)	BV_{EBO}	10	—	Vdc
Collector Saturation Voltage ** (I_C = 10 mAdc, I_B = 1 mAdc) (I_C = 30 mAdc, I_B = 3 mAdc)	$V_{CE(sat)}$**	— —	1 5	Vdc
Base-Emitter Saturation Voltage ** (I_C = 10 mAdc, I_B = 1 mAdc) (I_C = 30 mAdc, I_B = 3 mAdc)	$V_{BE(sat)}$**	— —	1.0 1.2	Vdc
DC Current Gain ** (I_C = 3 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 30 mAdc, V_{CE} = 10 Vdc) (I_C = 50 mAdc, V_{CE} = 20 Vdc)	h_{FE}**	10 15 20 20	— — 200 —	—
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0) (V_{CB} = 200 Vdc, I_E = 0, T_A = 100°C)	I_{CBO}	— —	0.2 20	μAdc
Emitter Cutoff Current V_{EB} = 6 Vdc, I_C = 0)	I_{EBO}	—	0.2	μAdc
Small Signal Current Gain (V_{CE} = 20 Vdc, I_C = 10 mAdc, f = 20 mc)	$\|h_{fe}\|$	1.5	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kc)	C_{ob}	—	6	pf
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kc)	C_{ib}	—	80	pf
Small Signal Current Gain (I_C = 10 mA, V_{CE} = 10 V, f = 1 kc)	h_{fe}	20	200	—
Voltage Feedback Ratio (I_C = 10 mA, V_{CE} = 10 V, f = 1 kc)	h_{re}	—	1.0	$X10^{-4}$
Input Impedance (I_C = 10 mA, V_{CE} = 10 V, f = 1 kc)	h_{ie}	—	0.5	Kohms
Output Admittance (I_C = 10 mA, V_{CE} = 10 V, f = 1 kc)	h_{oe}	5	50	mhos
Real Part of Input Impedance (I_C = 10 mA, V_{CE} = 10 V, f = 5 mc)	$Re(h_{ie})$	—	40	ohms

*PW $\leq$ 30 μsec, Duty Cycle $\leq$ 1%

**PW $\leq$ 300 μsec, Duty Cycle $\leq$ 2%

FIGURE 1 — JUNCTION CAPACITANCE

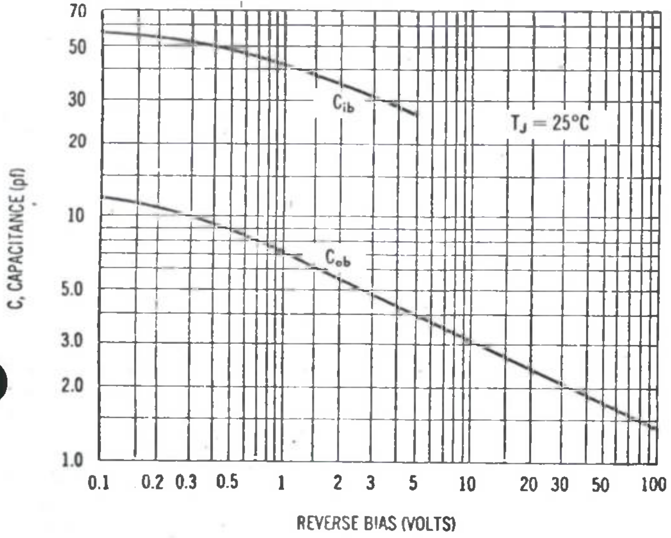
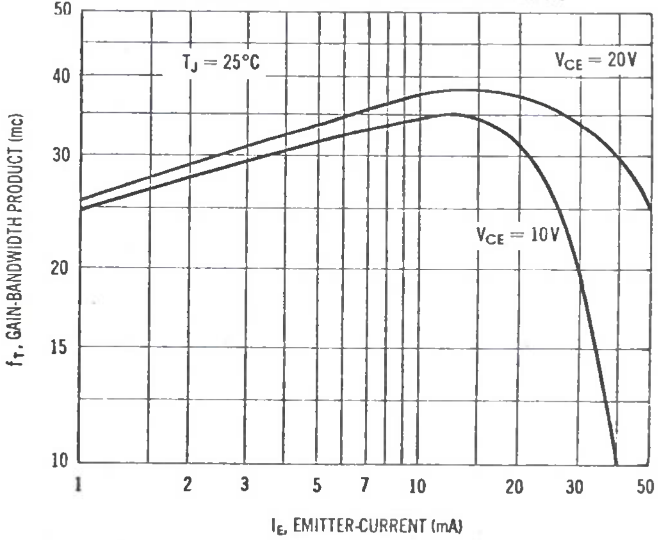


FIGURE 2 — GAIN-BANDWIDTH PRODUCT



MOTOROLA
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BOX 955 • PHOENIX, ARIZONA 85001

2N3742

NPN SILICON EPITAXIAL AMPLIFIER TRANSISTOR

MARCH 1965 — DS 5100

Si HIGH FREQUENCY TRANSISTOR
2N3742
DS 5100

HIGH-VOLTAGE NPN SILICON ANNULAR† TRANSISTOR

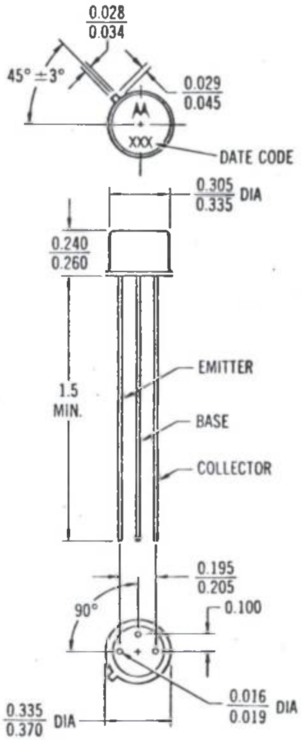
. . . designed for high-voltage DC to VHF amplifier applications.

TO-5
SOLID HEADER

- High Voltage Ratings
  BV_{CEO} = 300 Volts minimum
- Low Capacitance
  C_{ob} = 6 pf maximum
- Current-Gain Specified to 50 mAdc

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CB}	300	Vdc
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current	I_C	50	mAdc
Total Device Dissipation @ T_A = 25°C Derating Factor Above 25°C	P_D	1.0 5.71	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derating Factor Above 25°C	P_D	5 28.6	Watts mW/°C
Operating Junction Temperature	T_J	+200	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C



TO-5 OUTLINE

COLLECTOR CONNECTED TO CASE

The Motorola developed Annular process marks a breakthrough in low-leakage silicon transistor technology. Prior to this development, maximum voltage rating was limited by a phenomenon called "channeling," a surface-induced condition whose uncontrolled characteristics resulted in instability during operation. Channeling is traceable to the SiO_2 passivating layer necessary for low-leakage devices. By deliberately introducing a terminated channel whose predictable characteristics completely swamp out those of the randomly induced channel, the high-voltage capability of low-leakage transistors is greatly enhanced.

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† Manufactured by the Annular Process, Motorola patents applied for.

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FIGURE 7 — CURRENT GAIN

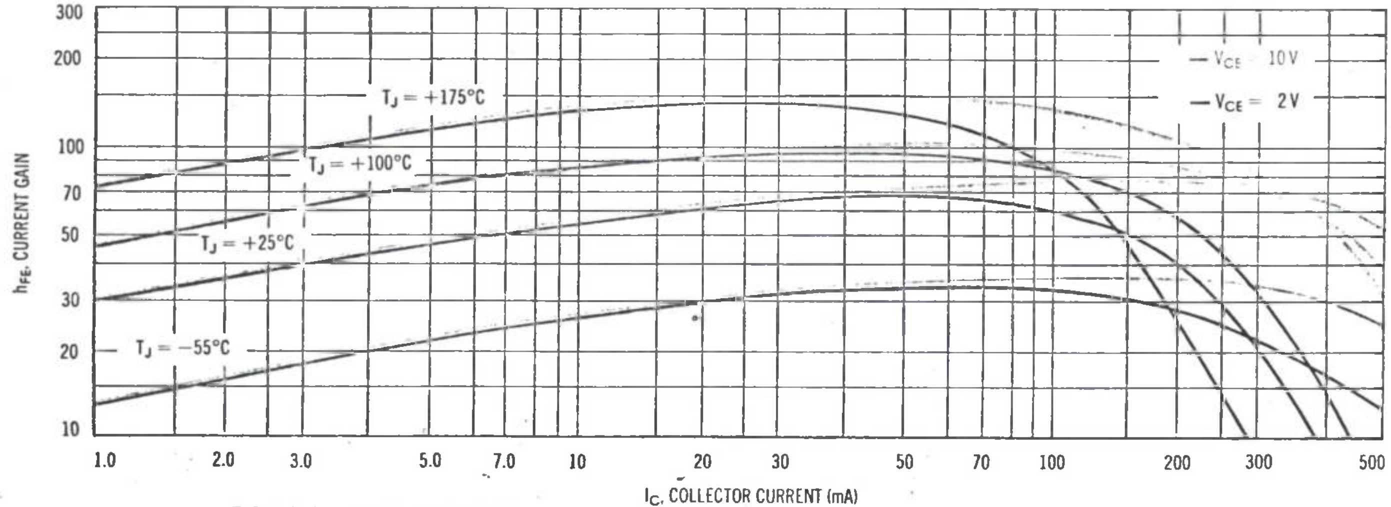


FIGURE 8 — "ON" VOLTAGES

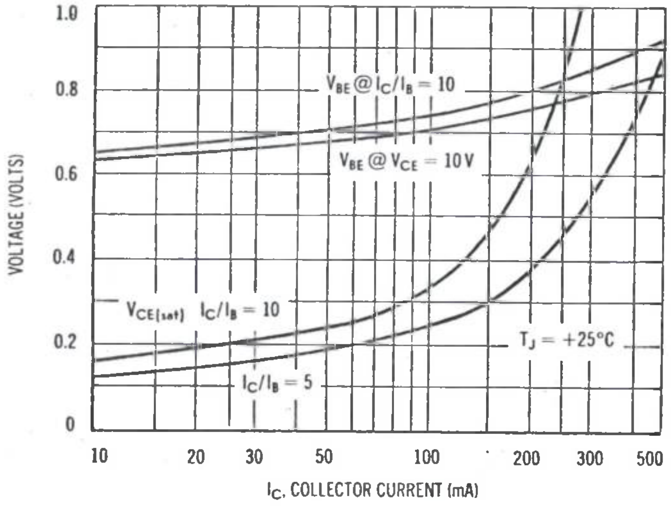


FIGURE 9 — CAPACITANCE

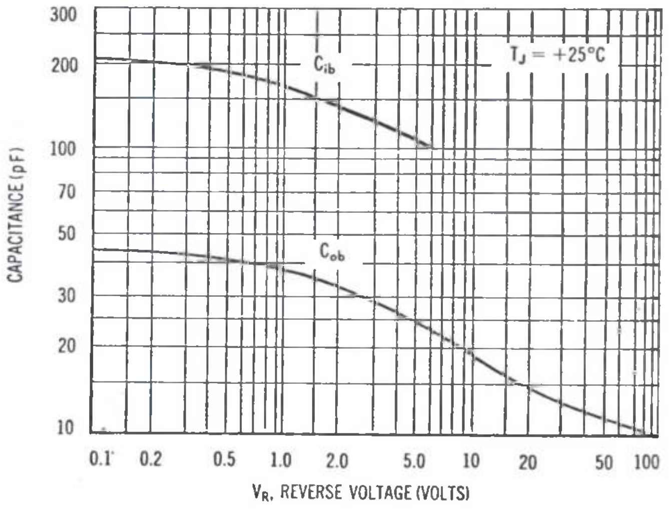


FIGURE 10 — TURN-ON TIME

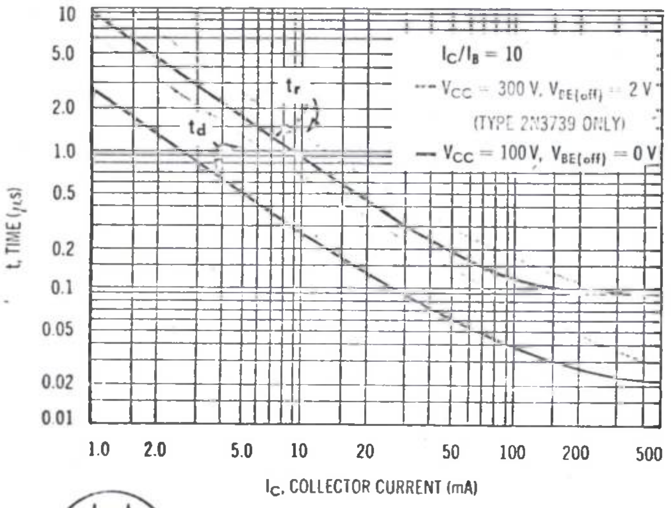
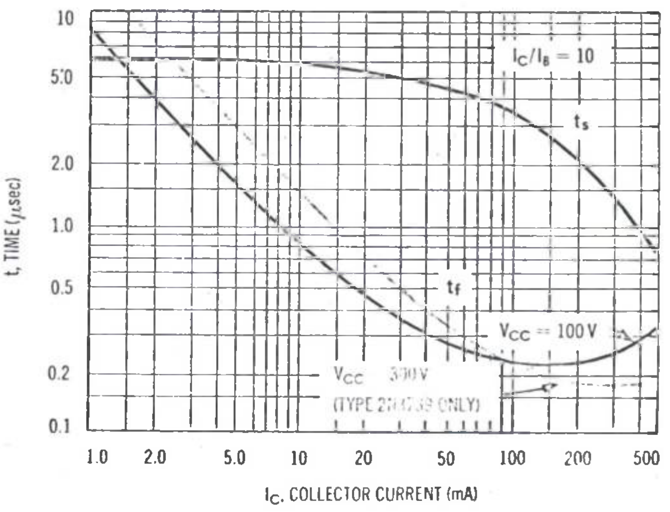


FIGURE 11 — TURN-OFF TIME



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BOX 955 • PHOENIX, ARIZONA 85001 • A SUBSIDIARY OF MOTOROLA INC.

927-1 PRINTED IN USA 8-68 IMPERIAL LITHO [illegible]

LARGE SIGNAL CHARACTERISTICS

FIGURE 3 — TRANSCONDUCTANCE

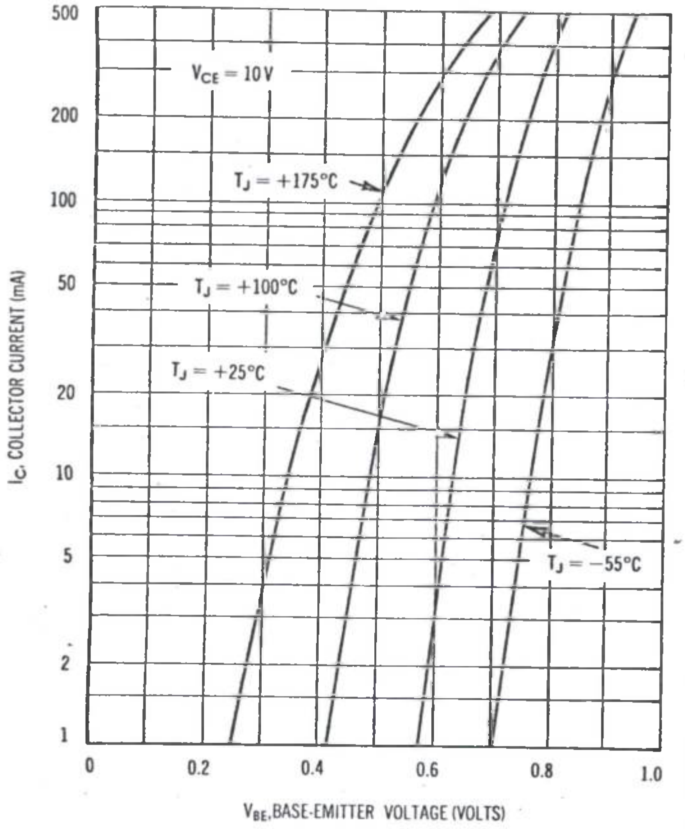
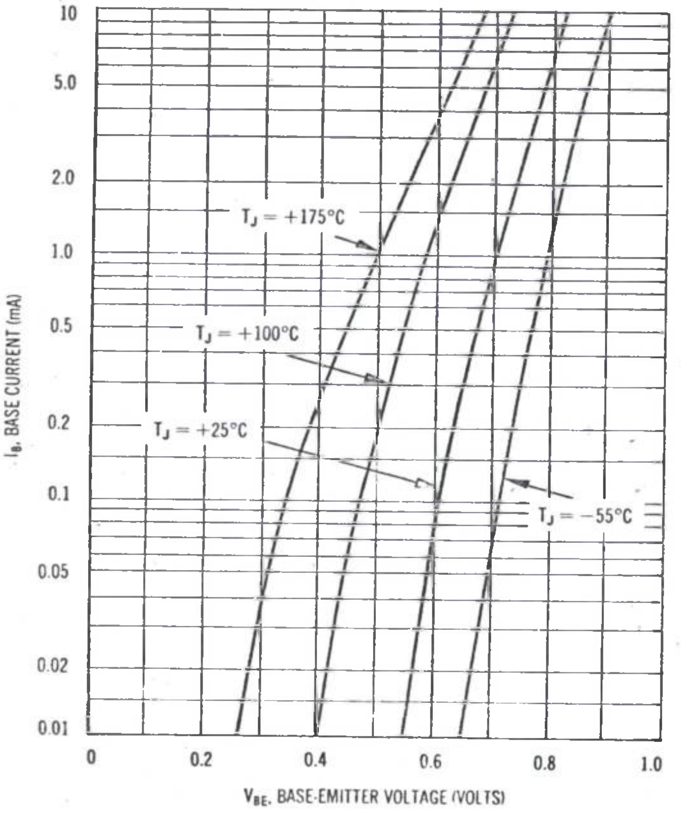


FIGURE 5 — INPUT ADMITTANCE



CUT-OFF CHARACTERISTICS

FIGURE 4 — TRANSCONDUCTANCE

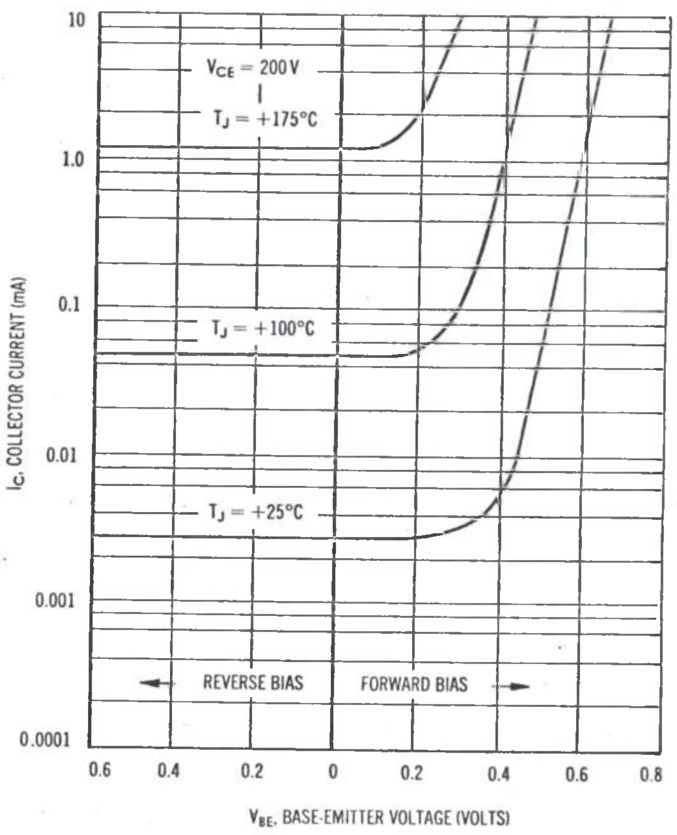
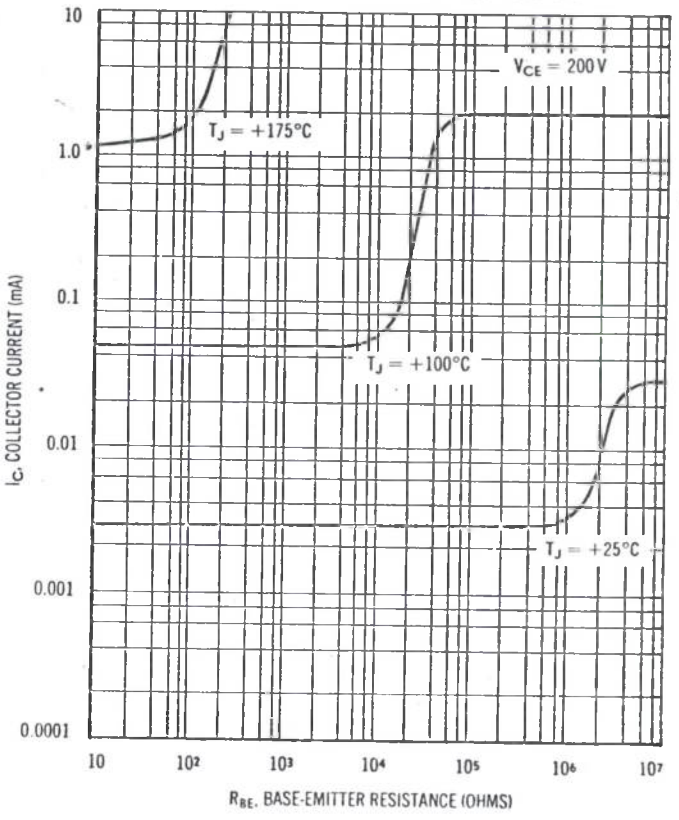


FIGURE 6 — EFFECT OF BASE-EMITTER RESISTANCE

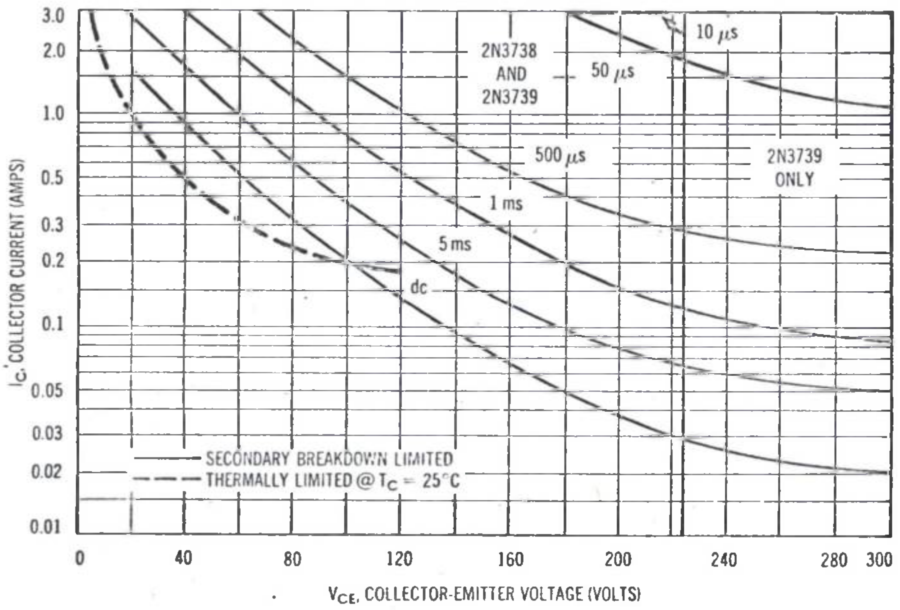


ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Figure No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage*						
(I_C = 5 mAdc, I_B = 0)	2N3738	-	$BV_{CEO(sus)}$*	225	-	Vdc
	2N3739	-		300	-	
Collector-Emitter Cutoff Current		-	I_{CEO}			mAdc
(V_{CE} = 125 Vdc, I_B = 0)	2N3738			-	0.25	
(V_{CE} = 200 Vdc, I_B = 0)	2N3739			-	0.25	
Collector-Base Cutoff Current		-	I_{CBO}			mAdc
(V_{CB} = 250 Vdc, I_E = 0)	2N3738			-	0.1	
(V_{CB} = 325 Vdc, I_E = 0)	2N3739			-	0.1	
Collector Cutoff Current		4	I_{CEX}			mAdc
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N3738			-	0.5	
(V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N3739			-	0.5	
(V_{CE} = 125 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N3738			-	1.0	
(V_{CE} = 200 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N3739			-	1.0	
Emitter-Base Cutoff Current (V_{BE} = 6 Vdc)	Both Types	-	I_{EBO}	-	0.1	mAdc
ON CHARACTERISTICS						
DC Current Gain*		7	h_{FE}*			-
(I_C = 50 mAdc, V_{CE} = 10 Vdc)	Both Types			30	-	
(I_C = 100 mAdc, V_{CE} = 10 Vdc)	Both Types			40	200	
(I_C = 250 mAdc, V_{CE} = 10 Vdc)	Both Types			25	-	
Collector-Emitter Saturation Voltage* (I_C = 250 mAdc, I_B = 25 mAdc)	Both Types	8	$V_{CE(sat)}$*	-	2.5	Vdc
Base-Emitter "On" Voltage* (I_C = 100 mAdc, V_{CE} = 10 Vdc)	Both Types	3, 4	$V_{BE(on)}$*	-	1.0	Vdc
SMALL SIGNAL CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	Both Types	-	f_T	10	-	MHz
Output Capacitance (V_{CB} = 100 Vdc, I_E = 0, f = 100 kHz)	Both Types	9	C_{ob}	-	20	pF
Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 20 Vdc, f = 1 kHz)	Both Types	-	h_{fe}	35	-	-

*PULSE TEST: PW ≤ 300 μs, Duty Cycle ≤ 2%

FIGURE 2 — ACTIVE-REGION SAFE OPERATING AREAS



The Safe Operating Area Curves indicate I_C-V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

MOTOROLA Semiconductors
BOX 955 • PHOENIX, ARIZONA 85001

2N3738
2N3739

HIGH-VOLTAGE NPN SILICON POWER TRANSISTORS

. . . designed for use in line-operated equipment such as audio output amplifiers; low-current, high-voltage converters; and AC line relays.

- High Voltages — V_{CEO} = 225 V and 300 V
- Excellent dc Gain: h_{FE} = 40-200 @ I_C = 100 mA, V_{CE} = 10 V
- f_T = 10 MHz (Minimum)
- Recommended for use @ I_C = 10-250 mA

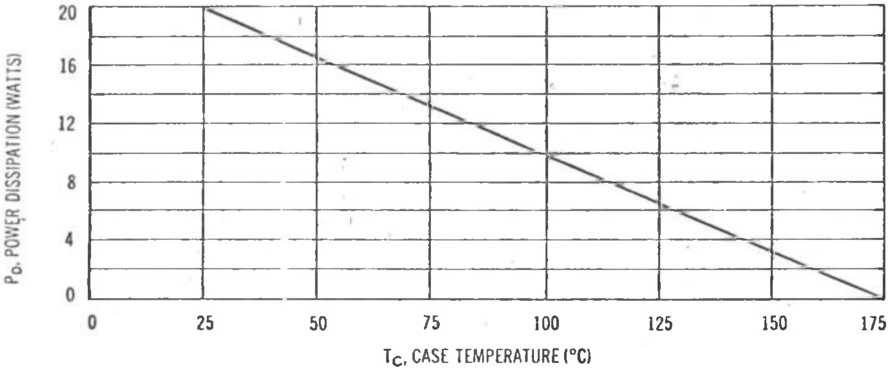
MAXIMUM RATINGS

Characteristic	Symbol	2N3738	2N3739	Unit
Collector-Emitter Voltage	V_{CEO}	225	300	Vdc
Collector-Base Voltage	V_{CB}	250	325	Vdc
Emitter-Base Voltage	V_{EB}	6	6	Vdc
Collector Current	I_C	3		Adc
Base Current	I_B	1		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0. 133		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	7. 5	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE

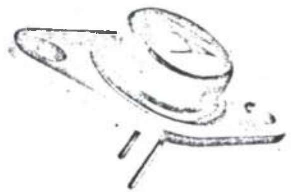


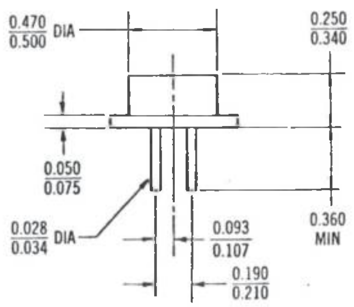
Safe Area Limits are indicated by Figure 2. Both limits are applicable and must be observed.

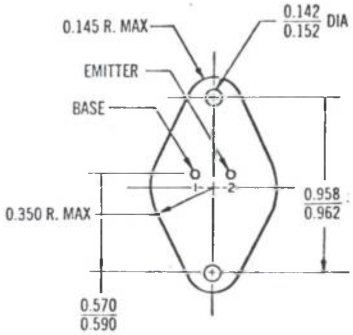
POWER TRANSISTORS

225-300 VOLTS
20 WATTS

AUGUST 1965 — DS3070 R1
(Replaces DS3070)



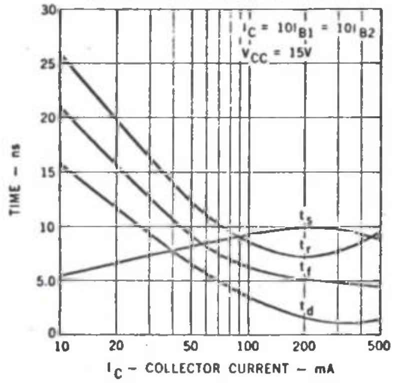




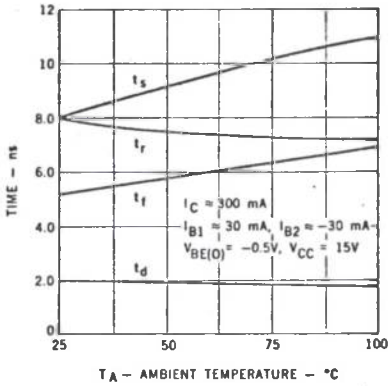
TO-66 OUTLINE
COLLECTOR CONNECTED
TO CASE

POWER TRANSISTORS (Si)
2N3738, 2N3739
DS 3070 R1

TYPICAL ELECTRICAL CHARACTERISTICS

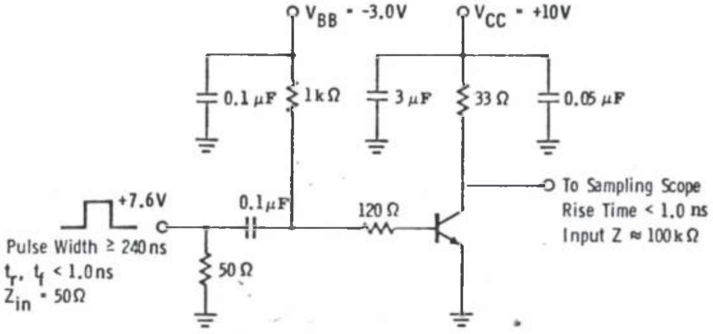


SWITCHING TIMES VERSUS COLLECTOR CURRENT



SWITCHING TIMES VERSUS AMBIENT TEMPERATURE

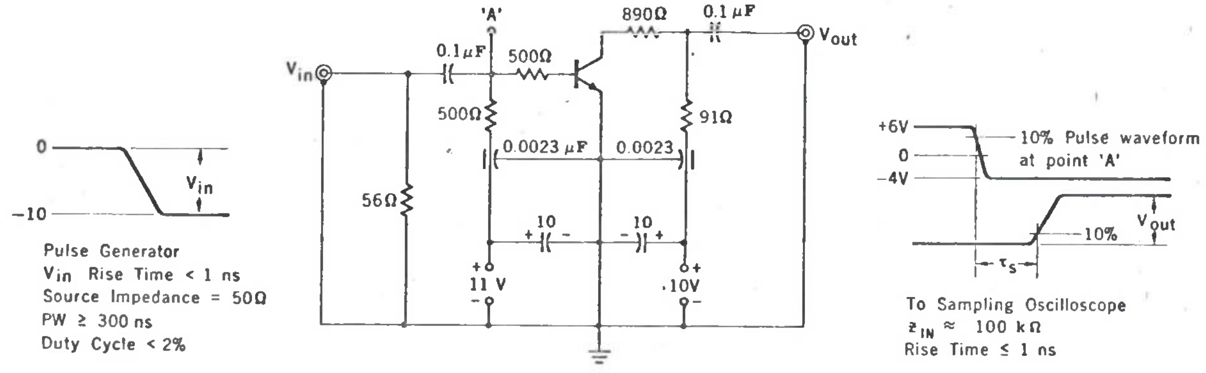
T_{ON} and T_{OFF} TEST CIRCUIT



Pulse Width ≥ 240 ns
t_r, t_f < 1.0 ns
Z_{in} = 50Ω

To Sampling Scope
Rise Time < 1.0 ns
Input Z ≈ 100 kΩ

CHARGE STORAGE TIME MEASUREMENT CIRCUIT

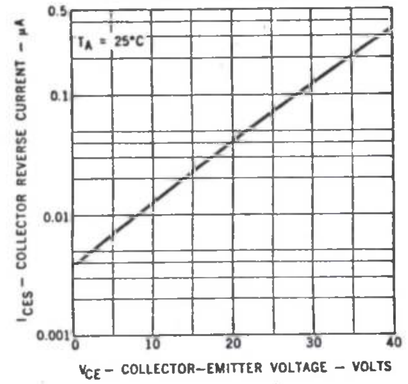


Pulse Generator
V_{in} Rise Time < 1 ns
Source Impedance = 50Ω
PW ≥ 300 ns
Duty Cycle < 2%

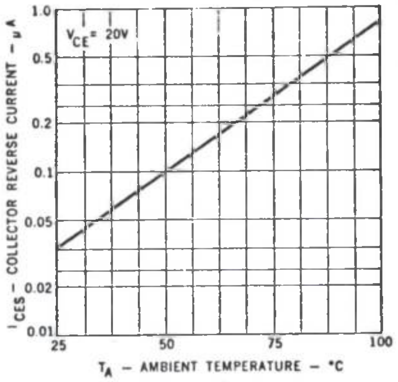
To Sampling Oscilloscope
$Z_{IN} \approx$ 100 kΩ
Rise Time ≤ 1 ns

TYPICAL ELECTRICAL CHARACTERISTICS

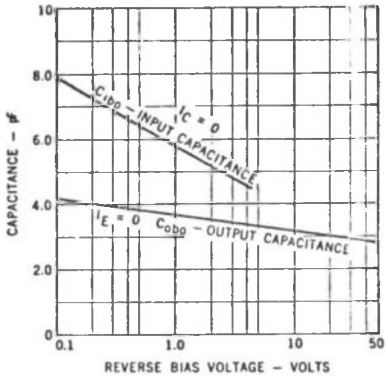
COLLECTOR REVERSE CURRENT VERSUS REVERSE BIAS VOLTAGE



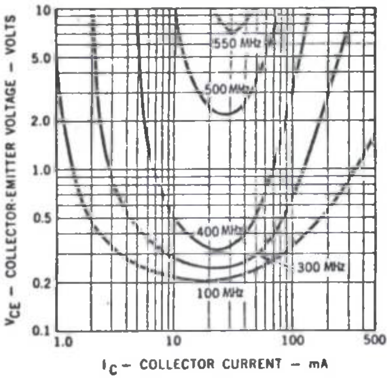
COLLECTOR REVERSE CURRENT VERSUS AMBIENT TEMPERATURE



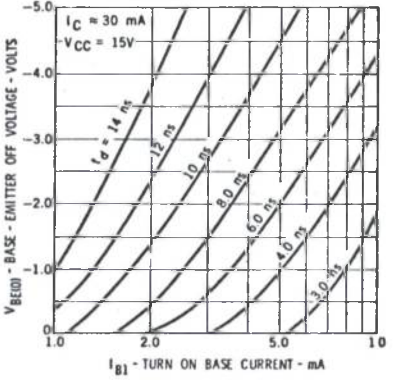
INPUT AND OUTPUT CAPACITANCES VERSUS REVERSE BIAS VOLTAGE



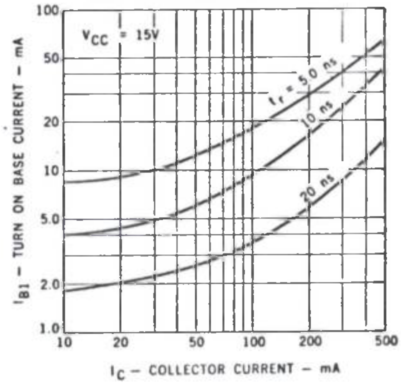
CONTOURS OF CONSTANT GAIN BANDWIDTH PRODUCT (f_T)



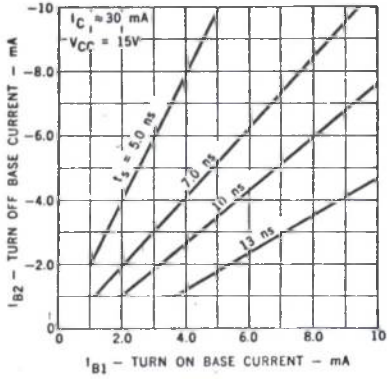
DELAY TIME VERSUS BASE EMITTER OFF VOLTAGE AND TURN ON BASE CURRENT



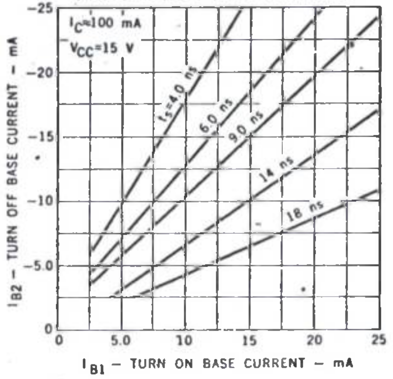
RISE TIME VERSUS COLLECTOR AND TURN ON BASE CURRENTS



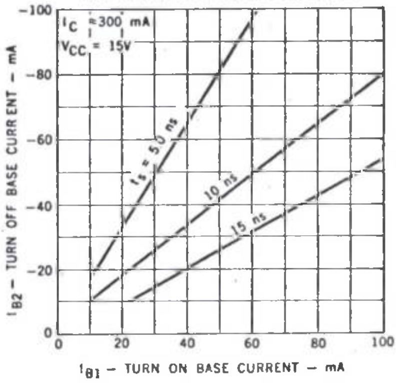
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



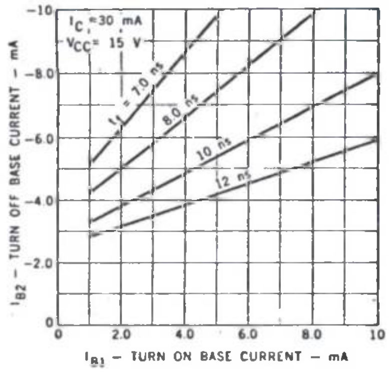
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



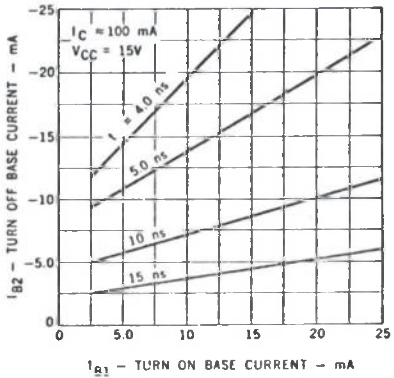
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



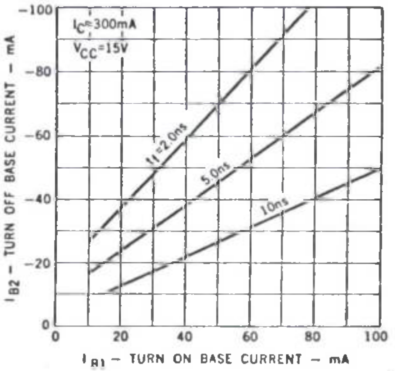
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
BV_{CBO}	Collector to Base Breakdown Voltage	40			Volts	I_C = 100 μA	I_E = 0
BV_{CES}	Collector to Emitter Breakdown Voltage	40			Volts	I_C = 100 μA	V_{EB} = 0
$V_{CEO}(sust)$	Collector to Emitter Sustaining Voltage (Notes 4 and 5)	15			Volts	I_C = 10 mA	I_B = 0
BV_{EBO}	Emitter to Base Breakdown Voltage	5.0			Volts	I_E = 100 μA	I_C = 0
$V_{BE}(sat)$	Base Saturation Voltage (Note 5)	0.75	0.82	0.95	Volts	I_C = 30 mA	I_B = 3.0 mA
$V_{BE}(sat)$	Base Saturation Voltage (Note 5)		0.97	1.2	Volts	I_C = 100 mA	I_B = 10 mA
$V_{BE}(sat)$	Base Saturation Voltage (Note 5)		1.3	1.7	Volts	I_C = 300 mA	I_B = 30 mA
I_{CES}	Collector Reverse Current		0.04	0.5	μA	V_{CE} = 20 V	V_{EB} = 0
$I_{CES}(65°C)$	Collector Reverse Current		0.5	3.0	μA	V_{CE} = 20 V	V_{EB} = 0

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 125°C and junction-to-case thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C). Junction-to-ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).

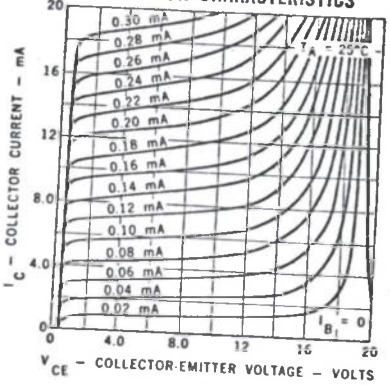
(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest. For more information send for Fairchild Publication APP-4.

(5) Pulse Conditions: length = 300 μsec; duty cycle = 1%.

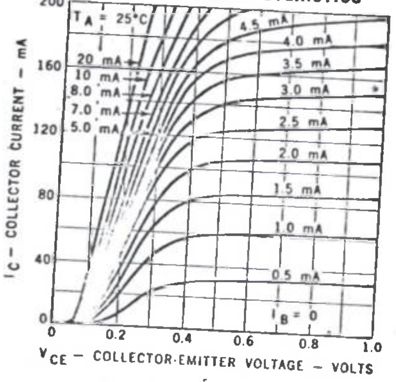
(6) See switching circuits for exact values of I_C, I_{B1}, and I_{B2}.

TYPICAL ELECTRICAL CHARACTERISTICS

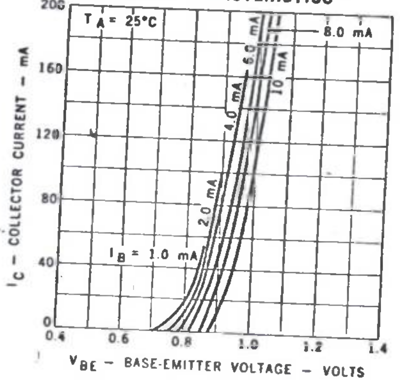
COLLECTOR CHARACTERISTICS*



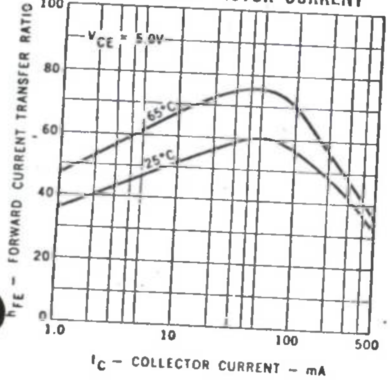
COLLECTOR CHARACTERISTICS*



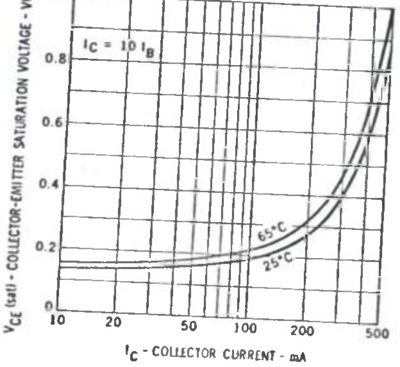
BASE CHARACTERISTICS*



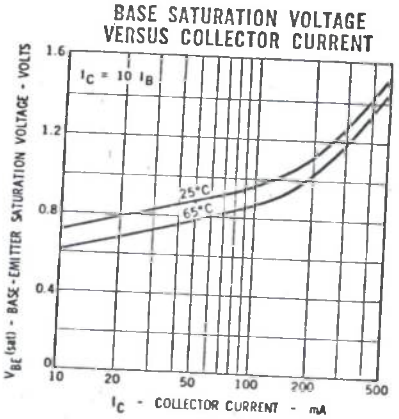
DC PULSE CURRENT GAIN VERSUS COLLECTOR CURRENT



COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



BASE SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



*Single family characteristics on Transistor Curve Tracer

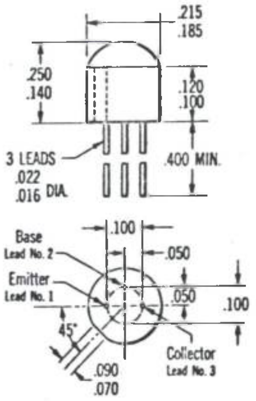
2N3646

FAIRCHILD NPN DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTOR

HIGH SPEED SATURATED SWITCH

The 2N3646 is an NPN silicon PLANAR epitaxial transistor designed for memory applications to 500 milliamperes. It features the unique combination of 350 MHzf_T minimum with a guaranteed 300 milliampere collector saturation voltage of 0.5 volt.

PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Storage Temperature	-55°C to +125°C
Operating Junction Temperature	+125°C Maximum
Lead Temperature (Soldering 10 sec time limit)	+260°C Maximum

Maximum Power Dissipation

Total Dissipation at 25°C Case Temperature (Notes 2 and 3)	0.5 Watt
at 25°C Ambient Temperature (Notes 2 and 3)	0.2 Watt

Maximum Voltages

V_{CBO}	Collector to Base Voltage	40 Volts
V_{CES}	Collector to Emitter Voltage	40 Volts
V_{CEO}	Collector to Emitter Voltage (Note 4)	15 Volts
V_{EBO}	Emitter to Base Voltage	5.0 Volts

ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

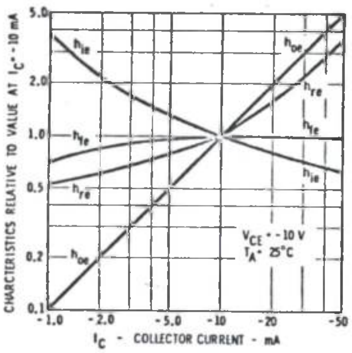
Symbol	Characteristic	Min.	Typ.	Max.	Units		
V_{CE}(sat)	Collector Saturation Voltage (Note 5)		0.16	0.2	Volts	I_C = 30 mA	I_B = 3.0 mA
V_{CE}(sat)	Collector Saturation Voltage (Note 5)		0.18	0.28	Volts	I_C = 100 mA	I_B = 10 mA
V_{CE}(sat)	Collector Saturation Voltage (Note 5) (T_A = +65°C)		0.18	0.3	Volts	I_C = 30 mA	I_B = 3.0 mA
V_{CE}(sat)	Collector Saturation Voltage (Note 5)		0.39	0.5	Volts	I_C = 300 mA	I_B = 30 mA
h_{fe}	High Frequency Current Gain (f = 100 MHz)	3.5	5.5			I_C = 30 mA	V_{CE} = 10 V
τ_s	Charge Storage Time Constant (Note 6)		8.0	18	ns	$I_C = I_{B1} \approx$ 10 mA	$I_{B2} \approx$ -10 mA
t_{on}	Turn On Time (Note 6)		9.0	18	ns	$I_C \approx$ 300 mA	$I_{B1} \approx$ 30 mA
t_{off}	Turn Off Time (Note 6)		15	28	ns	$I_C \approx$ 300 mA, $I_{B1} \approx$ 30 mA, $I_{B2} \approx$ -30 mA	
C_{obo}	Common Base Open Circuit Output Capacitance		3.3	5.0	pF	I_E = 0	V_{CB} = 5.0 V
C_{ibo}	Common Base Open Circuit Input Capacitance		6.6	8.0	pF	I_C = 0	V_{EB} = 0.5 V
h_{FE}	DC Pulse Current Gain (Note 5)	30	60	120		I_C = 30 mA	V_{CE} = 0.4 V
h_{FE}	DC Pulse Current Gain (Note 5)	25	55			I_C = 100 mA	V_{CE} = 0.5 V
h_{FE}	DC Pulse Current Gain (Note 5)	15				I_C = 300 mA	V_{CE} = 1.0 V

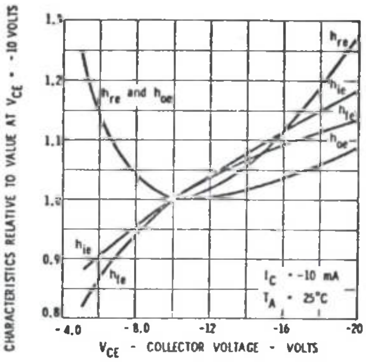
Additional Electrical Characteristics on page 2
Notes on page 2

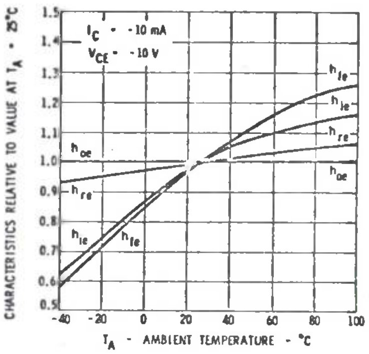
* Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

SMALL SIGNAL CHARACTERISTICS







NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 14 °C/Watt (derating factor of 7.0mW/°C); junction to ambient thermal resistance of 333°C/Watt (derating factor of 3.0 mW/°C).

(4) Rating refers to a high-current point where collector to emitter voltage is lowest. For more information send for Fairchild Publication APP-4/2.

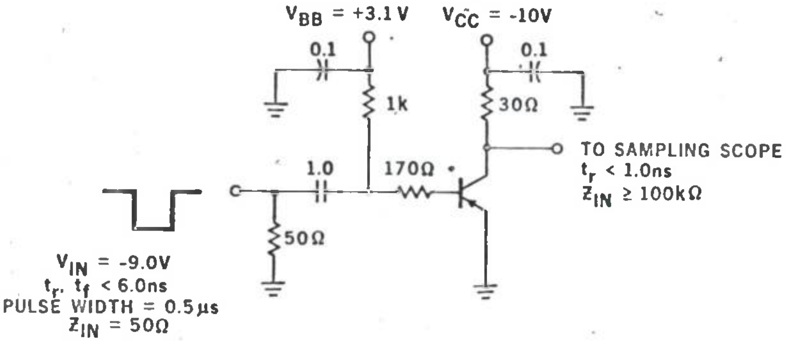
(5) Pulse conditions: length = 300 µs; duty cycle = 1%.

(6) See switching circuit for exact values of I_C, I_{B1}, and I_{B2}.

h PARAMETERS (f = 1.0 kHz)

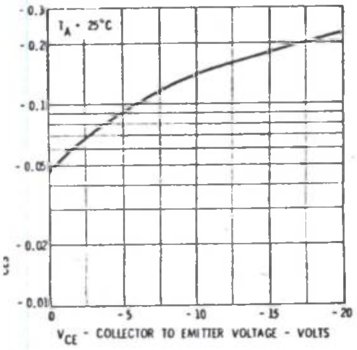
SYMBOL	CHARACTERISTIC	2N3638 MIN.	2N3638 TYP.	2N3638 MAX.	2N3638A MIN.	2N3638A TYP.	2N3638A MAX.	UNITS	TEST CONDITIONS	
h_{ie}	Input Resistance		200	2000		480	2000	ohms	I_C = 10 mA	$V_{CE} = -10$ V
h_{oe}	Output Conductance		80	1200		80	1200	µmhos	I_C = 10 mA	$V_{CE} = -10$ V
h_{re}	Voltage Feedback Ratio		162	2600		162	1500	$\times 10^{-6}$	I_C = 10 mA	$V_{CE} = -10$ V
h_{fe}	Small Signal Current Gain	25	74		100	180			I_C = 10 mA	$V_{CE} = -10$ V

T_{ON} and T_{OFF} TEST CIRCUIT

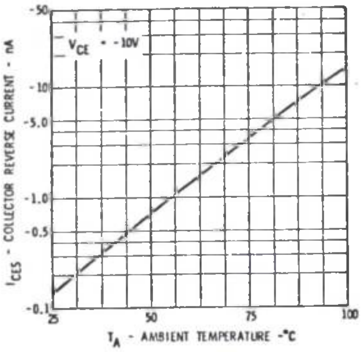


TYPICAL ELECTRICAL CHARACTERISTICS

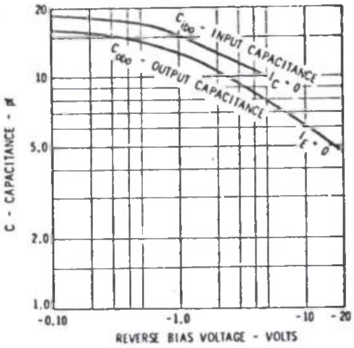
COLLECTOR REVERSE CURRENT VERSUS REVERSE BIAS VOLTAGE



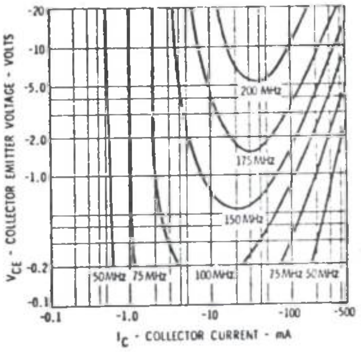
COLLECTOR-BASE DIODE REVERSE CURRENT VERSUS TEMPERATURE



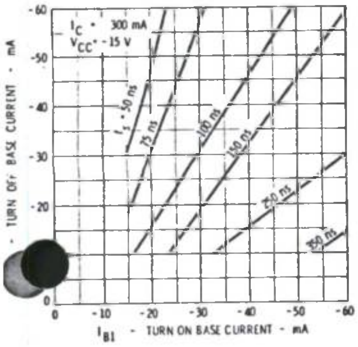
INPUT AND OUTPUT CAPACITANCE VERSUS REVERSE BIAS VOLTAGE



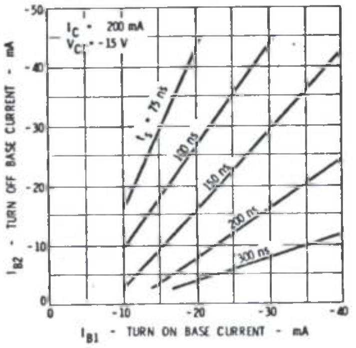
CONTOURS OF CONSTANT GAIN BANDWIDTH PRODUCT (f_T)



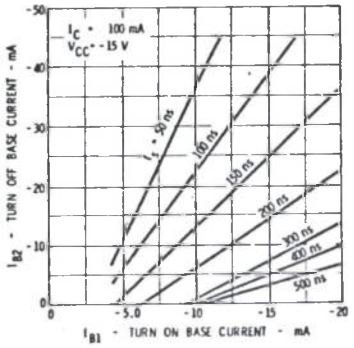
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENT



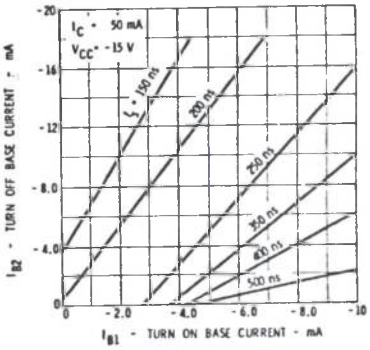
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENT



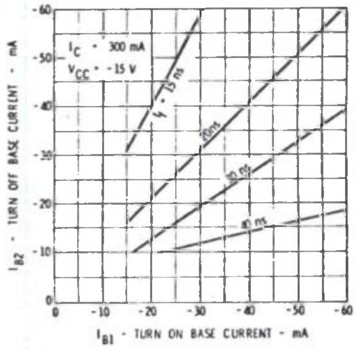
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENT



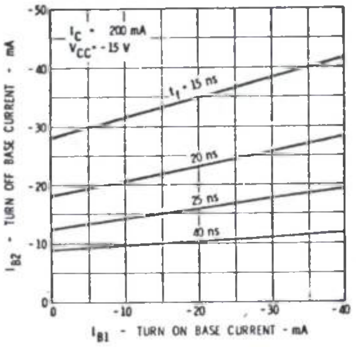
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENT



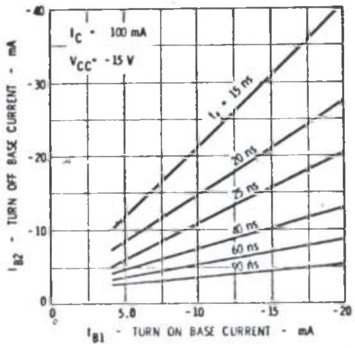
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



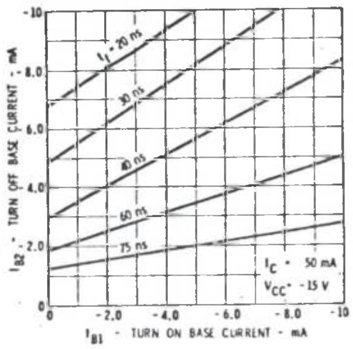
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



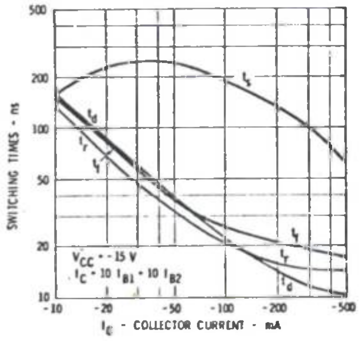
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



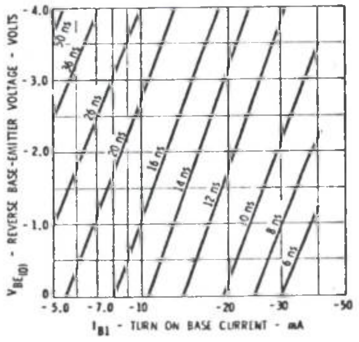
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



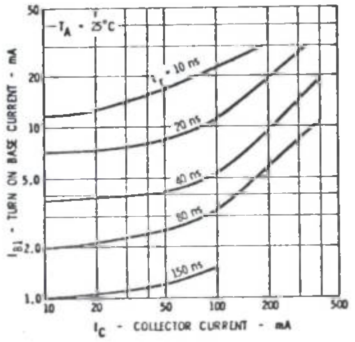
SWITCHING TIMES VERSUS COLLECTOR CURRENT



DELAY TIME VERSUS TURN ON BASE CURRENT AND REVERSE BASE EMITTER VOLTAGE



RISE TIME VERSUS TURN ON BASE CURRENT AND COLLECTOR CURRENT

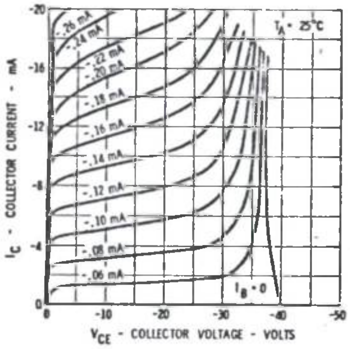


ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

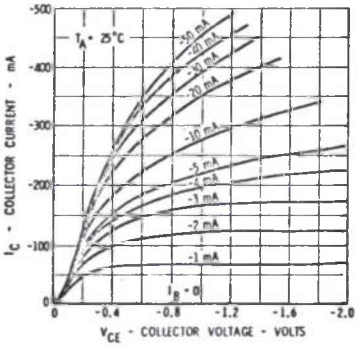
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
V_{BE}(sat)	Base-Emitter Saturation Voltage (pulsed, Note 5)		−0.9	−1.1	Volts	$I_C = 50$ mA	$I_B = 2.5$ mA
V_{BE}(sat)	Base-Emitter Saturation Voltage (pulsed, Note 5)	−0.8	−1.25	−2.0	Volts	$I_C = 300$ mA	$I_B = 30$ mA
BV_{EBO}	Emitter to Base Breakdown Voltage	−4.0			Volts	$I_E = 100\ \mu A$	$I_C = 0$
I_{CES}	Collector Reverse Current		0.1	35	nA	$V_{CE} = -15$ V	$V_{EB} = 0$
I_{CES}(65°C)	Collector Reverse Current		0.002	2.0	μA	$V_{CE} = -15$ V	$V_{EB} = 0$

TYPICAL ELECTRICAL CHARACTERISTICS

2N3638



COLLECTOR CHARACTERISTICS*



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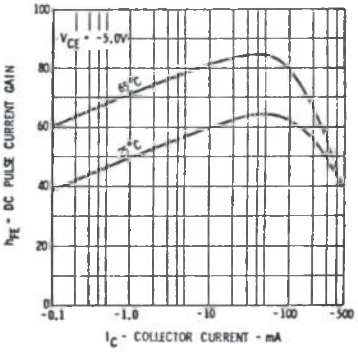
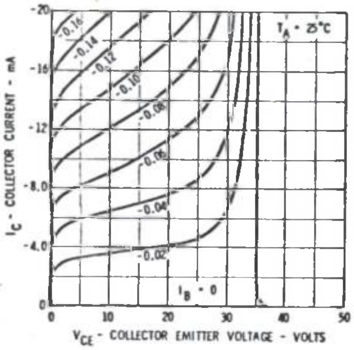
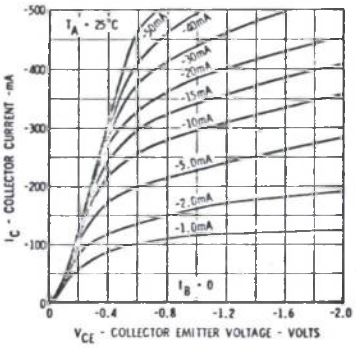


DC PULSE CURRENT GAIN VERSUS COLLECTOR CURRENT

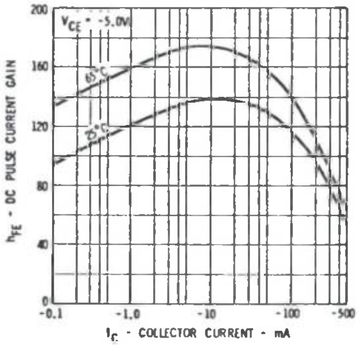
2N3638A



COLLECTOR CHARACTERISTICS*

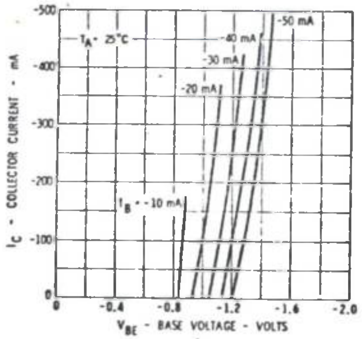


COLLECTOR CHARACTERISTICS*

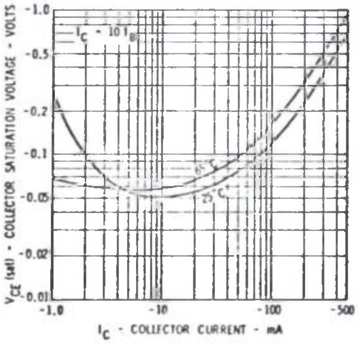


DC PULSE CURRENT GAIN VERSUS COLLECTOR CURRENT

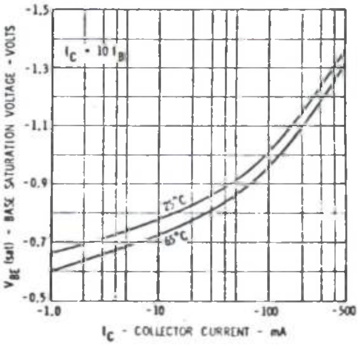
2N3638 • 2N3638A



BASE CHARACTERISTICS*



COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



BASE SATURATION VOLTAGE VERSUS COLLECTOR CURRENT

* Single family characteristics on Transistor Curve Tracer.

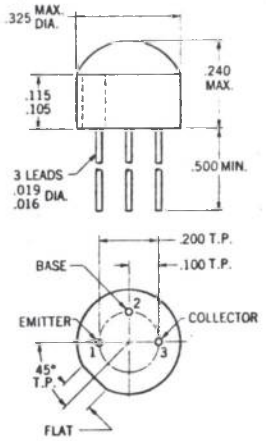
2N3638 · 2N3638A

PNP HIGH CURRENT SWITCHES

DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

- FAST SWITCHING - - $t_{on} = 75$ ns (max.) @ 300 mA
  - - $t_{off} = 170$ ns (max.) @ 300 mA
- HIGH BETA - - h_{FE} 100 (min.) @ $I_C = 50$ mA
- HIGH CURRENT - - Up to 500 mA
- LOW V_{CE}(sat) - - 1.0 Volt (max.) @ 300 mA
- LOW COST IN ALL QUANTITIES

PHYSICAL DIMENSIONS
Epoxy package
TO-105



NOTES: All dimensions in inches
Leads are gold-plated kovar
Package is electrically Non-conductive material
Package weight is 0.66 gram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures			
	Storage Temperature		−55°C to +125°C
	Operating Junction Temperature		+125°C Maximum
	Lead Temperature (Soldering, 10 sec time limit)		+260°C Maximum
Maximum Power Dissipation			
	Total Dissipation at 25°C Case Temperature	(Notes 2 and 3)	0.7 Watt
	at 25°C Free Air Temperature	(Notes 2 and 3)	0.3 Watt
Maximum Voltages and Current			
V_{CBO}	Collector to Base Voltage		−25 Volts
V_{CES}	Collector to Emitter Voltage		−25 Volts
V_{CEO}	Collector to Emitter Voltage	(Note 4)	−25 Volts
V_{EBO}	Emitter to Base Voltage		−4.0 Volts
I_C	Collector Current	(Note 2)	500 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N3638 MIN.	2N3638 TYP.	2N3638 MAX.	2N3638A MIN.	2N3638A TYP.	2N3638A MAX.	UNITS	TEST CONDITIONS	
h_{FE}	DC Pulse Current Gain (Note 5)				80	140			$I_C = 1.0$ mA	$V_{CE} = -10$V
h_{FE}	DC Pulse Current Gain (Note 5)	20	70		100	160			$I_C = 10$ mA	$V_{CE} = -10$V
h_{FE}	DC Pulse Current Gain (Note 5)	30	67		100	130			$I_C = 50$ mA	$V_{CE} = -1.0$ V
h_{FE}	DC Pulse Current Gain (Note 5)	20	40		20	50			$I_C = 300$ mA	$V_{CE} = -2.0$ V
V_{CE}(sat)	Pulsed Collector Saturation Voltage (Note 5)		−0.08	−0.25		−0.08	−0.25	Volt	$I_C = 50$ mA	$I_B = 2.5$ mA
V_{CE}(sat)	Pulsed Collector Saturation Voltage (Note 5)		−0.38	−1.0		−0.38	−1.0	Volt	$I_C = 300$ mA	$I_B = 30$ mA
V_{CEO}(sust)	Collector to Emitter Sustaining Voltage (Notes 4 & 5)	−25			−25			Volts	$I_C = 10$ mA (pulsed)	$I_B = 0$
BV_{CBO}	Collector to Base Breakdown Voltage	−25			−25			Volts	$I_C = 100\ \mu$A	$I_E = 0$
BV_{CES}	Collector to Emitter Breakdown Voltage	−25			−25			Volts	$I_C = 100\ \mu$A	$V_{EB} = 0$
t_{on}	Turn On Time (Note 6)		28	75		28	75	ns	$I_C \approx 300$ mA	$I_{B1} \approx 30$ mA
t_{off}	Turn Off Time (Note 6)		110	170		110	170	ns	$I_C \approx 300$ mA	$I_{B1} \approx 30$ mA $I_{B2} \approx -30$ mA
h_{fe}	High Frequency Current Gain (f = 100 MHz)	1.0	1.9		1.5	1.9			$I_C = 50$ mA	$V_{CE} = -3.0$ V
C_{obo}	Common-Base, Open-Circuit Output Capacitance		6.0	20		6.0	10	pF	$I_E = 0$	$V_{CB} = -10$ V
C_{ibo}	Common-Base, Open-Circuit Input Capacitance		18	65		18	25	pF	$I_C = 0$	$V_{EB} = -0.5$ V

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD TRANSISTOR 2N3569

SMALL SIGNAL CHARACTERISTICS (f=1.0KC)

Symbol	Characteristic	Typical	Units	Test Conditions	
h_{ie}	Input Resistance	3800	Ohms	I_C = 1.0 mA	V_{CE} = 5.0 V
h_{oe}	Output Conductance	19.2	μmhos	I_C = 1.0 mA	V_{CE} = 5.0 V
h_{re}	Voltage Feedback Ratio	5.6	$x10^{-4}$	I_C = 1.0 mA	V_{CE} = 5.0 V
h_{fe}	Small Signal Current Gain	130		I_C = 1.0 mA	V_{CE} = 5.0 V

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 125°C and junction-to-case thermal resistance of 125°C/Watt (derating factor of 8.0 mW/°C; junction-to-ambient thermal resistance of 333°C/Watt (derating factor of 3.0 mW/°C.

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300 μsec; duty cycle ≤ 1%.

~~2N3569~~

NPN GENERAL PURPOSE TYPE

DIFFUSED SILICON PLANAR EPITAXIAL TRANSISTOR

The 2N3569 is an NPN silicon PLANAR epitaxial transistor designed primarily for amplifier and switching applications over a wide range of voltage and current. This device features a useful beta range to 500 mA and low saturation voltage. High collector-to-emitter voltage allows operation to 40 volts.

ABSOLUTE MAXIMUM RATINGS [Note 1]

Maximum Temperatures

Storage Temperature	-55°C to +125°C
Operating Junction Temperature	+125°C Maximum
Lead Temperature (Soldering, 10 sec time limit)	+260°C Maximum

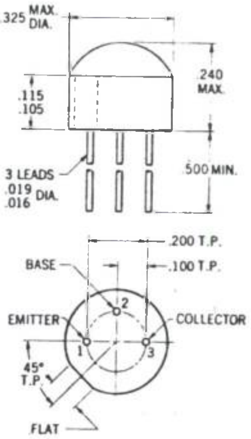
Maximum Power Dissipation

Total Dissipation at 25°C Case Temperature	(Notes 2 and 3)	0.8 Watt
at 25°C Free Air Temperature	(Notes 2 and 3)	0.3 Watt

Maximum Voltages

V_{CBO}	Collector to Base Voltage		80 Volts
V_{CEO}	Collector to Emitter Voltage	(Note 4)	40 Volts
V_{EBO}	Emitter to Base Voltage		5.0 Volts

PHYSICAL DIMENSIONS
Epoxy package
TO-105



NOTES: All dimensions in inches
Leads are gold plated kovar
Package is electrically Non-conductive material
Package weight is 0.66 gram

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Characteristic		Min.	Typ.	Max.	Units	Test Conditions	
h_{FE}	DC Pulse Current Gain	(Note 5)	100	150	300		I_C = 150 mA	V_{CE} = 1.0 V
h_{FE}	DC Pulse Current Gain	(Note 5)	100				I_C = 30 mA	V_{CE} = 1.0 V
$V_{CE}(sat)$	Collector Saturation Voltage (pulsed, see note 5)			0.1	0.25	Volts	I_C = 150 mA	I_B = 15 mA
$V_{BE}(sat)$	Base Saturation Voltage (pulsed, see note 5)			0.85	1.1	Volts	I_C = 150 mA	I_B = 15 mA
h_{fe}	High Frequency Current Gain (f = 20 Mc)		3.0				I_C = 50 mA	V_{CE} = 10 V
C_{obo}	Common Base Open Circuit Output Capacitance			18	20	pf	I_E = 0	V_{CB} = 10 V
C_{ibo}	Common Base Open Circuit Input Capacitance			44	80	pf	I_C = 0	V_{EB} = 0.5 V
I_{CBO}	Collector Cutoff Current				50	nA	I_E = 0	V_{CB} = 40 V
$I_{CBO}(75°C)$	Collector Cutoff Current				5.0	μA	I_E = 0	V_{CB} = 40 V
I_{EBO}	Emitter Cutoff Current				25	nA	I_C = 0	V_{EB} = 4.0 V
BV_{CBO}	Collector to Base Breakdown Voltage		80			Volts	I_C = 100 μA	I_E = 0
$V_{CEO}(sust)$	Collector to Emitter Sustaining Voltage (Notes 4 and 5)		40			Volts	I_C = 30 mA (pulsed)	I_B = 0
BV_{EBO}	Emitter to Base Breakdown Voltage		5.0			Volts	I_E = 10 μA	I_C = 0

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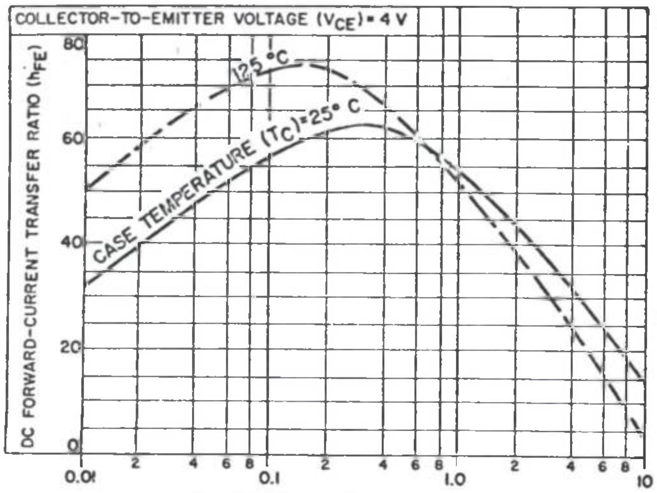
TYPICAL DC-BETA CHARACTERISTICS FOR TYPE 2N3055



92CS-12301R1

Fig. 26

TYPICAL INPUT CHARACTERISTICS FOR TYPE 2N3055

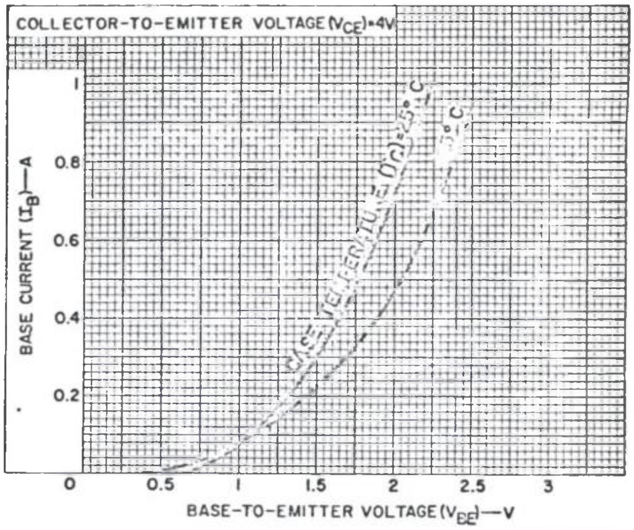


Fig. 27

92CS-12307R1

TYPICAL OUTPUT CHARACTERISTICS FOR TYPE 2N3055

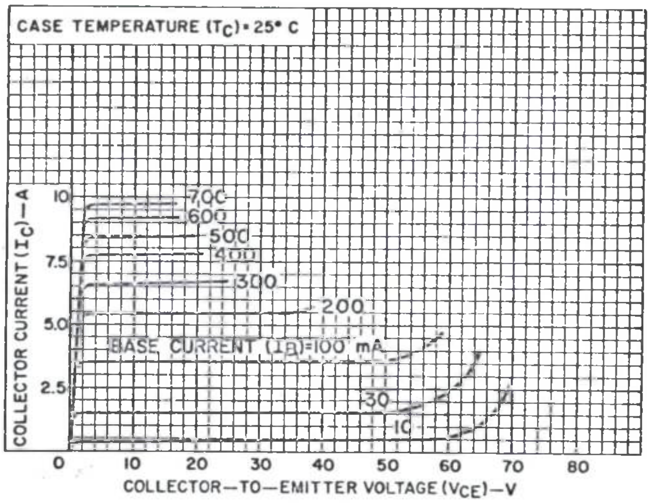


Fig. 28

92CS-12306R1

TYPICAL TRANSFER CHARACTERISTICS FOR TYPE 2N3055

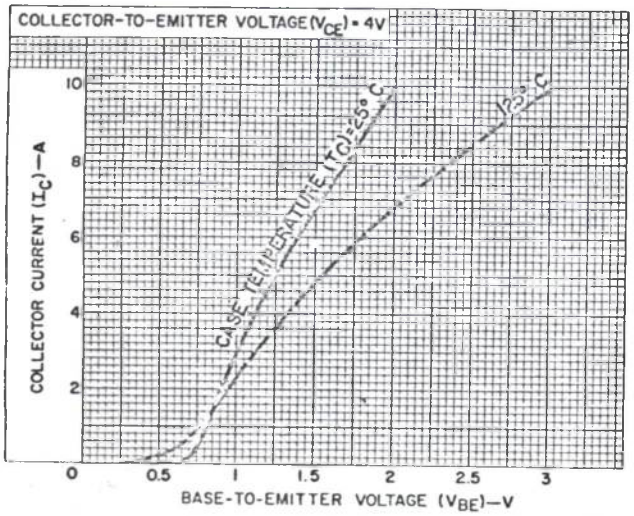
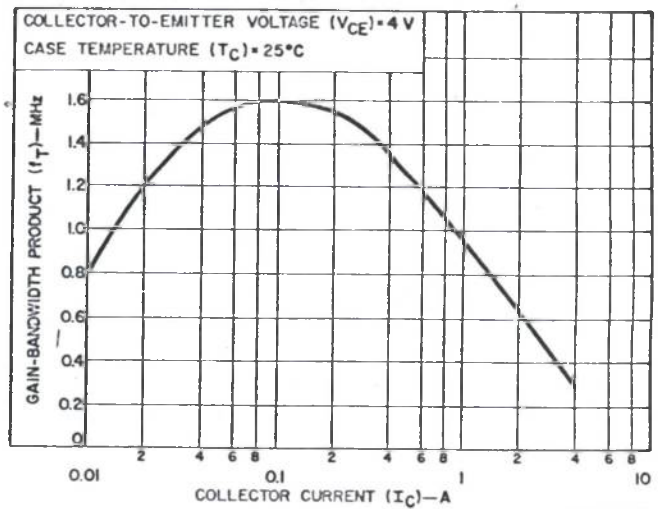


Fig. 29

92CS-12326R1

TYPICAL GAIN-BANDWIDTH PRODUCT FOR TYPE 2N3055



92SS-3378

Fig. 30

REVERSE-BIAS, SECOND-BREAKDOWN CHARACTERISTICS FOR TYPE 2N3054

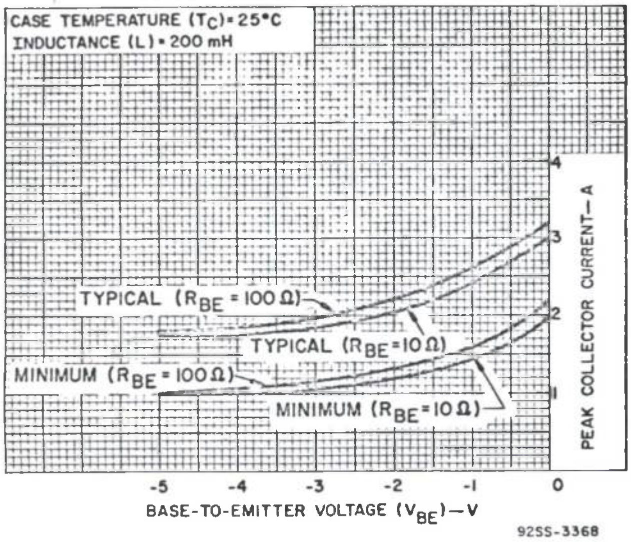


Fig. 13

REVERSE-BIAS, SECOND-BREAKDOWN CHARACTERISTICS FOR TYPE 2N3055

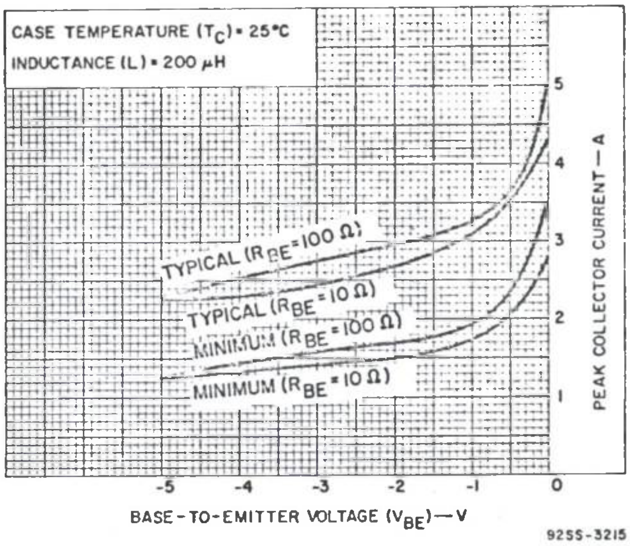


Fig. 14

TYPICAL DC-BETA CHARACTERISTICS

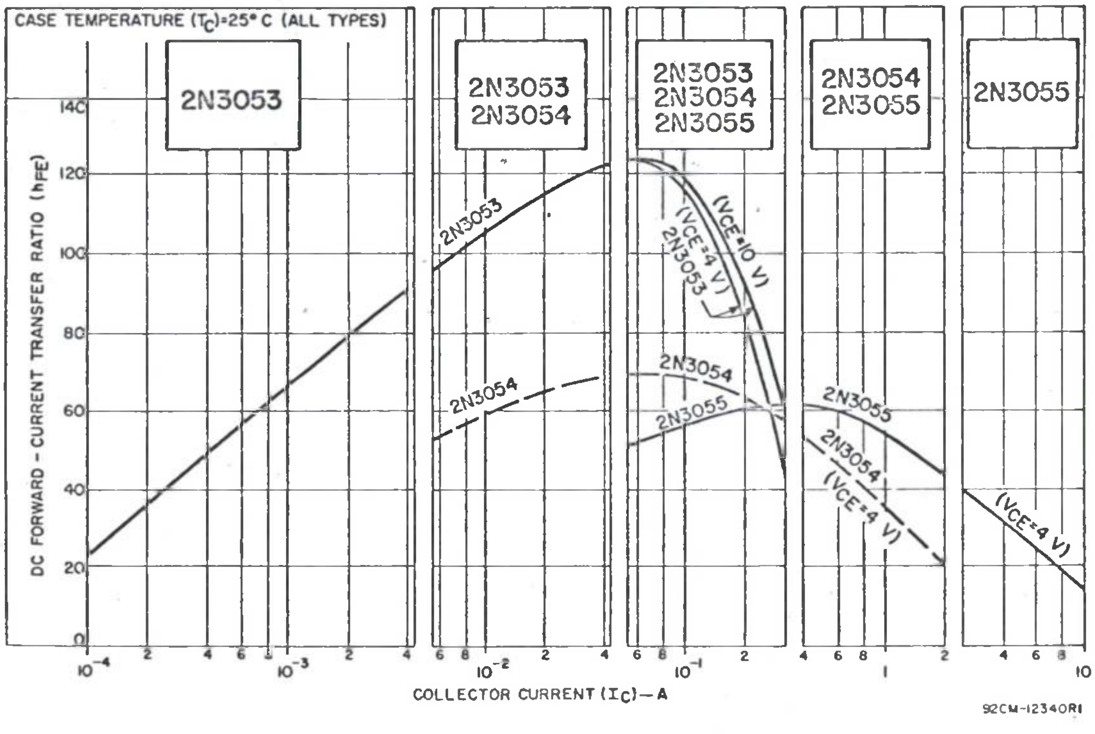
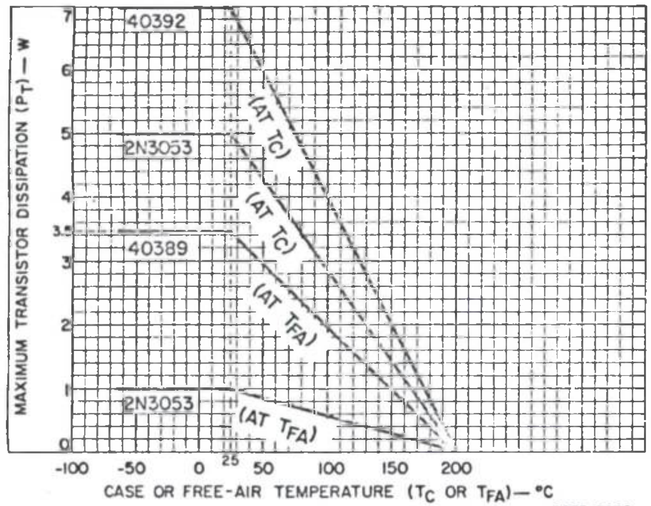


Fig. 15

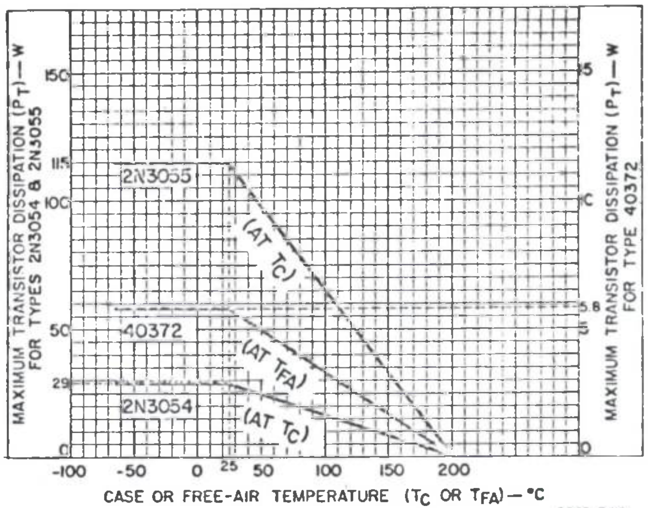
DISSIPATION DERATING CURVE FOR TYPES 2N3053, 40389, & 40392



92SS-3002

Fig. 5

DISSIPATION DERATING CURVE FOR TYPES 2N3054, 40372, & 2N3055



92SS-3001

Fig. 6

SUSTAINING VOLTAGE vs. BASE-TO-EMITTER RESISTANCE FOR TYPE 2N3053

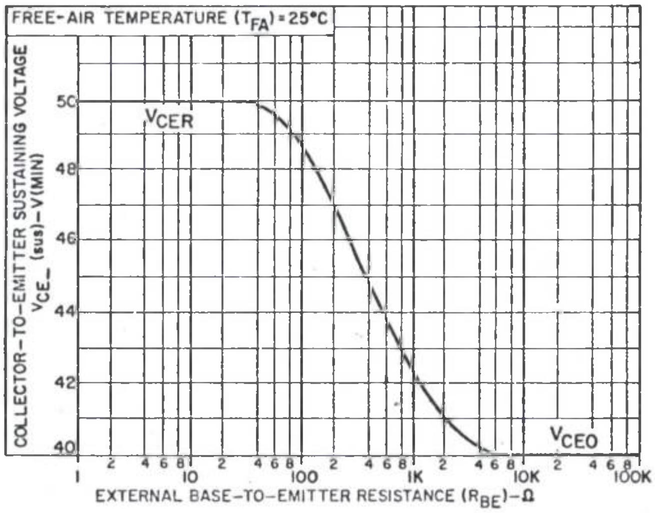


Fig. 7

92CS-12332R2

SUSTAINING VOLTAGE vs. BASE-TO-EMITTER RESISTANCE FOR TYPE 2N3054

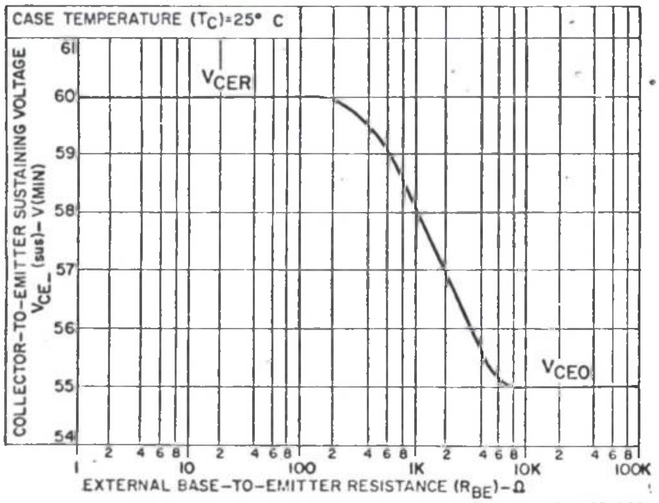


Fig. 8

92CS-12322R2

SUSTAINING VOLTAGE vs. BASE-TO-EMITTER RESISTANCE FOR TYPE 2N3055

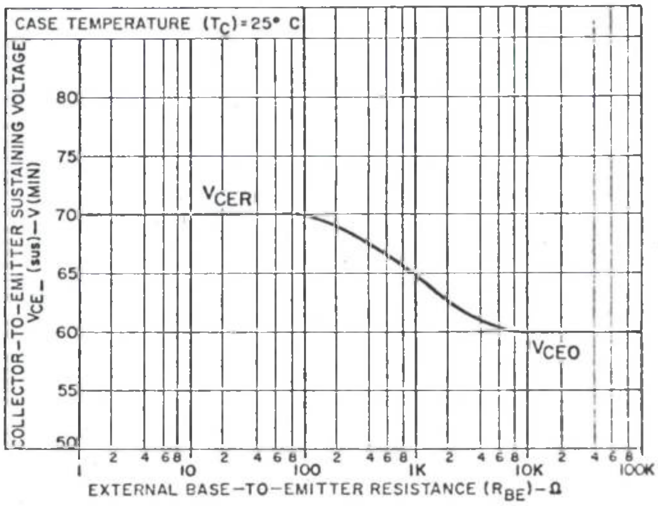


Fig. 9

92CS-12321R2

MAXIMUM OPERATING AREAS FOR TYPE 2N3055

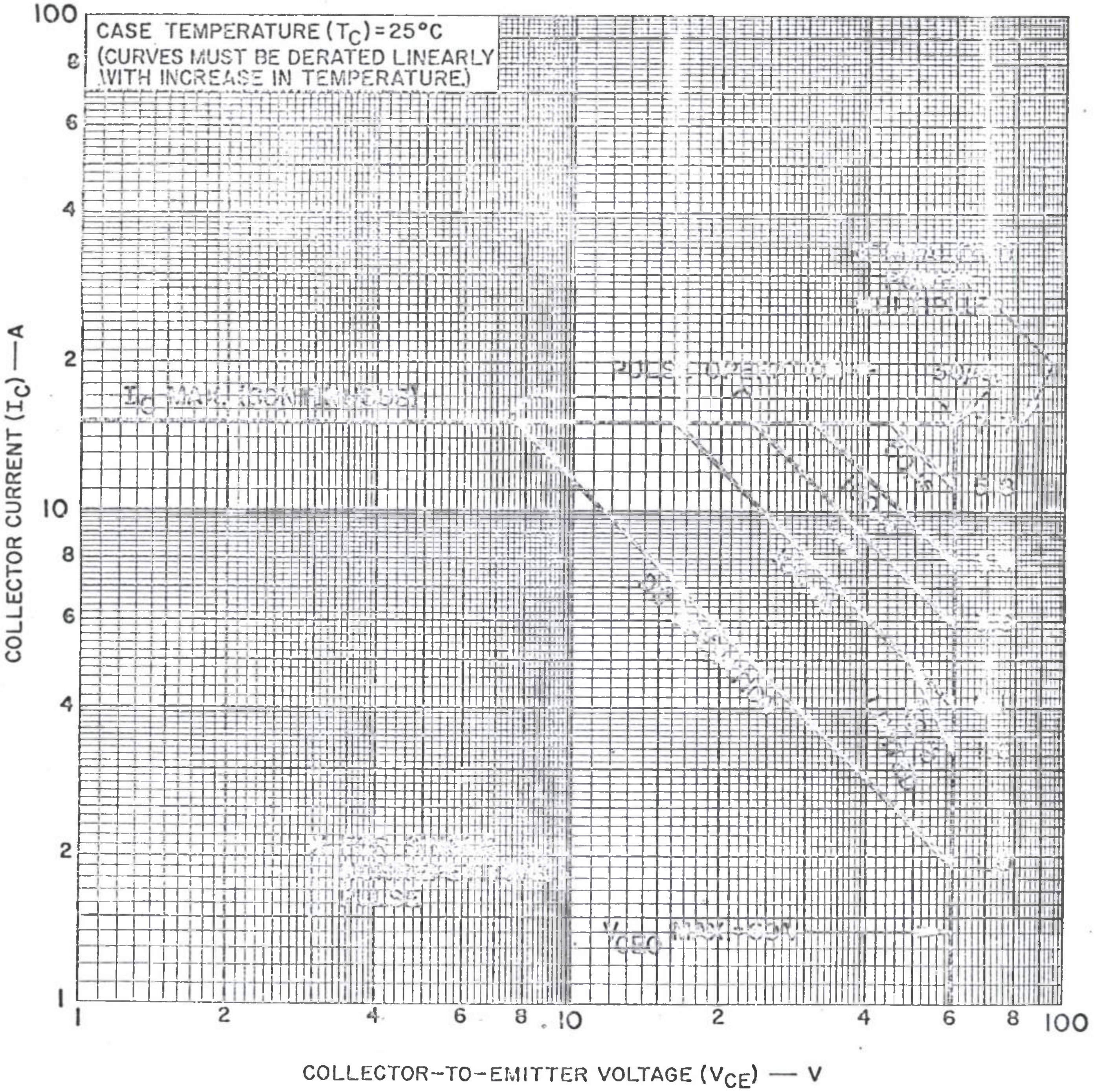


Fig. 4

ELECTRICAL CHARACTERISTICS

Case Temperature (T_C) = 25°C, Unless Otherwise Specified

Characteristics	Symbol	TEST CONDITIONS							LIMITS						Units
		DC Collector Volts		DC Emitter or Base Volts		DC Current milliamperes			Types 2N3053 40389 40392		Types 2N3054 40372		Type 2N3055		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	Min.	Max.	Min.	Max.	Min.	Max.	
Collector-Cutoff Current	I_{CBO}	30					0		—	0.25	—	—	—	—	μA
	I_{CEV}		90		-1.5				—	—	—	1.0	—	—	mA
			100		-1.5				—	—	—	—	—	5.0	
At T_C = 150°C	I_{CEV}		30		-1.5				—	—	—	5.0	—	—	mA
			60		-1.5				—	—	—	—	—	10.0	
Emitter-Cutoff Current	I_{EBO}			4		0			—	0.25	—	—	—	—	μA
				7		0			—	—	—	1.0	—	—	mA
				7		0			—	—	—	—	—	5.0	mA
DC Forward-Current Transfer Ratio	h_{FE}		10			150[a]			50	250	—	—	—	—	
			4			500			—	—	25	100	—	—	
			4			4 A[a]			—	—	—	—	20	70	
Collector-to-Base Breakdown Voltage	BV_{CBO}					0.1	0		60	—	—	—	—	—	V
Emitter-to-Base Breakdown Voltage	BV_{EBO}					0	0.1		5	—	—	—	—	—	V
						0	1		—	—	7	—	—	—	
						0	5		—	—	—	—	7	—	
Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$					100[a]		0	40	—	—	—	—	—	V
						100		0	—	—	55	—	—	—	
						200		0	—	—	—	—	60	—	
With base-emitter junction reverse biased	$V_{CEV}(sus)$				-1.5	100			—	—	—	—	100	—	V
With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{CER}(sus)$					100[a]			50	—	—	—	—	—	V
= 100 Ω						100			—	—	60	—	—	—	
= 100 Ω						200			—	—	—	—	70	—	
Base-to-Emitter Voltage	V_{BE}		4			500			—	—	—	1.7	—	—	V
			4			4 A[a]			—	—	—	—	—	1.8	
Base-to-Emitter Saturation Voltage						150		15	—	1.7	—	—	—	—	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					150		15	—	1.4	—	—	—	—	V
						500		50	—	—	—	1.0	—	—	
						4 A[a]		400	—	—	—	—	—	1.1	
Small-Signal, Forward Current Transfer Ratio (At 20 MHz)	h_{fe}		10			50			5	—	—	—	—	—	
Gain-Bandwidth Product	f_T					200			—	—	800	—	—	—	kHz
						1 A			—	—	—	—	800	—	
Output Capacitance	C_{ob}	10					0		—	15	—	—	—	—	pF
Input Capacitance	C_{ib}			0.5		0			—	80	—	—	—	—	pF
Power Rating Test	PRT		39			3 A			—	—	—	—	—	1[b]	s
Thermal Resistance: Junction-to-Case	θ_{J-C}								35(max.) 2N3053		6(max.) 2N3054		—	1.5	°C/W
									25(max.) 40392				—		°C/W
Junction-to-Free Air	θ_{J-FA}								175(max.) 2N3053		30(max.) 40372		—	—	°C/W
									50(max.) 40389				—	—	°C/W

[a] Pulsed; pulse duration = 300μs, duty factor = 1.8%.

[b] At 115W.

RCA POWER TRANSISTORS

2N3053 2N3054 2N3055

~~Including~~

40372 40389 40392

File No. 145

RCA-2N3053, 2N3054* , and 2N3055* are silicon n-p-n transistors intended for a wide variety of medium to high-power applications.

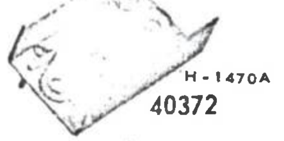
The 2N3053 is a triple-diffused planar type useful up to 20 MHz in small-signal, medium-power applications.

The 2N3054 and 2N3055 are Hometaxial-base** types useful for power-switching circuits, for series- and shunt-regulator driver and output stages, and for high-fidelity amplifiers.

* Formerly Dev. Type Nos. TA2402A and TA2403A, respectively.

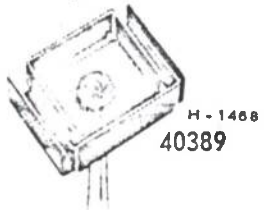
**"Hometaxial" was coined by RCA from "homogeneous" and "axial" to describe a single-diffused transistor with a base region of homogeneous-resistivity silicon in the axial direction (emitter-to-collector).

ALSO AVAILABLE. . .


H-1470A

40372

Type 40372 is a 2N3054 with a factory-attached heat radiator.


H-1468

40389

Type 40389 is a 2N3053 with a factory-attached heat radiator.

Types 40372 and 40389 are intended for printed-circuit-board applications.

H-1378

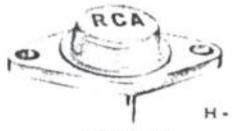
40392

Type 40392 is a 2N3053 with a factory-attached diamond-shaped mounting flange.

MAXIMUM RATINGS

Absolute-Maximum Values:		2N3053 40389, 40392	2N3054 40372	2N3055	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	60	90	100	V
COLLECTOR-TO-EMITTER VOLTAGE:					
With −1.5 V (V_{BE}) of reverse bias.	$V_{CEV}(sus)$	60	90	100	V
With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{CER}(sus)$	50	—	—	V
= 100 Ω	$V_{CER}(sus)$	—	60	70	V
With base open	$V_{CEO}(sus)$	40	55	60	V
EMITTER-TO-BASE VOLTAGE.	V_{EBO}	5	7	7	V
COLLECTOR CURRENT	I_C	0.7	4	15	A
BASE CURRENT	I_B	—	2	7	A
TRANSISTOR DISSIPATION:.	P_T				
At case temperatures up to 25°C		5(2N3053)	29(2N3054)	115	W
		7(40392)	—	—	W
At free-air temperatures up to 25°C. . . .		1(2N3053)	5.8(40372)	—	W
		3.5(40389)	—	—	W
At temperatures above 25°C, See Figs. .		1, 2, & 5	2, 3, & 6	2, 4, & 6	
TEMPERATURE RANGE:					
Storage & Operating (Junction).		←	−65 to 200	→	°C
LEAD OR PIN TEMPERATURE (During soldering):					
At distance ≥ 1/32" from seating plane for 10 s max.		255	235	235	°C

SILICON N-P-N GENERAL-PURPOSE TYPES FOR INDUSTRIAL AND COMMERCIAL APPLICATIONS


H-1340

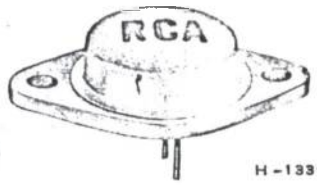
2N3054

JEDEC TO-66

H-1380

2N3053

JEDEC TO-5


H-1339

2N3055

JEDEC TO-3

- Maximum area-of-operation curves for DC and pulse operation
- Now possible to determine maximum operating conditions for operation free from second breakdown

2N3053

- Low leakage current (I_{CBO}) and wide beta (h_{FE}) range

2N3054

- $V_{CEV}(sus)$ = 90 V min.
- Low saturation voltage, $V_{CE}(sat)$ = 1.0 V (at I_C = 0.5 A)

2N3055

- High dissipation capability -- 115 W
- $V_{CEV}(sus)$ = 100 V min.
- Low saturation voltage, $V_{CE}(sat)$ = 1.1 V (at I_C = 4 A)

RADIO CORPORATION OF AMERICA
ELECTRONIC COMPONENTS AND DEVICES, HARRISON, N.J.

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Marca(s) Registrada(s)

Printed in U.S.A.
2N3053, 40389, 40392,
2N3054, 40372, 2N3055 8/66
Supersedes issue dated 10/64

SMALL SIGNAL CHARACTERISTICS (f=1.0 kHz)

Symbol	Characteristic	Typical	Units	Test Conditions	
[illegible]$_{ie}$	Input Resistance	1800	Ohms	I_C = 1.0 mA	V_{CE} = 5.0 V
h_{oe}	Output Conductance	8.0	μmhos	I_C = 1.0 mA	V_{CE} = 5.0 V
h_{re}	Voltage Feedback Ratio	2.1	$x10^{-4}$	I_C = 1.0 mA	V_{CE} = 5.0 V
h_{fe}	Small Signal Current Gain	60		I_C = 1.0 mA	V_{CE} = 5.0 V

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 125°C and junction-to-case thermal resistance of 125°C/Watt (derating factor of 8.0 mW/°C; junction-to-ambient thermal resistance of 333°C/Watt (derating factor of 3.0 mW/°C.

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest. For more information send for Fairchild Publication APP-4/2.

(5) Pulse Conditions: length = 300 μs; duty cycle ≤ 1%.

2N5133

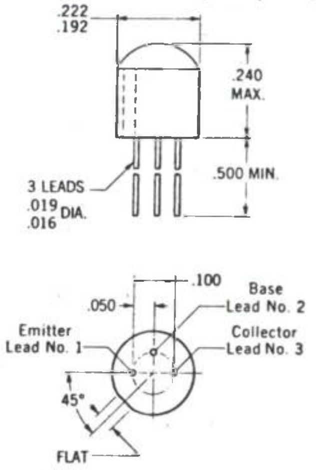
NPN HIGH-GAIN, LOW-NOISE AMPLIFIER

DIFFUSED SILICON PLANAR* TRANSISTOR

- LOW NOISE - - NF = 1.5 dB (TYP) @ 1.0 kHz
- HIGH GAIN - - h_{FE} = 60 (MIN), 220 (TYP) @ 1.0 mA
  h_{FE} = 50 (TYP) @ 50 μA
- BREAKDOWN VOLTAGE - - LV_{CEO} = 18 VOLTS (MIN)

PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-106) outline



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram Package
is electrically non-conductive material

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures		
	Operating Junction Temperature	125°C Maximum
	Storage Temperature	−55°C to +125°C
	Lead Temperature (Soldering, 10 second time limit)	260°C Maximum
Maximum Power Dissipation		
	Total Dissipation at 25°C Case Temperature (Note 2)	0.5 Watt
	at 25°C Ambient Temperature (Note 2)	0.2 Watt
Maximum Voltages and Current		
V_{CBO}	Collector to Base Voltage	20 Volts
V_{CEO}	Collector to Emitter Voltage (Note 3)	18 Volts
V_{EBO}	Emitter to Base Voltage	3.0 Volts

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
h_{FE}	DC Current Gain	60	220	1000		I_C = 1.0 mA	V_{CE} = 5.0 V
h_{FE}	DC Current Gain		50			I_C = 50 μA	V_{CE} = 10 V
h_{fe}	High Frequency Current Gain (f = 20 MHz)		1.3			I_C = 50 μA	V_{CE} = 5.0 V
h_{fe}	High Frequency Current Gain (f = 20 MHz)	2.0		20		I_C = 1.0 mA	V_{CE} = 5.0 V
NF	Narrow Band Noise Figure (f = 1.0 kHz)		1.5		dB	I_C = 30 μA PWR BW = 200 Hz	V_{CE} = 5.0 V R_S = 10 kΩ
V_{CE}(sat)	Collector Saturation Voltage			0.4	Volts	I_C = 1.0 mA	I_B = 0.1 mA
I_{CBO}	Collector Cutoff Current			50	nA	I_E = 0	V_{CB} = 15 V
I_{CBO}(65°C)	Collector Cutoff Current			5.0	μA	I_E = 0	V_{CB} = 15 V
C_{cb}	Collector-Base Capacitance			5.0	pF	I_E = 0	V_{CB} = 5.0 V
BV_{CBO}	Collector to Base Breakdown Voltage	20			Volts	I_C = 100 μA	I_E = 0
V_{CEO}(sust)	Collector to Emitter Sustaining Voltage (Notes 3 and 4)	18			Volts	I_C = 3.0 mA	I_B = 0
BV_{EBO}	Emitter to Base Breakdown Voltage	3.0			Volts	I_E = 10 μA	I_C = 0
V_{BE}(on)	Base to Emitter On Voltage			0.75	Volts	I_C = 100 μA	V_{CE} = 5.0 V
h_{fe}	Small Signal Current Gain (f = 1.0 kHz)	50		1100		I_C = 1.0 mA	V_{CE} = 5.0 V

*Planar is a patented Fairchild process.

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C); junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).

(3) Rating refers to a high-current point where collector to emitter voltage is lowest.

(4) Pulse Conditions: length = 300 μs; duty cycle = 1%.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

UNION CARBIDE

SEMICONDUCTOR

2N4416 · 2N4416A · 2N4417

N-CHANNEL FIELD EFFECT TRANSISTORS
FOR
VHF/UHF AMPLIFIER APPLICATIONS

Silicon planar epitaxial construction · high transconductance
low capacitance · low noise · specified for 400 MHz operation

MAXIMUM RATINGS

@ 25°C (UNLESS OTHERWISE NOTED)

	SYM.	2N4416	2N4416A	2N4417	Units
Drain to Gate Voltage	V_{DG}	30	35	30	V
Drain to Source Voltage	V_{DS}	30	35	30	V
Source to Gate Voltage	V_{SG}	30	35	30	V
Gate Current	I_G	10	10	10	mA
Total Device Dissipation at or Below Ambient Temperature Linear Derating Factor	P_D T_A	300 25 1.7	300 25 1.7	175 25 1.0	mW °C mW/°C
Total Device Dissipation at or Below Case Temperature Linear Derating Factor	P_D T_C	450 125 6.0	450 125 6.0	350 25 2.0	mW °C mW/°C
Storage Temperature	T_S	−65 to +200	−65 to +200	−65 to +200	°C
Lead Temperature for 10 Seconds		+300	+300	+300	°C

ELECTRICAL CHARACTERISTICS

@ 25°C (UNLESS OTHERWISE NOTED)

	SYM.	2N4416-2N4416A		2N4417		Units	CONDITIONS
		min.	max.	min.	max.		
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	−30, −35 †		−30		V	$I_G = -1\ \mu A$, $V_{DS} = 0$
Total Gate Leakage Current	I_{GSS}		−100		−100	pA	$V_{GS} = -20$ V, $V_{DS} = 0$
Total Gate Leakage Current (150°C)	I_{GSS}		−200		−200	nA	$V_{GS} = -20$ V, $V_{DS} = 0$ $T_A = +150$°C
Zero Gate Voltage Drain Current*	I_{DSS}	5.0	15	5.0	15	mA	$V_{DS} = 15$ V, $V_{GS} = 0$
Gate-Source Cutoff Voltage	$V_{GS(off)}$	−2.5	−6.0 ††		−6.0	V	$V_{DS} = 15$ V, $I_D = 1.0$ nA
Small-Signal, Common Source, Short Circuit, Forward Transadmittance*	$\lvert y_{fs} \rvert$	4500	7500	4500	7500	µmhos	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 kHz
Small-Signal, Common Source, Short Circuit, Output Admittance	$\lvert y_{os} \rvert$		50		50	µmhos	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 kHz
Small-Signal, Common-Source, Short-Circuit, Reverse Transfer Capacitance	C_{rss}		0.8		0.8	pF	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 MHz
Small-Signal, Common-Source, Short-Circuit Input Capacitance	C_{iss}		4.0		3.5	pF	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 MHz
Small-Signal, Common-Source, Short-Circuit Output Capacitance	C_{oss}		2.0		1.3	pF	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 MHz
Small-Signal, Common-Source, Short-Circuit Input Conductance	RE (y_{is})		1000		1000	µmhos	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 400 MHz
Small-Signal, Common-Source, Short-Circuit Input Susceptance	IM (y_{is})		10,000		10,000	µmhos	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 400 MHz
Small-Signal, Common-Source, Short-Circuit Input Conductance	RE (y_{is})		100		100	µmhos	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 100 MHz
Small-Signal, Common-Source, Short-Circuit Input Susceptance	IM (y_{is})		2500		2500	µmhos	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 100 MHz
Small-Signal, Common-Source, Short-Circuit Output Conductance	RE (y_{os})		100		100	µmhos	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 400 MHz

* Pulsed Measurement Required. PW ≈ 300 µsec, Duty Cycle ≦1.0%; † 2N4416 −30 V, 2N4416A −35 V. †† −2.5 V. Min. 2N4416A Only.

GENERAL INSTRUMENT
MTOS TRANSISTOR

PRELIMINARY
DECEMBER, 1968

MEM 562C

N-CHANNEL ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

cramer
CRAMER / DENVER
5465 EAST EVANS PL.
DENVER, COLORADO 80222

FEATURES
- 10^{13} ohms input resistance
- Normally off with zero gate voltage
- Square low transfer characteristics
- Low insertion loss
- Low input and output capacitance

APPLICATIONS
- Logic circuits
- Switches
- Choppers
- Multiplexers
- Audio/RF Amplifier, Oscillators
- Operational Amplifiers

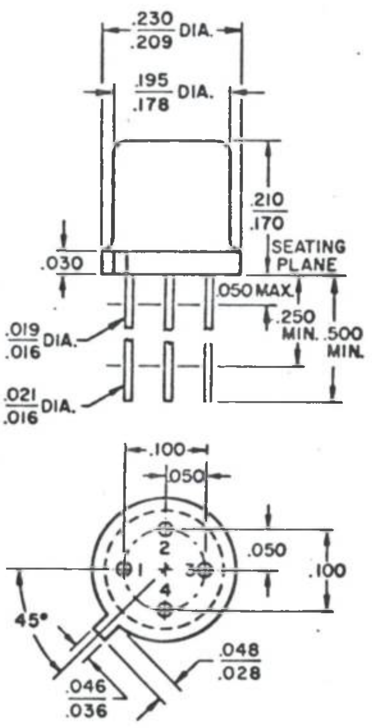
MAXIMUM RATINGS
(T_a = 25°C unless otherwise specified)

Drain to Source Voltage	+20 Volts
Gate to Source Voltage	±10 Volts
Gate to Drain Voltage	±30 Volts
Drain Current I_D	Limited by Dissipation
Storage Temperature	−50 to 125°C
Operating Junction Temperature	−50 to 100°C
Total Dissipation @ 25°C Ambient Temperature	175 mW
@ 25°C Case Temperature	500 mW

ELECTRICAL CHARACTERISTICS
(T_A = 25°C, unless otherwise specified)

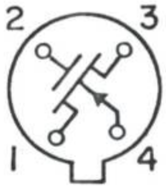
Symbol	Characteristic	Min	Typ	Max	Units	Conditions
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	0.50	1.5	4.0	V	$V_{DS} = V_{GS}$, $I_D = +10\mu A$
I_{DSS}	Drain Leakage Current	—	—	10	nA	$V_{DS} = +10V$, $V_{GS} = 0V$
I_{GSS}	Gate Leakage Current	—	—	100	pA	$V_{GS} = \pm 10V$, $V_{DS} = 0V$
BV_{DSS}	Drain Breakdown Voltage	20	—	—	V	$I_D \leq +10\mu A$, $V_{GS} = 0V$
$R_{DS(ON)}$	Drain-to-Source on Resistance	—	150	350	ohms	$V_{GS} = +10$, $I_D = 0.1mA$
$I_{D(ON)}$	Drain Current	5.0	15	—	mA	$V_{DS} = V_{GS} = +10V$
Y_{fs}	Forward Transadmittance	1000	—	—	μmhos	$V_{DS} = +10V$, $I_D = 2mA$, $f = 1kHz$
C_{iss}	Total Gate Input Capacitance	—	3.0	5.0	pF	$V_{GS} = 0V$, $V_{DS} = +10V$, $f = 1$ MHz
C_{oss}	Total Drain Output Capacitance	—	3.0	5.0	pF	$V_{GS} = 0V$, $V_{DS} = +10V$, $f = 1$ MHz
C_{gd}	Gate-to-Drain Capacitance	—	0.3	0.6	pF	$V_{GS} = 0V$, $V_{DS} = 0V$, $f = 1$ MHz
T_{D1}	Turn on Delay Time	—	—	55	nS	See Figure 1
T_r	Rise Time	—	—	75	nS	See Figure 1
$T_{(off)}$	Turnoff Time	—	—	170	nS	See Figure 1

TO-72



Bottom view
NOTE: All dimensions in inches

TERMINAL DIAGRAM



LEAD

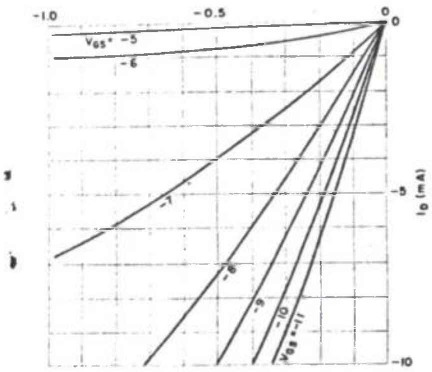
1. Source
2. Gate
3. Drain
4. Substrate, case

N-CHANNEL ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

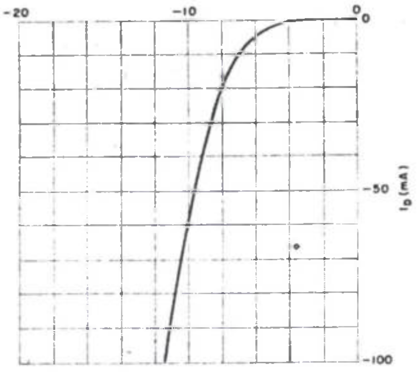
MEM 562 C

TYPICAL CHARACTERISTIC CURVES
MEM 517C

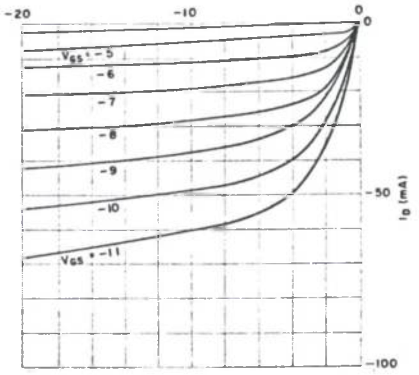
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



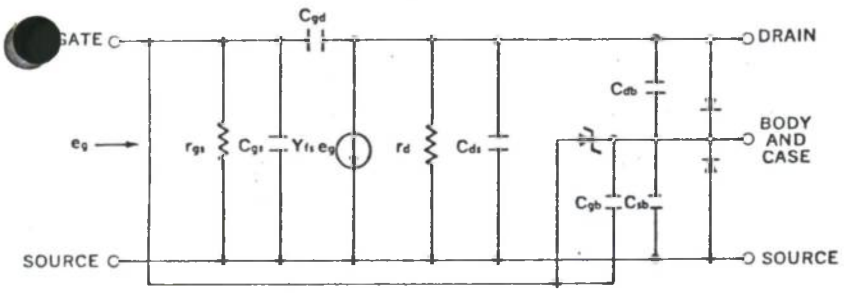
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)



SMALL SIGNAL EQUIVALENT CIRCUIT
(Conditions: $V_{GS} = V_{DS} = -10V$)
$I_D \approx 60mA$



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance and diode leakage resistance	10^{10}	ohms
r_d	Dynamic drain resistance	1.0	Kohms
C_{gs}	Gate to source capacitance	10	pF
C_{gd}	Gate to drain capacitance	10	pF
C_{ds}	Drain to source capacitance	0.15	pF
C_{gb}	Gate to body capacitance	6	pF
C_{db}	Drain to body capacitance	10	pF
C_{sb}	Source to body capacitance	20	pF
Y_{fs}	Forward transadmittance	12000	µmho

HANDLING PRECAUTIONS

MEM 517C insulated gate field effect transistors have been designed with an integrated zener diode which clamps the high internal resistance (10^{15} ohm typical) gate, to the body. This clamp eliminates the detrimental effects of high electrostatic voltages on the gate that can be generated in normal handling.

ENERAL INSTRUMENT CORPORATION
[illegible]

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GENERAL INSTRUMENT EUROPE S.p.A., Via Turati 28, Milan, Italy, Tel: 654475. Telex: GINEUR 31454

600 West John Street
Hicksville, L. I., N. Y. 11802
(516) OV 1-8000

GENERAL
INSTRUMENT

GENERAL INSTRUMENT POWER MTOS TRANSISTOR

P CHANNEL–ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

Technical Specifications
APRIL, 1968

MEM 517C

FEATURES:

- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law transfer characteristics

APPLICATIONS:

(Designed Primarily For Power Audio, Radio Frequency and Commutating Applications.)

- Audio output stages
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF power amplifiers
- Multiplexers

MAXIMUM RATINGS:

($T_A = 25°C$, unless otherwise specified)

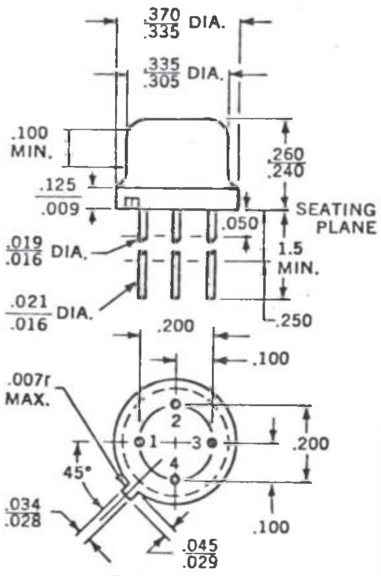
Drain to Source Voltage	−25V
Gate to Source Voltage	−25V
Gate to Drain Voltage	−25V
Drain Current	−250mA
Gate Current (Forward Direction for Zener Clamp)	+0.1mA
Storage Temperature	−50 to 125°C
Operating Junction Temperature	−50 to 100°C
Total Dissipation at 25°C Case Temperature	1.5 WATTS
Total Dissipation at 25°C Ambient Temperature	.45 WATT

ELECTRICAL CHARACTERISTICS:

($T_A = 25°C$, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{GST}	Gate Source Cutoff Voltage	−2.5		−5	Volts	$V_{GS} = V_{DS}$, $I_D = -10\mu A$
I_{DSS}	Drain Leakage Current			−50	nA	$V_{DS} = -20V$, $V_{GS} = 0V$
I_{GSS}	Gate Leakage Current			−1	nA	$V_{GS} = -15V$, $V_{DS} = 0V$
$I_{D(on)}$	Drain Current	−20	−50		mA	$V_{GS} = V_{DS} = -10V$
BV_{DSS}	Drain-Source Breakdown	−25	−40		Volts	$I_D = -10\mu A$, $V_{GS} = 0V$
BV_{GSS}	Gate to Source Breakdown	−25	−40		Volts	$I_{GS} = -10\mu A$, $V_{DS} = 0V$
Y_{fs}	Transadmittance		12000		µmho	1 kHz, $V_{GS} = V_{DS} = -10V$
C_{gs}	Gate to Source Capacitance		10	15	pF	$V_{GS} = V_{DS} = -10V$
C_{gd}	Gate to Drain Capacitance		10	15	pF	$V_{GS} = V_{DS} = -10V$
C_{ds}	Drain to Source Capacitance		0.15	0.2	pF	$V_{GS} = V_{DS} = -10V$
$r_{DS(on)}$	Drain to Source on Resistance		25	50	Ohms	$V_{GS} = -20V$, $I_{DS} = -10mA$
$r_{DS(on)}$	Drain to Source on Resistance		45	100	Ohms	$V_{GS} = -10V$, $I_{DS} = -10mA$

TO-33

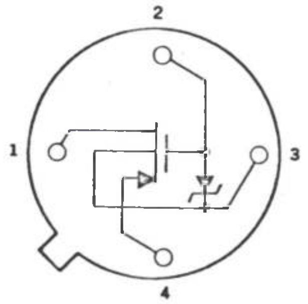


Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

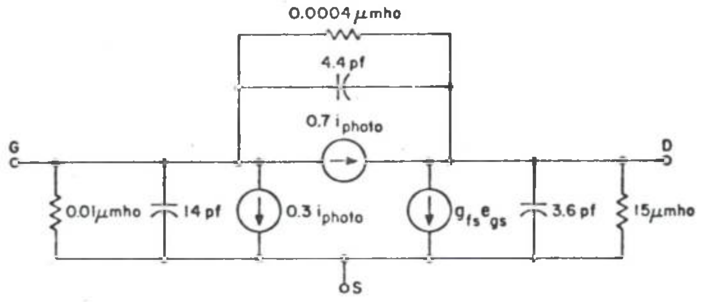
Lead
1. Drain
2. Gate
3. Body (Case)
4. Source



P CHANNEL–ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

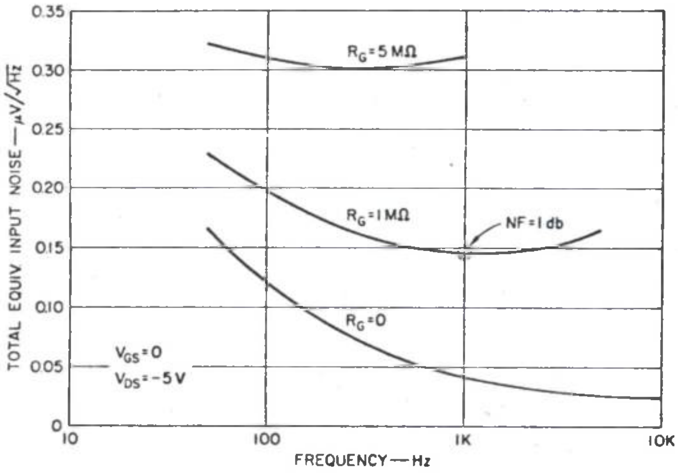
MEM 517C

SMALL SIGNAL EQUIVALENT CIRCUIT (25°C, f = 1 kHz, V_{DS} = -5 V, V_{GS} = 0)

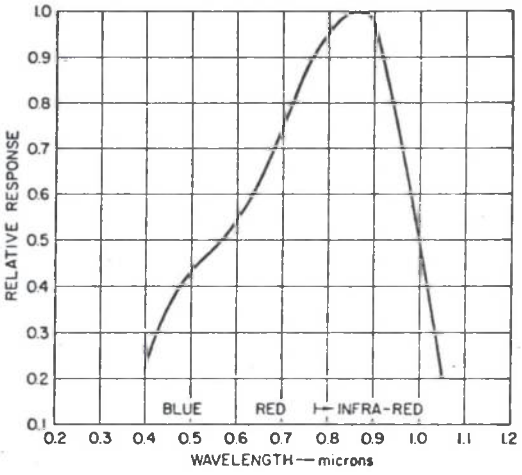


Photocurrent division above is 0.5:0.5 instead of 0.3:0.7 with positive gate bias larger than 0.5 volts.

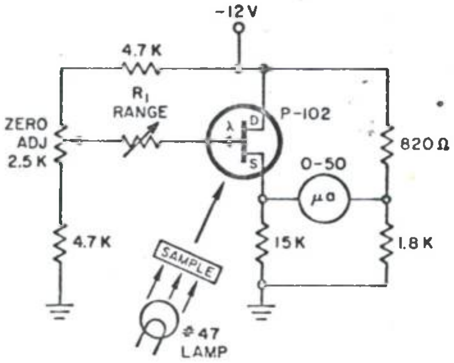
TYPICAL NOISE DATA



TYPICAL SPECTRAL RESPONSE



PHOTOMETER CIRCUIT



R_1 RANGE RESISTOR VALUE	FULL-SCALE OPTICAL DENSITY CALIBRATION
10K	0.0 (100% TRANSMISSION)
100 K	1.0 (10% TRANSMISSION)
1 meg	2.0 (1% TRANSMISSION)
10 meg	3.0 (0.1% TRANSMISSION)
100 meg	4.0 (0.01% TRANSMISSION)

Printed in USA

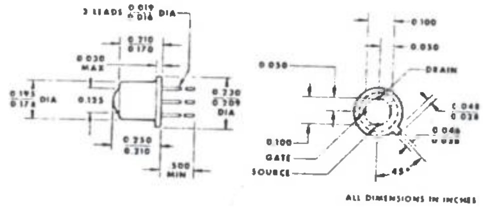
Test FETs
with
MONITOR II
Call us !

May 15, 1966

P-CHANNEL SILICON JUNCTION PHOTOSENSITIVE FIELD-EFFECT TRANSISTORS

FUNCTIONALLY INTEGRATED PHOTODIODE AND LOW-NOISE AMPLIFIER

- ○ High Input Sensitivity
- ○ Adjustable Threshold



JEDEC TO-18 with Top Lens
The gate is in electrical contact with the case

PRODUCT CONDITIONING

Units receive the following treatment before final electrical tests:

High Temperature Storage: 72 hrs at 150°C
Thermal Shock in Liquid +100 to 0°C for 5 cycles; 3 sec Max Transfer Time

35,000g Centrifuge in the Y_1 Plane
Helium and Gross Leak Tests for Hermeticity

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-drain or gate-source voltage (Note 1). .30 V
Total device dissipation at (or below) 25°C free-air temperature (Note 2) . . 300 mW
Storage temperature range . . . . -65 to +200°C

ELECTRICAL CHARACTERISTICS Equivalent to 2N2608 (25°C unless otherwise noted)

	Characteristic	Test Conditions	Min	Typ	Max	Unit
S_{IN}	Input Sensitivity (Gate Current per Unit Radiant Power Density)	$\lambda = 0.9$ microns $V_{GS} = 5$ V, $V_{DS} = 0$	0.4	1.2		$\mu A/mW/cm^2$
$D^\star$	Detectivity	$V_{GS} = 0$, $V_{DS} = -5$ V, $\lambda = 0.9$ microns f = 1 kHz, BW = 1 Hz, $R_G = 1$ MΩ	0.6	2.7		10^{10} $\frac{(cm)\ \sqrt{Hz}}{W}$
NF	Noise Figure (Note 3)	$V_{GS} = 0$, $V_{DS} = -5$ V, $f_o = 1$ kHz BW = 16%, $R_{gen} = 1$ MΩ		0.5	3.0	db
	Response Time 10% to 90% Points t_r t_f	Xenon Flash Source $R_G = 0$, $R_L = 330$ Ω $V_{GS} = 0$, $V_{DS} = -5$ V		0.1 1.5		μsec
I_{GSS}	Gate-Source Dark Current (Note 3)	$V_{GS} = 30$ V, $V_{DS} = 0$			10	nA
I_{GSS}	Gate-Source Dark Current (Note 3)	$V_{GS} = 5$ V, $V_{DS} = 0$, $T_A = 150°C$			10	μA
I_{DSS}	Drain Current at Zero Gate Voltage	$V_{GS} = 0$, $V_{DS} = -5$ V	-0.90	-1.60	-4.50	mA
V_P	Gate-Source Pinch-Off Voltage (Note 3)	$I_D = -1$ μA, $V_{DS} = -5$ V	1	2	4	V
g_{fs}	Common-Source Forward Transconductance	$V_{GS} = 0$, $V_{DS} = -5$ V, f = 1 kHz	1000	1600		μmho
C_{iss}	Common-Source Input Capacitance (Output Shorted)	$V_{GS} = 1$ V, $V_{DS} = -5$ V, f = 140 kHz		12	17	pF

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
Derate linearly to +175°C free-air temperature at the rate of 2 mW/C°.
3. Measured under dark conditions.

Refer to the 2N2606-9 series data sheet for typical characteristic curves on the 2N2608.

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0) MPS-U55 MPS-U56	BV_{CEO}	 60 80	 – –	 – –	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) MPS-U55 (V_{CB} = 60 Vdc, I_E = 0) MPS-U56	I_{CBO}	 – –	 – –	 100 100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc) (I_C = 250 mAdc, V_{CE} = 1.0 Vdc) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc) (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	 100 – 50 –	 180 100 140 90	 – – – –	–
Collector-Emitter Saturation Voltage (I_C = 250 mAdc, I_B = 10 mAdc) (I_C = 250 mAdc, I_B = 25 mAdc)	$V_{CE(sat)}$	 – –	 0.3 0.15	 0.6 –	Vdc
Base-Emitter Saturation Voltage (I_C = 250 mAdc, I_B = 25 mAdc)	$V_{BE(sat)}$	–	0.86	–	Vdc
Base-Emitter On Voltage (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	0.78	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain–Bandwidth Product (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	50	125	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	8.5	12	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{ib}	–	20	–	pF

FIGURE 1 – TYPICAL DC CURRENT GAIN

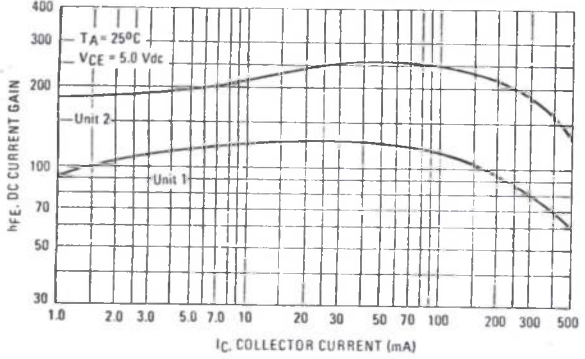


FIGURE 2 – "SATURATION" AND "ON" VOLTAGES

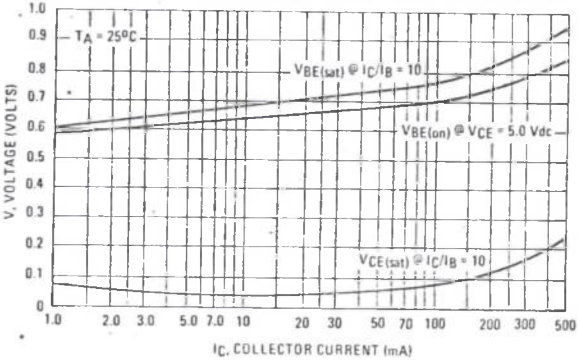
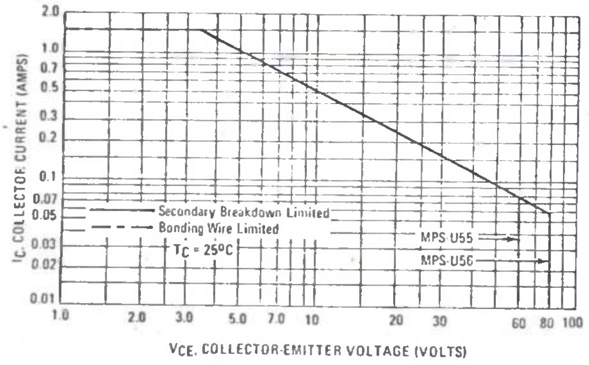


FIGURE 3 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 135^{\circ}C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

SPECIFICATION

2N5484
thru
2N5486

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

N-CHANNEL
JUNCTION FIELD-EFFECT
TRANSISTORS
(Type A)

AUGUST 1968 – PS 101

Depletion mode (Type A) Junction Field-Effect Transistors designed for VHF/UHF amplifier applications.

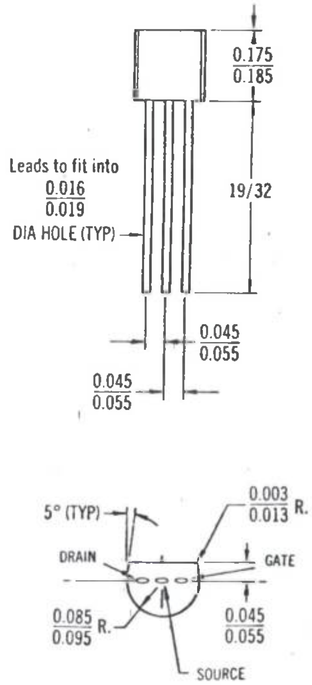
- Low Noise Figure –
  NF = 2.0 dB (Max) @ f = 100 MHz (2N5485, 2N5486)
  = 4.0 dB (Typ) @ f = 100 MHz (2N5484)
  = 4.0 dB (Max) @ f = 400 MHz (2N5485, 2N5486)
- Low Input Capacitance – C_{iss} = 5.0 pF (Max)
- Low Output Capacitance – C_{oss} = 2.0 pF (Max)
- Low Transfer Reverse Capacitance – C_{rss} = 1.0 pF (Max)
- High Power Gain –
  G_{ps} = 18 dB (Min) @ f = 100 MHz (2N5485, 2N5486)
  = 14 dB (Typ) @ f = 200 MHz (2N5484)
  = 10 dB (Min) @ f = 400 MHz (2N5485, 2N5486)
- High $|y_{fs}|/C_{iss}$ Ratio (High Frequency Figure of Merit)
- High Maximum Stable Gain Due to Drain and Gate Lead Separation

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	25	Vdc
Drain Current	I_D	30	mAdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	310 2.82	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = -1.0 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	-25	-	-	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5484 2N5485 2N5486	$V_{GS(off)}$	-0.3 -0.5 -2.0	- - -	-3.0 -4.0 -6.0	Vdc
Gate Reverse Current (V_{GS} = -20 Vdc, V_{DS} = 0) (V_{GS} = -20 Vdc, V_{DS} = 0, T_A = 100°C)		I_{GSS}	- -	- -	-1.0 -0.2	nAdc μAdc
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5484 2N5485 2N5486	I_{DSS}	1.0 4.0 8.0	- - -	5.0 10 20	mAdc



TO-92
CASE 29 (5)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	2N5460, 2N5461, 2N5462	$V_{(BR)GSS}$	40	-	-	Vdc
	2N5463, 2N5464, 2N5465		60	-	-	
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 1.0 μAdc)	2N5460, 2N5463	$V_{GS(off)}$	0.75	-	6.0	Vdc
	2N5461, 2N5464		1.0	-	7.5	
	2N5462, 2N5465		1.8	-	9.0	
Gate Reverse Current (V_{GS} = 20 Vdc, V_{DS} = 0)	2N5460, 2N5461, 2N5462	I_{GSS}	-	-	5.0	nAdc
(V_{GS} = 30 Vdc, V_{DS} = 0)	2N5463, 2N5464, 2N5465		-	-	5.0	
(V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 100°C)	2N5460, 2N5461, 2N5462		-	-	1.0	μAdc
(V_{GS} = 30 Vdc, V_{DS} = 0, T_A = 100°C)	2N5463, 2N5464, 2N5465		-	-	1.0	
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5460, 2N5463	I_{DSS}	1.0	-	5.0	mAdc
	2N5461, 2N5464		2.0	-	9.0	
	2N5462, 2N5465		4.0	-	16	
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 0.1 mAdc)	2N5460, 2N5463	V_{GS}	0.5	-	4.0	Vdc
(V_{DS} = 15 Vdc, I_D = 0.2 mAdc)	2N5461, 2N5464		0.8	-	4.5	
(V_{DS} = 15 Vdc, I_D = 0.4 mAdc)	2N5462, 2N5465		1.5	-	6.0	
SMALL-SIGNAL CHARACTERISTICS						
Forward Transadmittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5460, 2N5463	$\lvert y_{fs} \rvert$	1000	-	4000	μmhos
	2N5461, 2N5464		1500	-	5000	
	2N5462, 2N5465		2000	-	6000	
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\lvert y_{os} \rvert$	-	-	75	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	-	5.0	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	-	1.0	2.0	pF
Common-Source Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1.0 Megohm, f = 100 Hz, BW = 1.0 Hz)		NF	-	1.0	2.5	dB
Equivalent Short-Circuit Input Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 Hz, BW = 1.0 Hz)		e_n	-	60	115	nV/√Hz

DRAIN CURRENT versus GATE SOURCE VOLTAGE

FIGURE 1 – 2N5460 and 2N5463

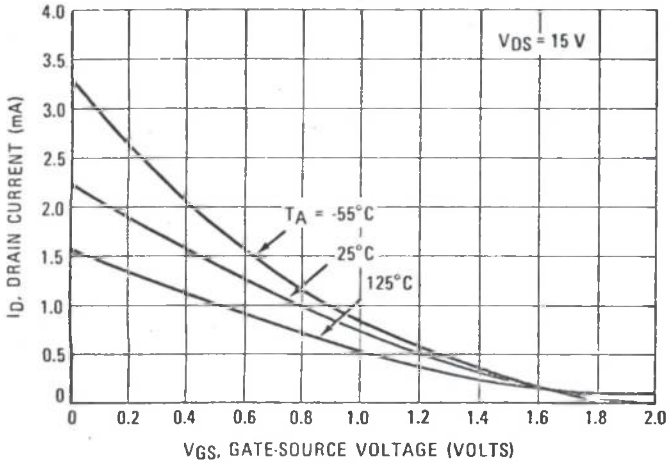


FIGURE 2 – 2N5461 and 2N5464

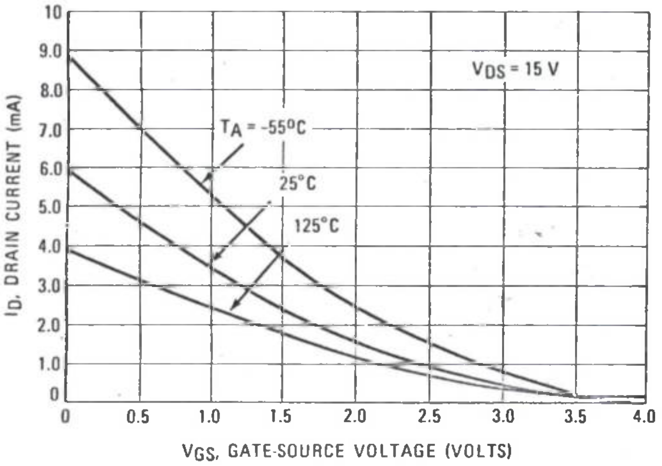
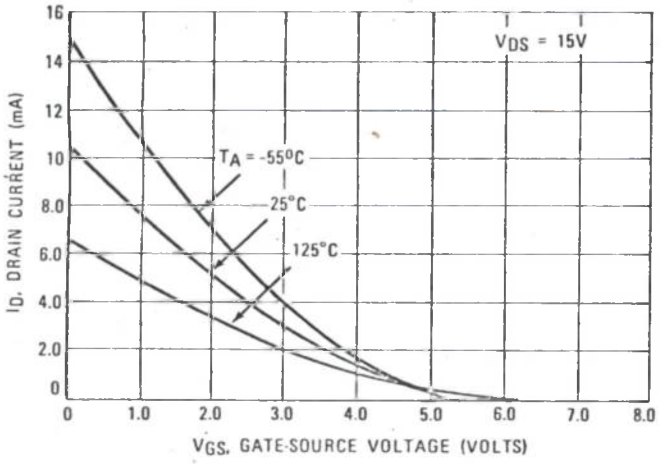


FIGURE 3 – 2N5462 and 2N5465



FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

FIGURE 4 – 2N5460 and 2N5463

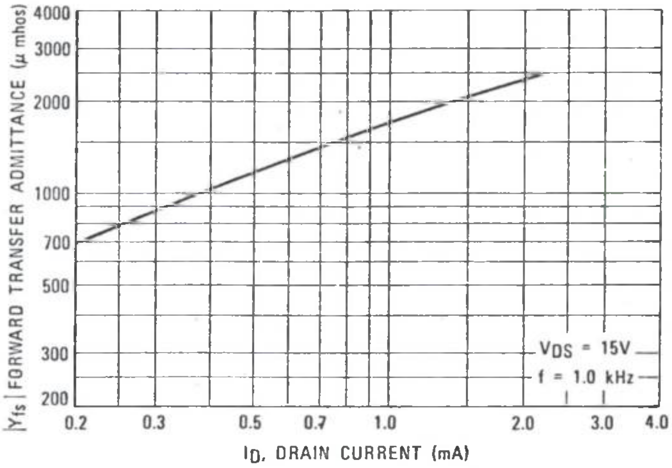


FIGURE 5 – 2N5461 and 2N5464

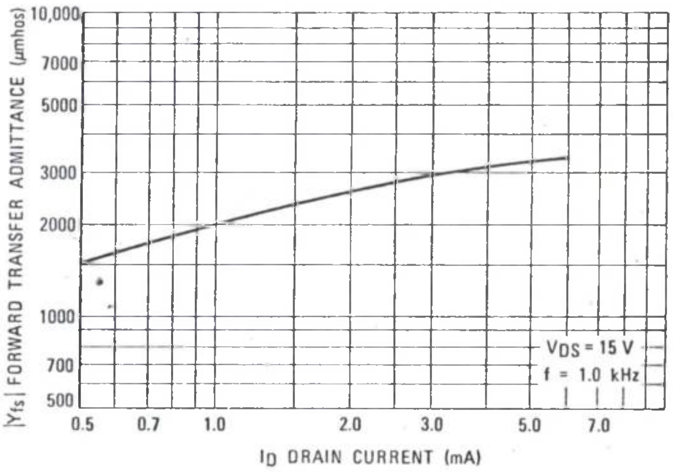


FIGURE 6 – 2N5462 and 2N5465

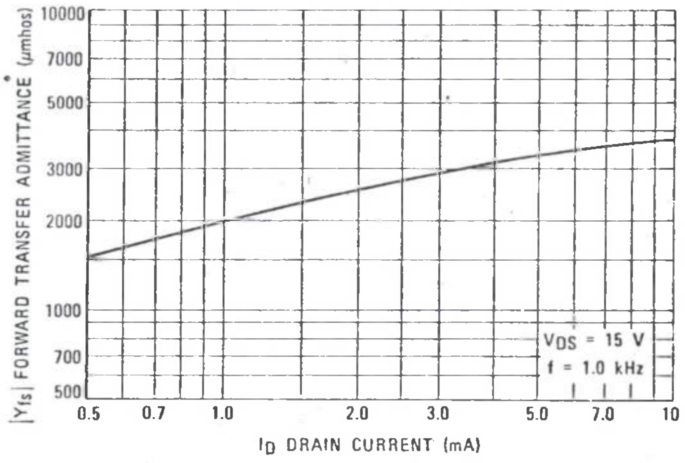


FIGURE 7 – OUTPUT RESISTANCE VERSUS DRAIN CURRENT

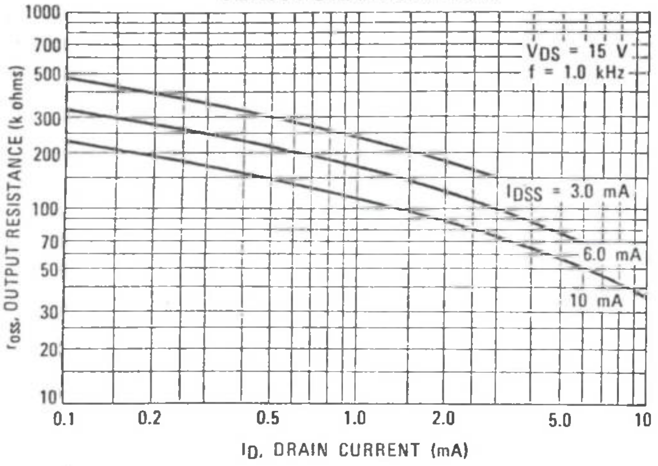


FIGURE 8 – CAPACITANCE VERSUS DRAIN-SOURCE VOLTAGE

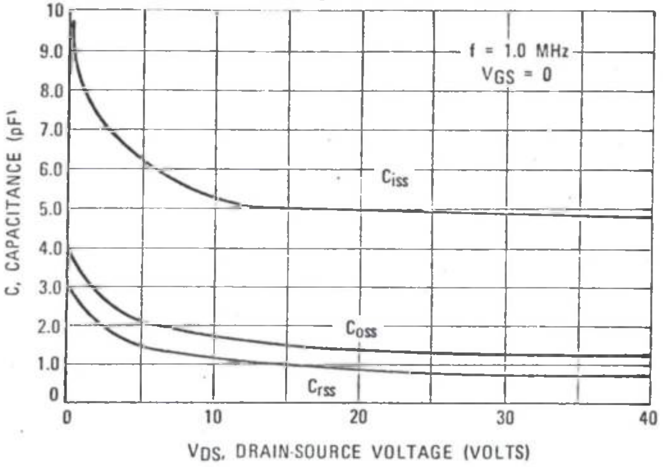


FIGURE 9 – NOISE FIGURE VERSUS FREQUENCY

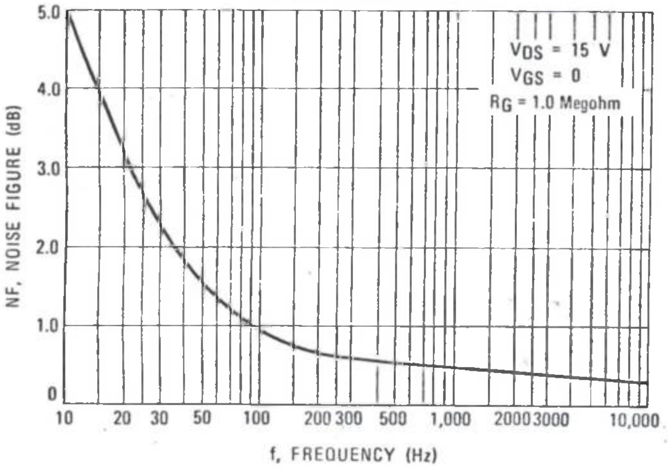


FIGURE 10 – NOISE FIGURE VERSUS SOURCE RESISTANCE

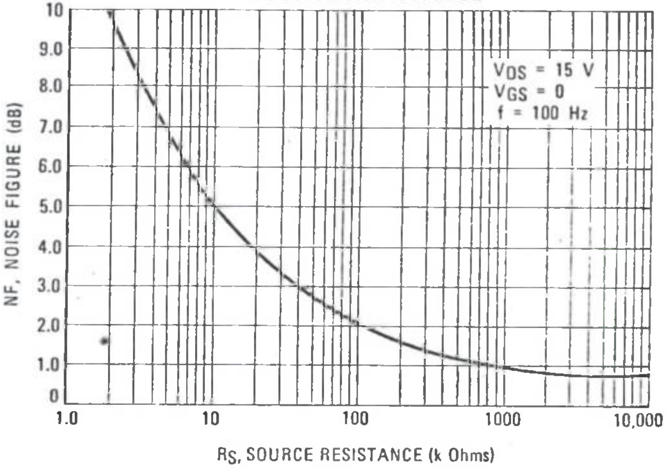
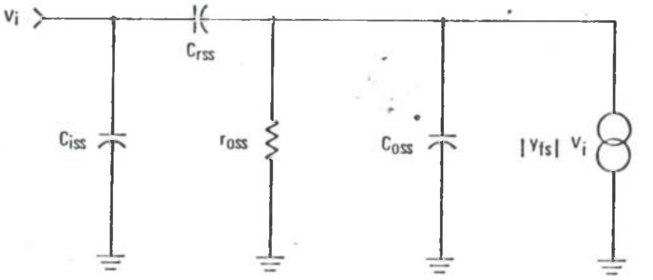


FIGURE 11 – EQUIVALENT LOW FREQUENCY CIRCUIT



Common Source
y Parameters for Frequencies
Below 30 MHz

$y_{is} = j\omega C_{iss}$

$y_{os} = j\omega C_{osp}{}^{*} + 1/r_{oss}$

$y_{fs} = y_{fs}\,|$

$y_{rs} = -j\omega C_{rss}$

*C_{osp} is C_{oss} in parallel with Series Combination of C_{iss} and C_{rss}.

NOTE:

1. Graphical data is presented for dc conditions. Tabular data is given for pulsed conditions (Pulse Width = 630 ms, Duty Cycle = 10%).

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2N5460,2,4
thru
2N5465

P-CHANNEL
JUNCTION
FIELD-EFFECT
TRANSISTORS

TYPE A

OCTOBER 1968 – DS 5279 R1
(Replaces DS 5279)

DS 5279 R1

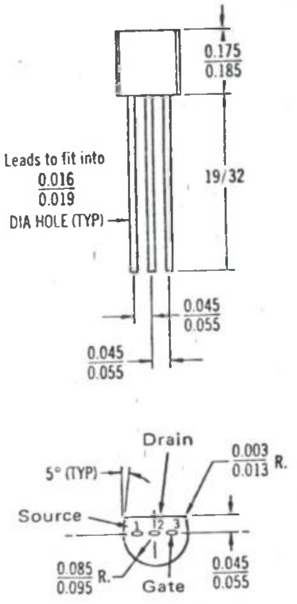
P-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

. . . depletion mode (Type A) Junction Field-Effect Transistors designed for use in general-purpose amplifier applications.

- High Gate-Source Breakdown Voltage – $V_{(BR)GSS}$ = 60 Vdc (Min) - 2N5463 thru 2N5465
- Low Noise Figure – NF = 2.5 dB (Max) @ f = 100 Hz - All Types
- Low Reverse Transfer Capacitance – C_{rss} = 2.0 pF (Max) - All Types
- Interchangeable Drain and Source Terminals

MAXIMUM RATINGS

Rating	Symbol	2N5460 2N5461 2N5462	2N5463 2N5464 2N5465	Unit
Drain-Gate Voltage	V_{DG}	40	60	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	40	60	Vdc
Forward Gate Current	$I_{G(f)}$	10		mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.82		mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +150		°C
Operating Junction Temperature Range	T_J	-65 to +135		°C



Case 29 (7)
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = -10μAdc, V_{DS} = 0)		BV_{GSS}	-25	—	—	Vdc
Gate Reverse Current (V_{GS} = -15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	-1.0	nAdc
(V_{GS} = -15 Vdc, V_{DS} = 0, T_A = 100°C)			—	—	-200	
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5457	$V_{GS(off)}$	-0.5	—	-6.0	Vdc
	2N5458		-1.0	—	-7.0	
	2N5459		-2.0	—	-8.0	
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 100 μAdc)	2N5457	V_{GS}	—	-2.5	—	Vdc
(V_{DS} = 15 Vdc, I_D = 200 μAdc)	2N5458		—	-3.5	—	
(V_{DS} = 15 Vdc, I_D = 400 μAdc)	2N5459		—	-4.5	—	
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current* (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5457	I_{DSS}*	1.0	3.0	5.0	mAdc
	2N5458		2.0	6.0	9.0	
	2N5459		4.0	9.0	16	
DYNAMIC CHARACTERISTICS						
Forward Transfer Admittance* (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz)	2N5457	$\lvert y_{fs} \rvert$*	1000	3000	5000	μmhos
	2N5458		1500	4000	5500	
	2N5459		2000	4500	6000	
Output Admittance* (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz)		$\lvert y_{os} \rvert$*	—	10	50	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz)		C_{iss}	—	4.5	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz)		C_{rss}	—	1.5	3.0	pF

*Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%

1948-4 PRINTED IN USA 6-68 IMPERIAL LITHO 96549 30M
CODE 6.2.1-2 12 6.2.1-2 DS 5207 R1

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

2N5457
2N5458
2N5459

JUNCTION FIELD-EFFECT TRANSISTORS

SYMMETRICAL
SILICON
N-CHANNEL

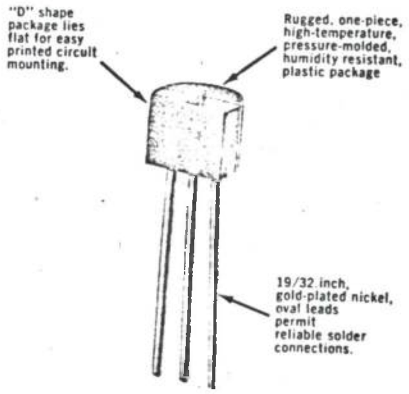
JULY 1968 – DS 5207 R2
(Replaces DS 5207 R1)

Type A

SILICON N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

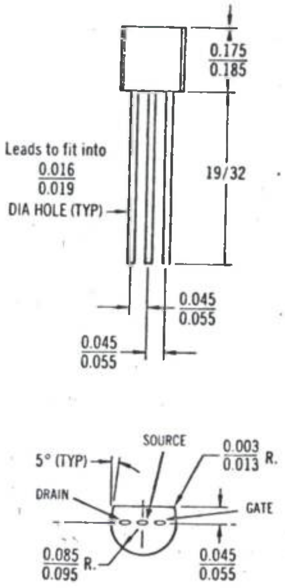
. . . depletion mode (Type A) transistors designed for general-purpose audio and switching applications.

- N-Channel for Higher Gain
- Drain and Source Interchangeable
- High AC Input Impedance
- High DC Input Resistance
- Low Transfer and Input Capacitance
- Low Cross-Modulation and Intermodulation Distortion
- Unibloc* Plastic Encapsulated Package


"D" shape package lies flat for easy printed circuit mounting.
Rugged, one-piece, high-temperature, pressure-molded, humidity resistant, plastic package
19/32 inch, gold-plated nickel, oval leads permit reliable solder connections.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	-25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	310 2.82	mW mW/°C
Operating Junction Temperature	T_J	135	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



BOTTOM VIEW

TO-92
CASE 29(5)

Drain and Source may be Interchanged.

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*Trademark of Motorola Inc.

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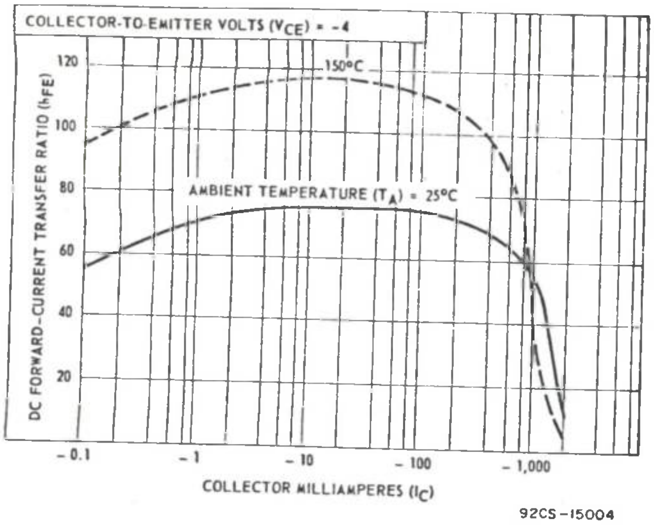


Fig.7 - Typical static beta characteristics for types 2N5322 and 2N5323.

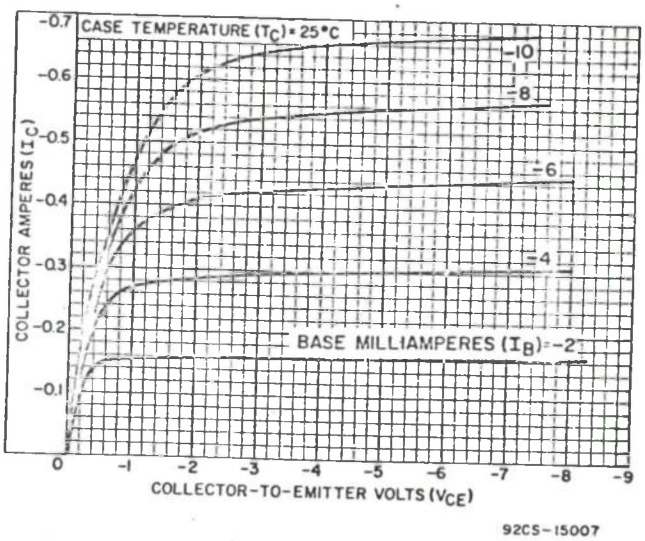


Fig.8 - Typical output characteristics for types 2N5322 and 2N5323.

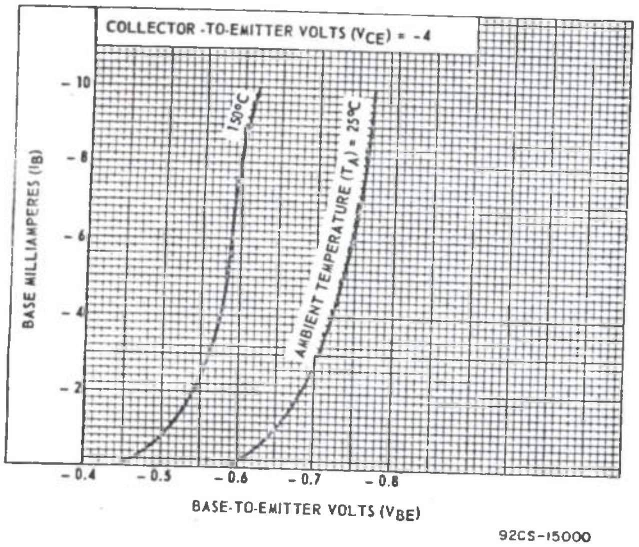


Fig.9 - Typical input characteristics for types 2N5322 and 2N5323.

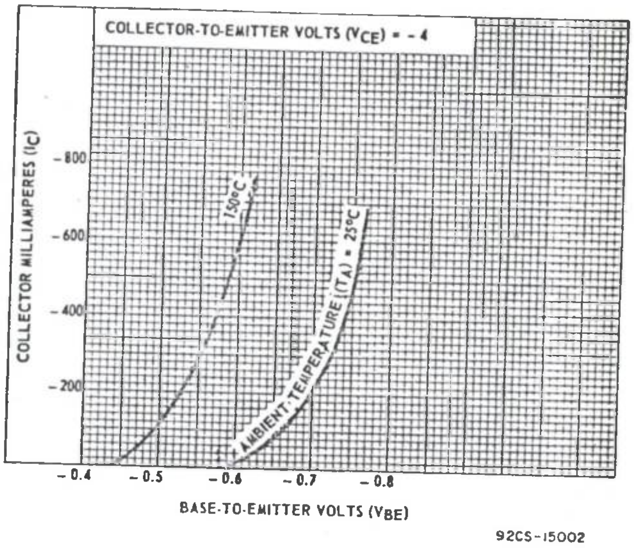
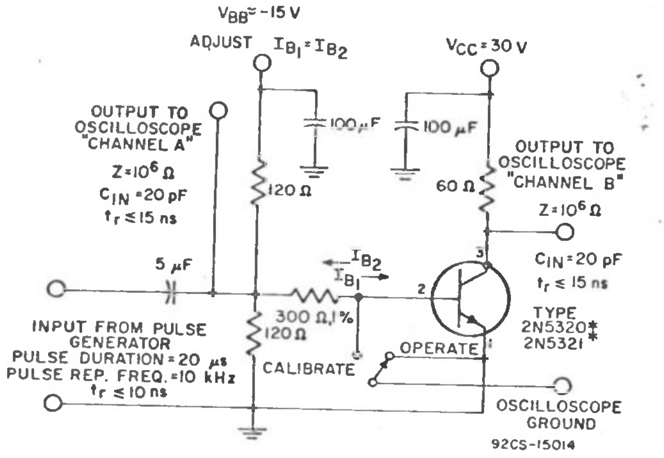


Fig.10 - Typical transfer characteristics for types 2N5322 and 2N5323.

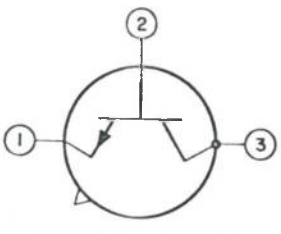


* For 2N5322 or 2N5323, reverse direction of I_{B1} and I_{B2} and reverse polarity of V_{BB} and V_{CC}.

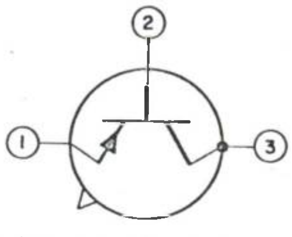
Fig.11 - Circuit used to measure switching times for types 2N5320, 2N5321, 2N5322 and 2N5323.

TERMINAL DIAGRAMS
(Bottom Views)

2N5320 and 2N5321



2N5322 and 2N5323



LEAD 1 - EMITTER
LEAD 2 - BASE
LEAD 3 - COLLECTOR, CASE

DIMENSIONAL OUTLINE

Types 2N5320–2N5323 employ the JEDEC TO-5 package. The dimensional outline for this package is shown in the RCA SEMICONDUCTOR PRODUCTS DATABOOK (Form No.SPD-100) and in the RCA TRANSISTOR MANUAL (Technical Series SC-13). Also copies of this dimensional outline can be obtained from RCA, Commercial Engineering, Harrison, N.J., 07029.

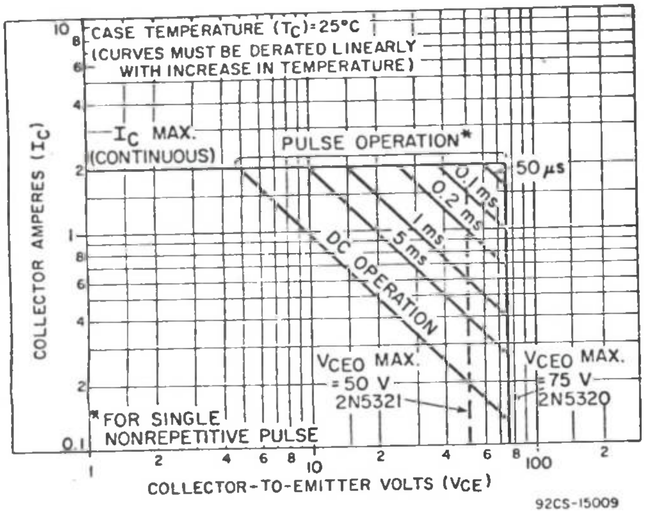


Fig.1 - Maximum operating areas for types 2N5320 and 2N5321.

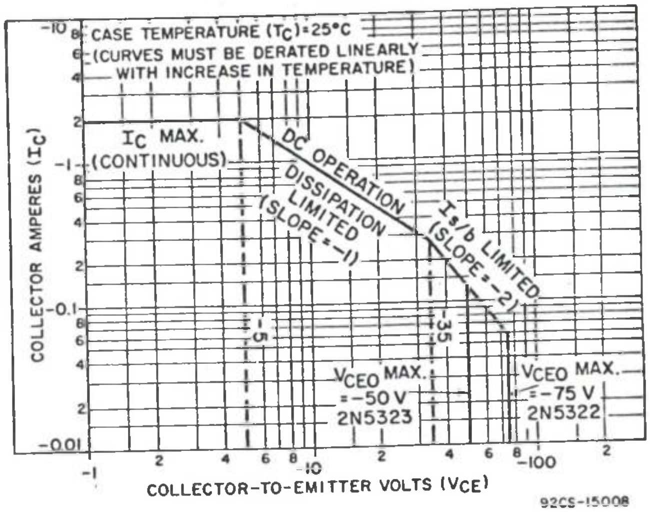


Fig.2 - Maximum operating areas for types 2N5322 and 2N5323.

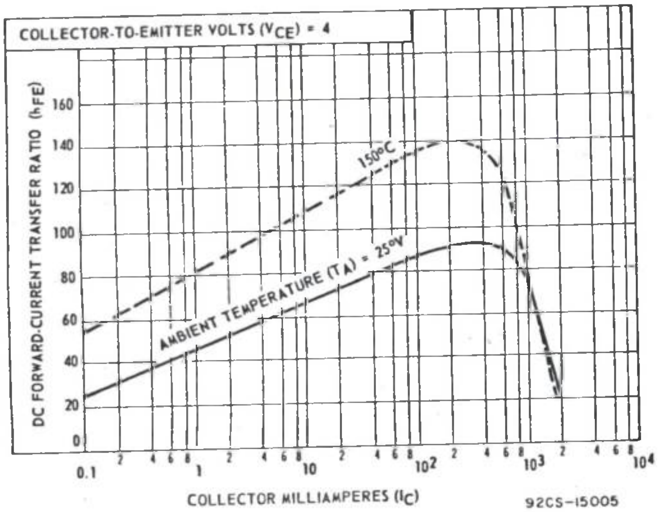


Fig.3 - Typical static beta characteristics for types 2N5320 and 2N5321.

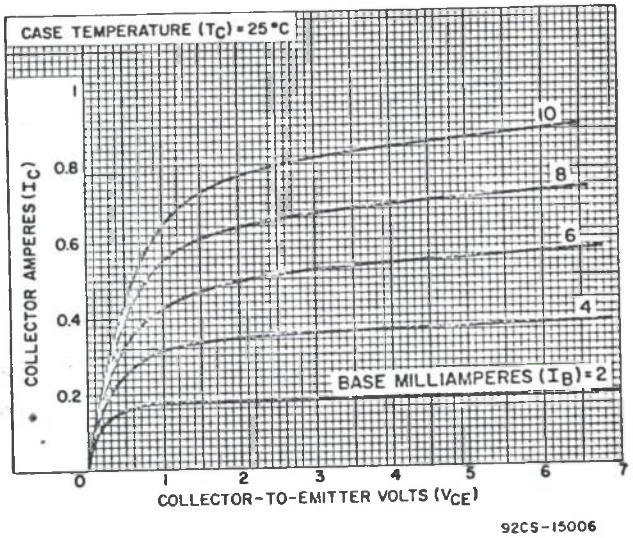


Fig.4 - Typical output characteristics for types 2N5320 and 2N5321.

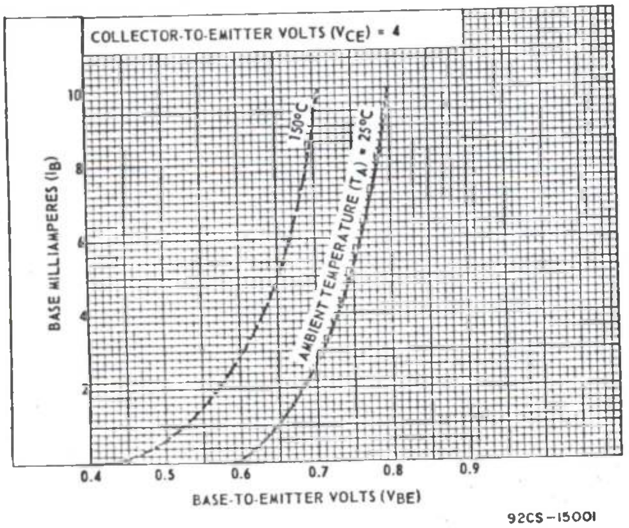


Fig.5 - Typical input characteristics for types 2N5320 and 2N5321.

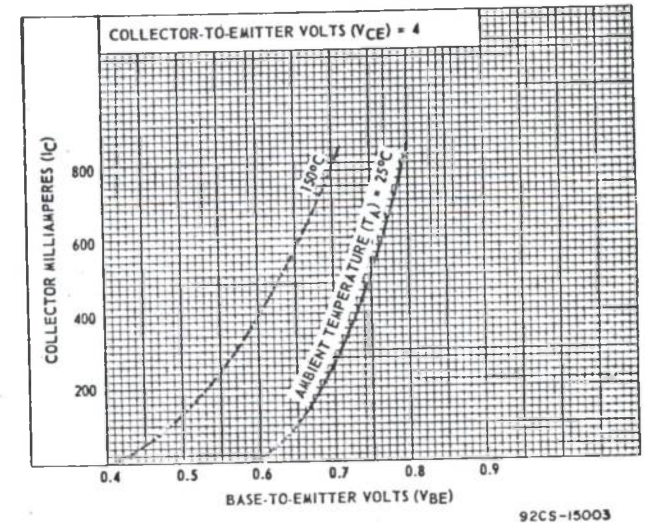


Fig.6 - Typical transfer characteristics for types 2N5320 and 2N5321.

ELECTRICAL CHARACTERISTICS, *Case Temperature* (T_C) = 25°C	Symbol	TEST CONDITIONS							LIMITS								Units
		DC Collector Volts		DC Emitter or Base Volts		DC Current Milliamperes			Type 2N5320		Type 2N5321		Type 2N5322		Type 2N5323		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Collector-Cutoff Current	I_{CBO}	80 60 -80 -60					0 0 0 0		- - - -	0.5 - - -	- - - -	- 5 - -	- - - -	- - -0.5 -	- - - -	- - - -5	µA
Emitter-Cutoff Current	I_{EBO}			5 4 -5 -4		0 0 0 0			- - - -	0.1 - - -	- - - -	- 0.5 - -	- - - -	- - -0.1 -	- - - -	- - - -0.5	µA
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$					0 0	0.1 -0.1		7 -	- -	5 -	- -	- -7	- -	- -5	- -	V
Collector-to-Emitter Breakdown Voltage: With base-emitter junction reverse biased	$V_{(BR)CEV}$				-1.5 1.5	0.1 -0.1			100 -	- -	75 -	- -	- -100	- -	- -75	- -	V
Collector-to-Emitter Sustaining Voltage: With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER(sus)}$[a]					100 -100			90 -	- -	65 -	- -	- -90	- -	- -65	- -	V
With base open	$V_{CEO(sus)}$[a]					100 -100		0 0	75 -	- -	50 -	- -	- -75	- -	- -50	- -	V
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$					500 -500		50 -50	- -	0.5 -	- -	0.8 -	- -	- -0.7	- -	- -1.2	V
Base-to-Emitter Voltage	V_{BE}		4 -4			500 -500			- -	1.1 -	- -	1.4 -	- -	- -1.1	- -	- -1.4	V
DC Forward Current Transfer Ratio	h_{FE}[b] See NOTE		4 -4 2 -2			500 -500 1000 -1000			30 - 10 -	130 - - -	40 - - -	250 - - -	- 30 - 10	- 130 - -	- 40 - -	- 250 - -	
Gain-Bandwidth Product	f_T		4 -4			50 -50			50 -	- -	50 -	- -	- 50	- -	- 50	- -	MHz
Second Breakdown Collector Current[c,e] (With base forward biased)	$I_{S/b}$[d]		50 -35						200 -	- -	200 -	- -	- -285	- -	- -285	- -	mA
Sat. Switching Time: *(See Fig.11.)* Turn-on Time	t_{on}		30 -30			500 -500		50 -50	- -	80 -	- -	80 -	- -	- 100	- -	- 100	ns
Turn-off Time	t_{off}		30 -30			500 -500		50 -50	- -	800 -	- -	800 -	- -	- 1000	- -	- 1000	ns
Thermal Resistance: Junction-to-Case	$\theta_{J\text{-}C}$								-	17.5	-	17.5	-	17.5	-	17.5	°C/W
Junction-to-Ambient	$\theta_{J\text{-}A}$								-	150	-	150	-	150	-	150	°C/W

[a] CAUTION: The sustaining voltages $V_{CEO(sus)}$ and $V_{CER(sus)}$ MUST NOT be measured on a curve tracer.

[b] Pulsed; pulse duration ≤ 300 µs, duty factor ≤ 0.02.

[c] Safe operating regions for forward-bias operation are shown on page 3.

[d] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward biased for transistor operation in the active region.

[e] Pulsed; 1 s, non-repetitive pulse.

NOTE: RCA 2N5320, 2N5321, 2N5322, and 2N5323 can be shipped with color dots on the device case to indicate the following ranges of beta values within the beta limits specified for each device.

Color Code	Beta Range	Color Code	Beta Range
Brown	25-38	Green	73-110
Red	33-50	Blue	95-145
Orange	43-65	Violet	125-190
Yellow	56-85	Grey	165-250

Specific beta distributions or beta matching are available as custom types only on special order. For further details, contact your local RCA Sales office.

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RCA POWER TRANSISTORS

2N5320 2N5321
2N5322 2N5323

File No. 325

SILICON POWER TRANSISTORS

General-Purpose Complementary N-P-N and P-N-P Types

For Small-Signal Medium-Power Applications In Military, Industrial, and Commercial Equipment

RCA-2N5320, 2N5321, 2N5322, and 2N5323* are multiple-diffused silicon power transistors intended for small-signal medium-power applications in military, industrial, and commercial equipment.

The 2N5320 and 2N5321 are triple-diffused silicon n-p-n planar types which differ in voltage ratings, leakage-current and beta-spread values. They have all of the desirable features of the 2N2102 silicon n-p-n type and, in addition, higher collector-current and dissipation ratings.

The 2N5322 and 2N5323, p-n-p complements of the 2N5320 and 2N5321, are double-diffused, epitaxial-planar types which differ in voltage ratings, leakage-current and beta-spread values. They have all of the desirable features of the 2N4036 (p-n-p complement of 2N2102) and, in addition, higher current and higher power ratings.

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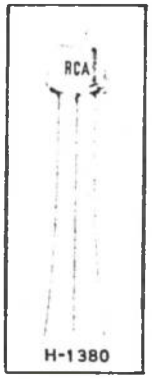
* Formerly RCA Dev. Types TA7121, TA7122, TA7124 and TA7125, respectively.



JEDEC TO-5

N-P-N Types	P-N-P Types
2N5320	2N5322
2N5321	2N5323

FEATURES

- Maximum safe area-of-operation curves
- Planar construction provides low-noise and low-leakage characteristics
- Low saturation voltage:
  $V_{CE}(sat)$ = 0.5 V max. (2N5320)
  -0.7 V max. (2N5322)
- High beta at high collector current:
  h_{FE} = 40 min. at I_C = 500 mA (2N5321 & 2N5323)
- High saturated switching speed:
  t_{on} = 80 ns max.
  t_{off} = 800 ns max. } (2N5320 & 2N5321)
- Hermetically sealed JEDEC TO-5 package

MAXIMUM RATINGS, *Absolute-Maximum Values:*		2N5321	2N5323	2N5320	2N5322	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	75	-75	100	-100	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:						
With 1.5 volts (V_{BE}) of reverse bias	V_{CEV}(sus)	75	-75	100	-100	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}(sus)	65	-65	90	-90	V
With base open	V_{CEO}(sus)	50	-50	75	-75	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	-5	7	-7	V
COLLECTOR CURRENT	I_C	2	-2	2	-2	A
BASE CURRENT	I_B	1	-1	1	-1	A
TRANSISTOR DISSIPATION:	P_T	10	10	10	10	W
At case temperatures up to 25°C		See Fig.1				
At case temperatures above 25°C		Derate linearly at 0.057 W/°C				
TEMPERATURE RANGE:						
Storage and operating (Junction)		-65 to +200				°C
LEAD TEMPERATURE (During soldering):						
At distance ≥ 1/32 in. (3.17 mm) from seating plane for 10 s max.		230				°C

RCA Electronic Components

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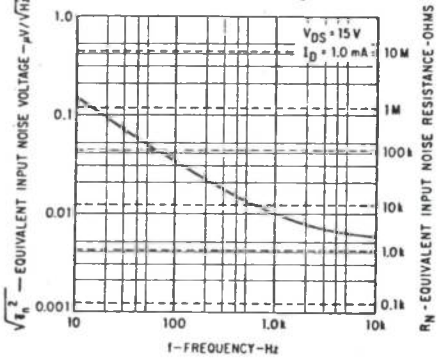
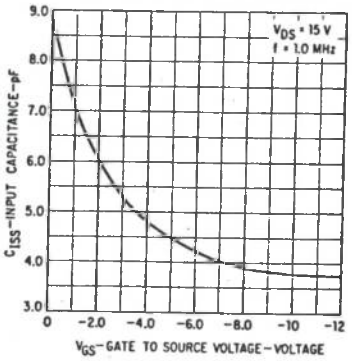
TYPICAL ELECTRICAL CHARACTERISTICS

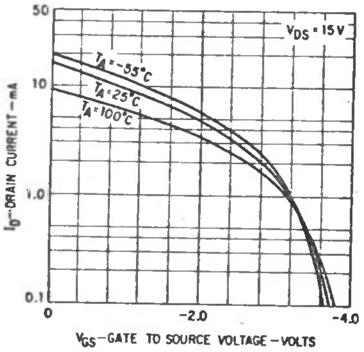
EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



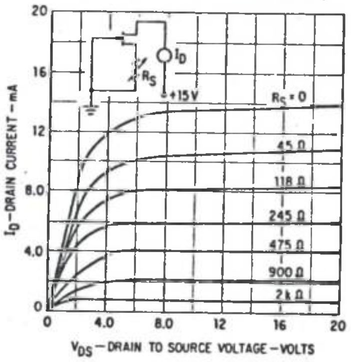
INPUT CAPACITANCE VERSUS GATE TO SOURCE VOLTAGE



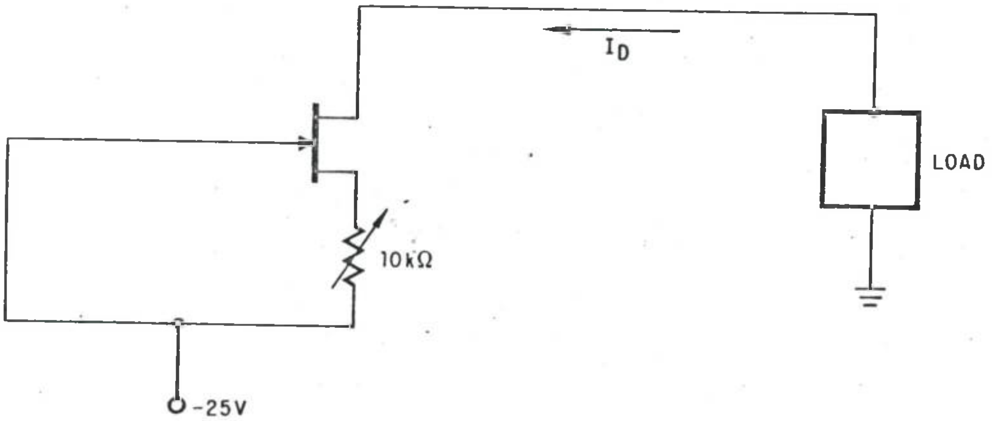
DRAIN CURRENT VERSUS GATE TO SOURCE VOLTAGE



DRAIN CURRENT VERSUS DRAIN TO SOURCE VOLTAGE WITH SOURCE RESISTANCE



CONSTANT CURRENT SOURCE



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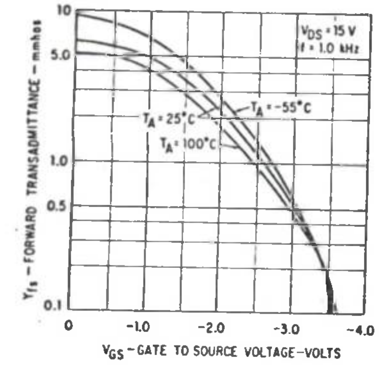
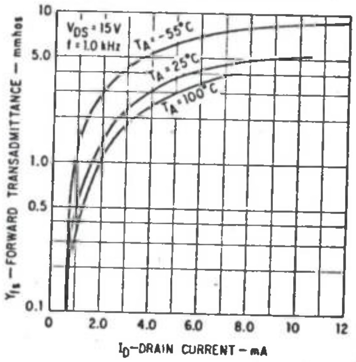
FAIRCHILD TRANSISTOR 2N5163

TYPICAL ELECTRICAL CHARACTERISTICS

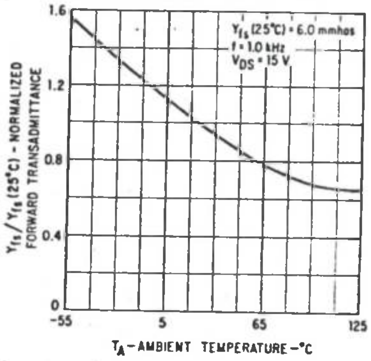
FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



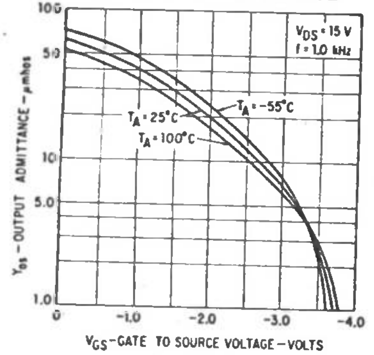
FORWARD TRANSADMITTANCE VERSUS DRAIN CURRENT



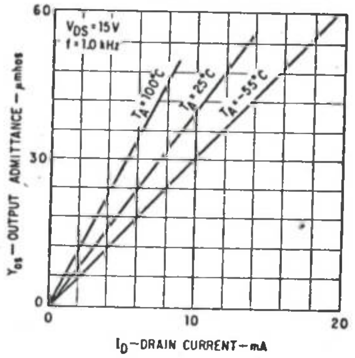
NORMALIZED FORWARD TRANSADMITTANCE VERSUS AMBIENT TEMPERATURE



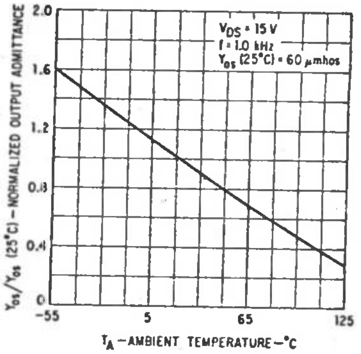
OUTPUT ADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



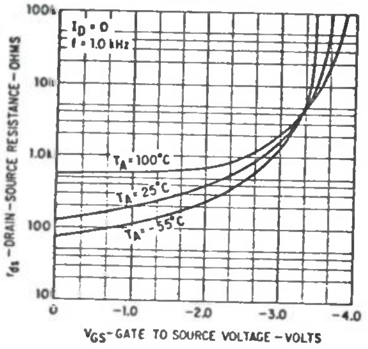
OUTPUT ADMITTANCE VERSUS DRAIN CURRENT



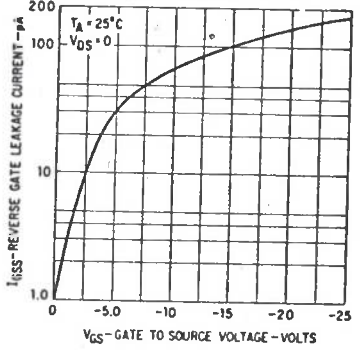
NORMALIZED OUTPUT ADMITTANCE VERSUS AMBIENT TEMPERATURE



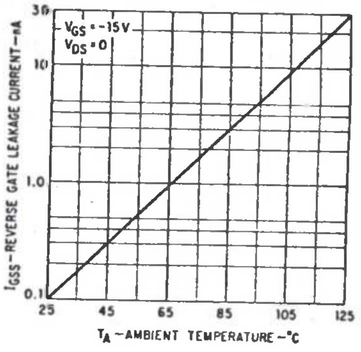
DRAIN SOURCE RESISTANCE VERSUS GATE TO SOURCE VOLTAGE



REVERSE GATE LEAKAGE CURRENT VERSUS GATE TO SOURCE VOLTAGE

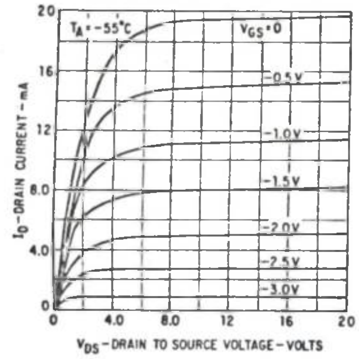


REVERSE GATE LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE



TYPICAL ELECTRICAL CHARACTERISTICS

DRAIN CHARACTERISTICS



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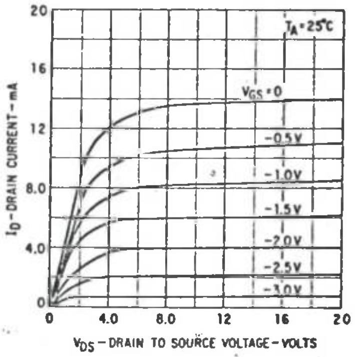

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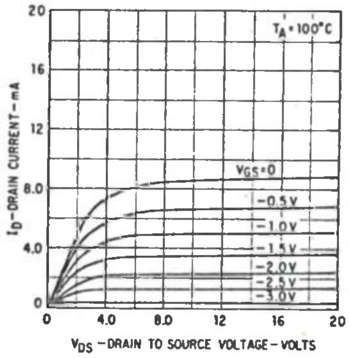
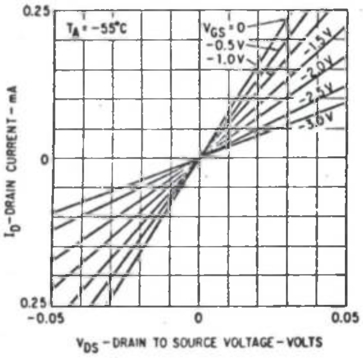
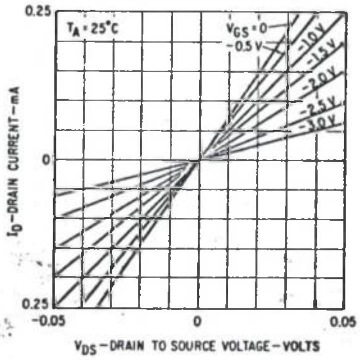


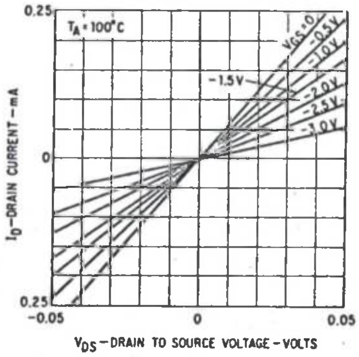
LOW VOLTAGE
DRAIN CHARACTERISTICS



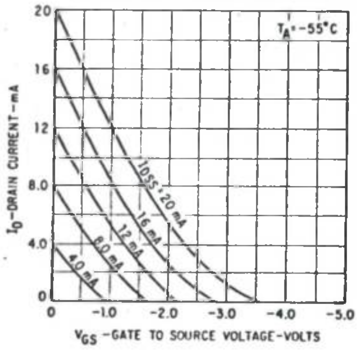
LOW VOLTAGE
DRAIN CHARACTERISTICS



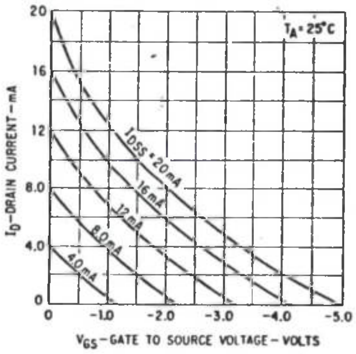
LOW VOLTAGE
DRAIN CHARACTERISTICS



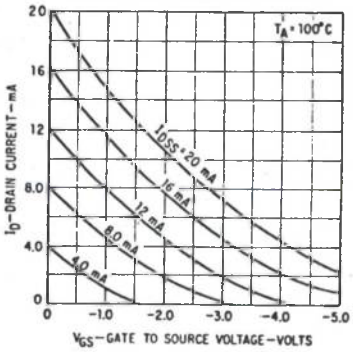
TRANSFER CHARACTERISTICS



TRANSFER CHARACTERISTICS



TRANSFER CHARACTERISTICS



2N5138

PNP LOW-LEVEL AMPLIFIER

DIFFUSED SILICON PLANAR* TRANSISTOR

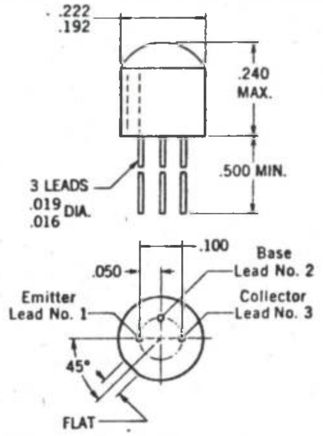
- LOW NOISE FIGURE . . . . 0.7 dB (TYP) AT f = 1 kHz
- HIGH CURRENT GAIN . . . h_{FE} = 100 (TYP) AT I_C = 100 μA
- HIGH BREAKDOWN . . . . . LV_{CEO} = 30 V (MIN)
- EXCELLENT BETA LINEARITY FROM 1 μA TO 50 mA

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures		
Storage Temperatures		−55° to +125°C
Operating Junction Temperatures		+125°C
Lead Temperature (Soldering, 10 second time limit)		+260°C
Maximum Power Dissipation (Notes 2 and 3)		
Total Dissipation at 25°C Case Temperature		0.5 Watt
at 25°C Ambient Temperature		0.2 Watt
Maximum Voltages and Current		
V_{CBO}	Collector to Base Voltage	−30 Volts
V_{CEO}	Collector to Emitter Voltage	−30 Volts
V_{EBO}	Emitter to Base Voltage	−5.0 Volts

PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-106) outline



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram Package
is electrically non-conductive material

ECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

			2N5138				
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
NF	Narrow Band Noise Figure (f = 1.0 kHz) (Note 6)		0.7		dB	I_C = 20 μA	V_{CE} = −5.0 V
NF	Wide Band Noise Figure (Note 7)		1.0		dB	I_C = 20 μA	V_{CE} = −5.0 V
NF	Narrow Band Noise Figure (f = 1.0 kHz) (Note 8)		0.8		dB	I_C = 250 μA	V_{CE} = −5.0 V
h_{FE}	DC Current Gain	50	100	800		I_C = 100 μA	V_{CE} = −10 V
h_{FE}	DC Current Gain	50	110			I_C = 1.0 mA	V_{CE} = −10 V
h_{FE}	DC Pulse Current Gain (Note 5)	50	120			I_C = 10 mA	V_{CE} = −10 V
BV_{CBO}	Collector to Base Breakdown Voltage	−30			Volts	I_C = 100 μA	I_E = 0
V_{CEO}(sust)	Collector to Emitter Sustaining Voltage (Notes 4 and 5)	−30			Volts	I_C = 10 mA (pulsed)	I_B = 0
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0			Volts	I_C = 0	I_E = 100 μA
I_{CBO}	Collector Cutoff Current			10	nA	I_E = 0	V_{CB} = −20 V
I_{CBO}(65°C)	Collector Cutoff Current			3.0	μA	I_E = 0	V_{CB} = −20 V
V_{CE}(sat)	Pulsed Collector Saturation Voltage (Note 5)			−0.3	Volts	I_C = 10 mA	I_B = 0.5 mA
V_{BE}(sat)	Pulsed Base Saturation Voltage (Note 5)			−1.0	Volts	I_C = 10 mA	I_B = 0.5 mA
V_{BE}(on)	Pulsed Base to Emitter "On" Voltage (Note 5)		−0.74	−1.0	Volts	I_C = 10 mA	V_{CE} = −10 V
h_{fe}	Small Signal Current Gain (f = 1.0 kHz)	40		1000		I_C = 1.0 mA	V_{CE} = −10 V
h_{fe}	High Frequency Current Gain (f = 20 MHz)	1.5				I_C = 0.5 mA	V_{CE} = −5.0 V
C_{cb}	Collector to Base Capacitance			7.0	pF	I_E = 0	V_{CB} = −5.0 V
C_{eb}	Emitter to Base Capacitance			30	pF	I_C = 0	V_{EB} = −0.5 V

*Planar is a patented Fairchild process.

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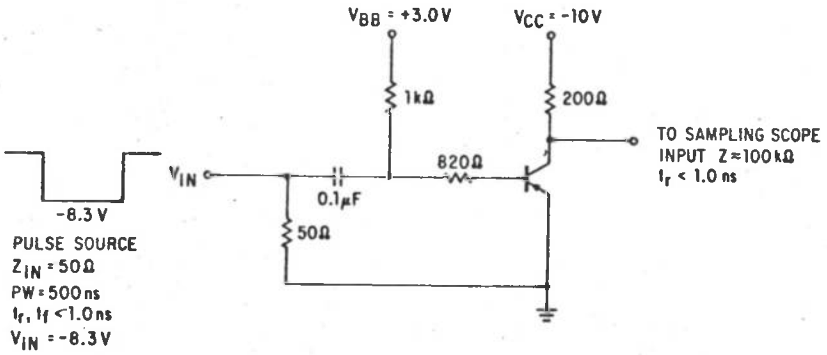
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
V_{CEO}(sust)	Collector to Emitter Sustaining Voltage (Notes 4 and 5)	−20			Volts	$I_C = 10$ mA (pulsed)	$I_B = 0$
BV_{CBO}	Collector to Base Breakdown Voltage	−20			Volts	$I_C = 100\ \mu A$	$I_E = 0$
BV_{CES}	Collector to Emitter Breakdown Voltage	−20			Volts	$I_C = 100\ \mu A$	$V_{BE} = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0			Volts	$I_C = 0$	$I_E = 100\ \mu A$
I_{CES}	Collector Reverse Current			50	nA	$V_{CE} = -15$ V	$V_{BE} = 0$
I_{CES}(+65°C)	Collector Reverse Current			25	μA	$V_{CE} = -15$ V	$V_{BE} = 0$
C_{cb}	Collector to Base Capacitance			5.0	pF	$I_E = 0$	$V_{CB} = -10$ V
C_{eb}	Emitter to Base Capacitance			8.0	pF	$I_C = 0$	$V_{EB} = -0.5$ V

SWITCHING TIME TEST CIRCUIT



2N5138

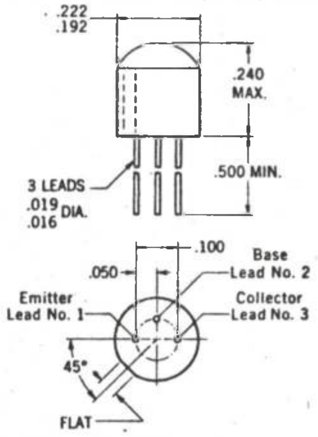
PNP LOW-LEVEL AMPLIFIER

DIFFUSED SILICON PLANAR* TRANSISTOR

- LOW NOISE FIGURE . . . . 0.7 dB (TYP) AT f = 1 kHz
- HIGH CURRENT GAIN . . . $h_{FE} = 100$ (TYP) AT $I_C = 100\ \mu A$
- HIGH BREAKDOWN . . . . . $LV_{CEO} = 30$ V (MIN)
- EXCELLENT BETA LINEARITY FROM 1 μA TO 50 mA

PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-106) outline



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram. Package
is electrically non-conductive material

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures		
Storage Temperatures		−55° to +125°C
Operating Junction Temperatures		+125°C
Lead Temperature (Soldering, 10 second time limit)		+260°C
Maximum Power Dissipation (Notes 2 and 3)		
Total Dissipation at 25°C Case Temperature		0.5 Watt
at 25°C Ambient Temperature		0.2 Watt
Maximum Voltages and Current		
V_{CBO}	Collector to Base Voltage	−30 Volts
V_{CEO}	Collector to Emitter Voltage	−30 Volts
V_{EBO}	Emitter to Base Voltage	−5.0 Volts

ECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	2N5138 MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
NF	Narrow Band Noise Figure (f = 1.0 kHz) (Note 6)		0.7		dB	$I_C = 20\ \mu A$	$V_{CE} = -5.0$ V
NF	Wide Band Noise Figure (Note 7)		1.0		dB	$I_C = 20\ \mu A$	$V_{CE} = -5.0$ V
NF	Narrow Band Noise Figure (f = 1.0 kHz) (Note 8)		0.8		dB	$I_C = 250\ \mu A$	$V_{CE} = -5.0$ V
h_{FE}	DC Current Gain	50	100	800		$I_C = 100\ \mu A$	$V_{CE} = -10$ V
h_{FE}	DC Current Gain	50	110			$I_C = 1.0$ mA	$V_{CE} = -10$ V
h_{FE}	DC Pulse Current Gain (Note 5)	50	120			$I_C = 10$ mA	$V_{CE} = -10$ V
BV_{CBO}	Collector to Base Breakdown Voltage	−30			Volts	$I_C = 100\ \mu A$	$I_E = 0$
V_{CEO}(sust)	Collector to Emitter Sustaining Voltage (Notes 4 and 5)	−30			Volts	$I_C = 10$ mA (pulsed)	$I_B = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0			Volts	$I_C = 0$	$I_E = 100\ \mu A$
I_{CBO}	Collector Cutoff Current			10	nA	$I_E = 0$	$V_{CB} = -20$ V
I_{CBO}(65°C)	Collector Cutoff Current			3.0	μA	$I_E = 0$	$V_{CB} = -20$ V
V_{CE}(sat)	Pulsed Collector Saturation Voltage (Note 5)			−0.3	Volts	$I_C = 10$ mA	$I_B = 0.5$ mA
V_{BE}(sat)	Pulsed Base Saturation Voltage (Note 5)			−1.0	Volts	$I_C = 10$ mA	$I_B = 0.5$ mA
V_{BE}(on)	Pulsed Base to Emitter "On" Voltage (Note 5)		−0.74	−1.0	Volts	$I_C = 10$ mA	$V_{CE} = -10$ V
h_{fe}	Small Signal Current Gain (f = 1.0 kHz)	40		1000		$I_C = 1.0$ mA	$V_{CE} = -10$ V
h_{fe}	High Frequency Current Gain (f = 20 MHz)	1.5				$I_C = 0.5$ mA	$V_{CE} = -5.0$ V
C_{cb}	Collector to Base Capacitance			7.0	pF	$I_E = 0$	$V_{CB} = -5.0$ V
C_{eb}	Emitter to Base Capacitance			30	pF	$I_C = 0$	$V_{EB} = -0.5$ V

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